UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio de Ciencias e Ingenierías

A 3-bit Slope Tracking Type-Analog to Digital Converter (STT-ADC) in SKYWATER 130nm Technology

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Ingeniería en Electrónica y Automatización

Trabajo de fin de carrera presentado como requisito
para la obtención del título de
Ingeniero en Electrónica y Automatización

Quito, 20 de Diciembre de 2024

UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio del Politécnico

HOJA DE CALIFICACIÓN
DE TRABAJO DE FIN DE CARRERA

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Quito, 20 de Diciembre de 2024

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Lugar y fecha: Quito, 20 de Diciembre de 2024

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Resumen

Este proyecto emplea la tecnología de semiconductores complementarios de óxido metálico (CMOS) del kit de diseño de procesos (PDK) de 130 nm de SKYWATER para construir e implementar un convertidor analógico a digital de tipo de seguimiento de pendiente de 3 bits (STT-ADC). Al adaptarse dinámicamente a la pendiente de la señal de entrada, el STT-ADC sugerido logra una reducción de potencia de más del 70 % en comparación con el ADC Flash convencional [1], al tiempo que conserva un rendimiento de retardo competitivo con solo un aumento del 18,7 % en el retraso en las peores condiciones. Además, en comparación con el ADC de tipo de seguimiento (TT-ADC) de última generación [2], el STT-ADC ofrece una reducción del 88 % en el retraso al tiempo que mantiene una eficiencia energética comparable, con una compensación de un consumo de energía un 22 % mayor en las peores condiciones. El circuito incorpora módulos optimizados para un bajo consumo de energía y un área de silicio pequeña, incluidos amplificadores operacionales, un convertidor digital a analógico y un circuito de muestreo y retención. Los resultados de la simulación resaltan el potencial de la arquitectura para sistemas de sonido y sensores en aplicaciones integradas y de Internet de las cosas (IoT), donde la confiabilidad y la eficiencia son cruciales. Las investigaciones futuras investigarán la escalabilidad para lograr una mayor resolución y una mejor eficiencia energética.

Palabras clave: ADC, SKYWATER $130nm$, seguimiento basado en pendiente, ADC de tipo seguimiento, Diseño analógico, Diseño digital, Nivel de circuito

Abstract

This project employs SKYWATER 130nm Process Design Kit (PDK) Complementary Metal-Oxide Semiconductor (CMOS) technology to build and implement a 3-bit Slope Tracking Type Analog-to-Digital Converter (STT-ADC). By dynamically adapting to the slope of the input signal, the suggested STT-ADC achieves a power reduction of over 70% compared to conventional Flash ADC [1], while preserving competitive delay performance with only an 18.7% increase in delay under worst-case conditions. Additionally, when compared to the state-of-the-art Tracking-Type ADC (TT-ADC) [2], the STT-ADC offers an 88% reduction in delay while maintaining comparable power efficiency, with a trade-off of 22% higher power consumption under worst-case conditions. The circuit incorporates modules optimized for low power consumption and small silicon area, including operational amplifiers, a digital-to-analog converter, and a sample-and-hold circuit. Simulation results highlight the architecture's potential for sound and sensor systems in embedded and Internet of Things (IoT) applications, where dependability and efficiency are crucial. Future research will investigate scalability for higher resolution and improved energy efficiency.

Keywords: ADC, SKYWATER 130nm, Slope Tracking Type, Tracking-Type ADC, Analog Circuit Design, Digital Circuit Design, Circuit-Level

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General Objective

- Explore and Design a 3-bit Tracking Type Analog-to-Digital Converter topologies in $130nm$ Complementary Metal-Oxide-Semiconductor (CMOS) technology Full Custom at circuit-level

Specific Objectives

- Perform system-level test of concept of the proposed converter.
- Employ a $130nm$ Process Design Kit (PDK) from SKYWATER to implement the transistor-level design, simulate it, and perform tests.
- Evaluate performance, operating characteristics, and delay and power consumption analysis.
- Compare the proposed ADC against the current state-of-the-art ADC architectures and chip design with 3-bit resolution.

1 Introduction

Analog to Digital Converters (ADCs) are widely used in electronic systems. Their primary purpose is to transform signals of an analog nature (continuous in time and amplitude) into digital signals (discrete in time and amplitude) for processing and analysis. Most of these analog signals are captured from the external environment by sensors or transducers and fed into an embedded electronic device, where they are converted and processed, as mentioned in [3].

Flash ADC architecture is known for their high speed but suffer from significant power consumption, as detailed in [1], while Sigma-Delta ADCs prioritize resolution over speed and bandwidth, studied in [4]. The present Slope Tracking Type (STT) ADC, based on the work explored in [2], aims to bridge these performance gaps with a hybrid approach. This architecture targets applications in sound and sensor systems, where power efficiency is critical due to constraints in embedded systems and IoT devices.

The primary application of these circuits is to retrieve physical variables from processes such as temperature, flow, pH, light, weight, or sound. Additionally, most electrical instrumentation, including multi-meters, requires an ADC to display the measured electrical values, as explored in [5]. Specifically, this research focuses on sound [6], sensors, and instrumentation [5]. Based on these requirements, the operating frequency range is between $50[Hz]$ and $25[kHz]$. This implies that, regardless of the ADC circuit's bandwidth, all frequency-related measurements fall within the specified operating range.

The key aspects of an ADC are sampling rate, resolution, conversion time, and power consumption [7]. These parameters serve as a performance and efficiency guide to determine whether the converter is suitable for a specific application. The purpose of this proposal is to develop an architecture that not only reduces power consumption but also offers a simple way to increase bit resolution at the circuit schematic level, all while maintaining optimal delay and reliable operation.

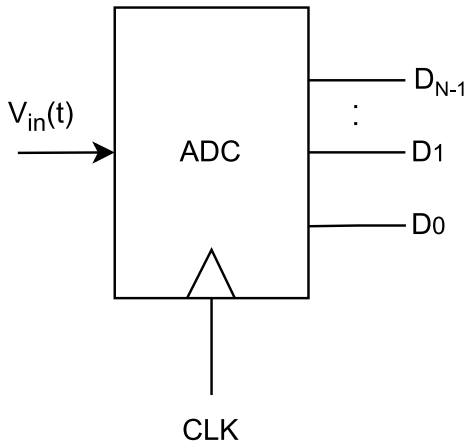


Figure 1: General N-bit ADC Block.

Figure 1 represents the general block of an ADC [3] with two inputs: $V_{in}(t)$ and a clock signal CLK. $V_{in}(t)$ represents the analog input signal, which is continuously varying over time, while the CLK signal is used to sample this input at specific intervals. The output consists of N digital bits, labeled D_0 to D_{N-1}, which represent the binary encoded value of the sampled analog signal. These bits form the digital representation of the analog input for further processing.

Various ADC schemes and architectures have been proposed over the years. Architectures such as Flash ADC [1], Sigma-Delta ADC [4], and Successive Approximation Register (SAR) ADC [8] have gained recognition due to their effectiveness, ease of implementation, or high bandwidth. Each of these architectures offers distinct advantages depending on the application, such as speed, accuracy, or power efficiency.

2 Proposal

2.1 Overview and Operation

The proposed ADC scheme is based on tracking the monotony of the input analog signal [2]. The conversion process is carried out by a counter that increments or decrements based on the sign of the signal's slope and the converter's current state. Figure 2 presents the system-level architecture of the STT-ADC, detailing the analog, combinational, and sequential modules within the design.

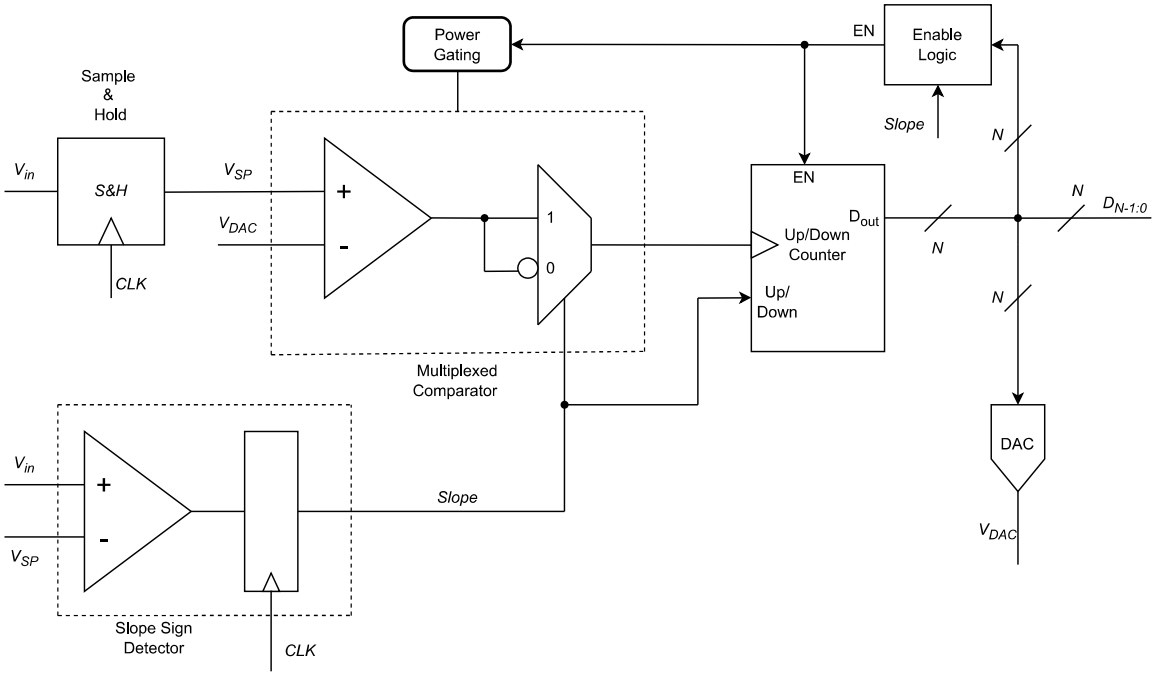


Figure 2: Proposed Slope Tracking Type-ADC (STT-ADC) Scheme.

The core of the circuit is the up/down counter, which generates the digital representation of the analog signal. This counter is activated whenever the analog signal is either at its maximum or minimum level. The direction of the counter is determined by the sign of the input signal's derivative. Moreover, the counter is triggered whenever there is a change in the current level of the analog signal, which is detected by the multiplexed comparator module.

The multiplexed comparator receives its input from the power gating module, whose purpose is to deactivate the multiplexed comparison module when its signal is not in use, optimizing power consumption. To accurately determine the sign of the derivative and ensure correct operation, the input signal is sampled, and its final value is held for further processing.

On the other hand, the current state-of-the-art includes the ADC topology on which the proposed design is based. This ADC architecture, known as the Tracking-Type ADC (TT-ADC) [2], is illustrated in Figure 3. The TT-ADC operates by periodically sampling employing a sawtooth signal, as described in [2]. The primary advantage of this topology is its ability to sample at varying levels while requiring a reduced number of electrical components, which enhances its efficiency and simplifies implementation.

Figure 4 shows the Transfer Curve (TC) of a 3-bit ADC. Each digital value (in hexadecimal) is associated with an analog voltage interval. The width of each interval is the maximum analog input voltage, V_{MAX} divided by $2^N - 1$. In this case, $V_{MAX} = 1[V]$ and $N = 3$ bits. In total, there are 2^N intervals distributed uniformly between $0[V]$ and V_{MAX}.

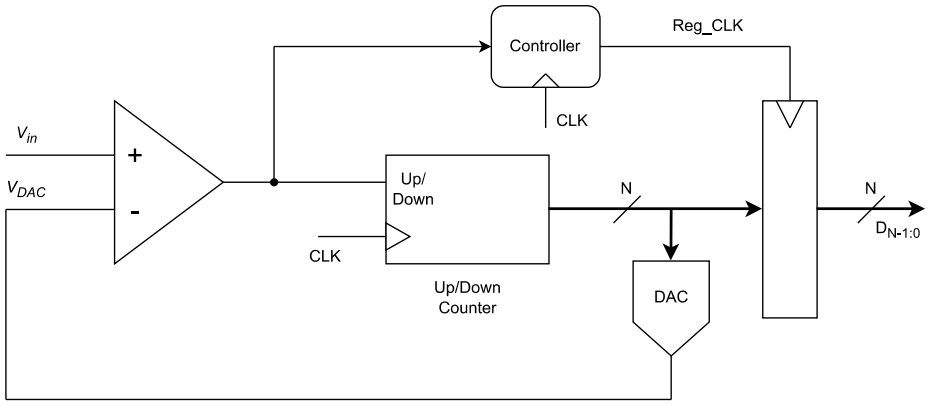


Figure 3: Current State-of-the-Art Tracking Type-ADC (TT-ADC) Scheme.

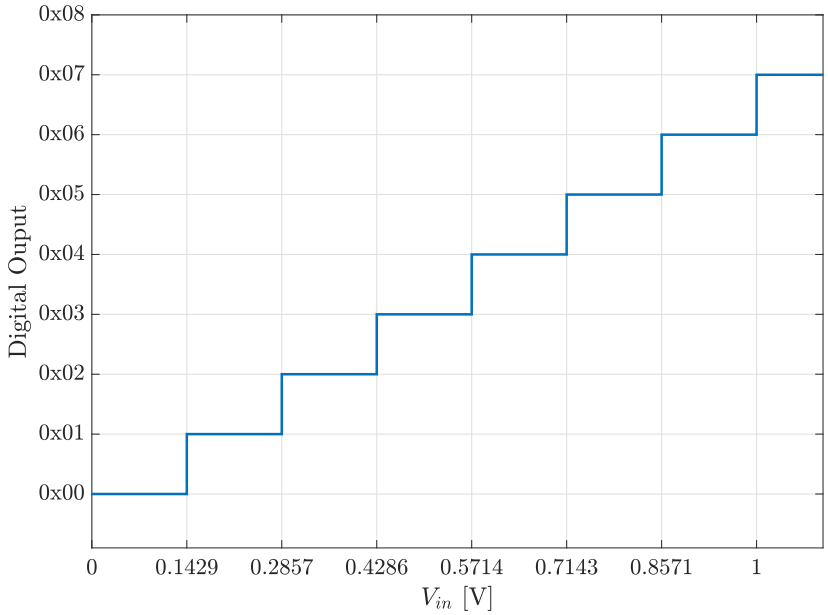


Figure 4: ADC Transfer Curve.

2.2 System-Level Concept Testing

To validate the predicted behavior of the STT-ADC, a system-level simulation was performed using Matlab/Simulink. The simulation utilized a sine wave input signal with a frequency of $1[kHz]$, ranging from $0[V]$ to $1[V]$.

As shown in Figure 5, each module is implemented using ideal analog, combinational, and sequential blocks. It is important to note that the Enable Logic and DAC modules must be sequential to ensure proper functioning of the simulation environment, due to feedback loops generated between these blocks and the counter module.

Figure 6 demonstrates the expected behavior of the system. Whenever the sampled input signal

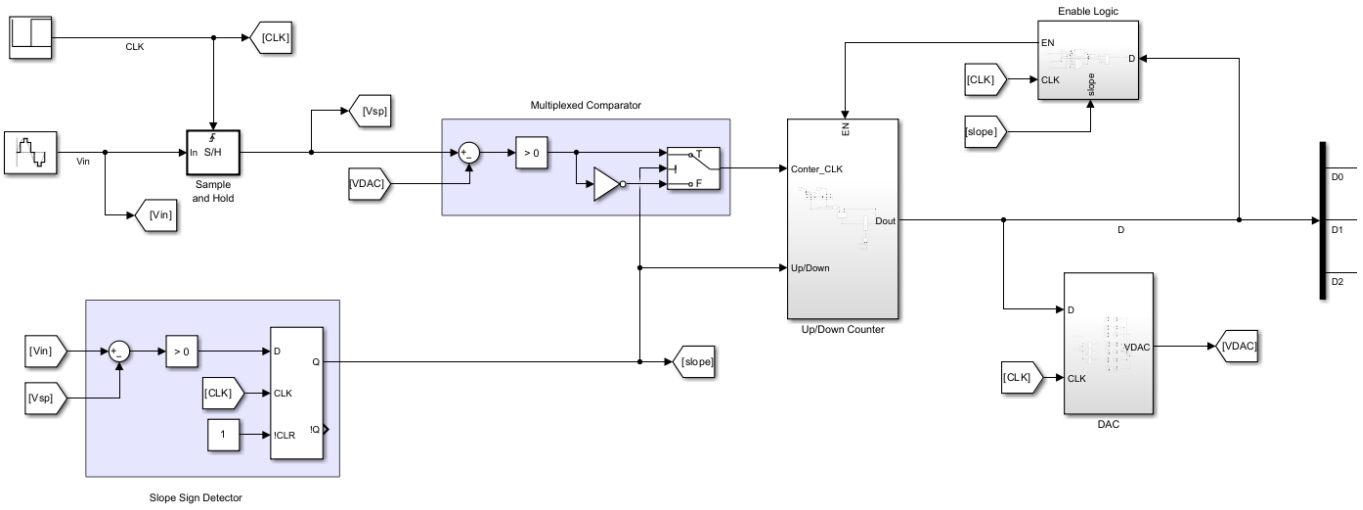


Figure 5: STT-ADC System-Level Implementation in Simulink Software.

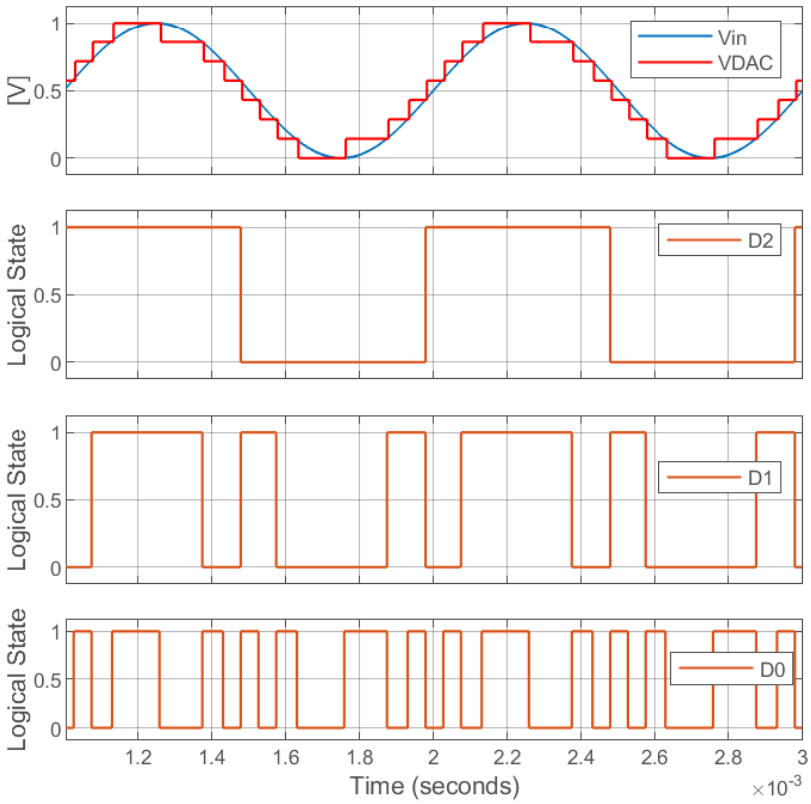


Figure 6: STT-ADC System-Level Response.

intersects with the DAC voltage stair-step level, the counter increments when the slope is positive and decrements when the slope is negative. Additionally, when the analog signal reaches its maximum or minimum value, the system pauses and waits for a change in slope before adjusting to a higher or lower level. The 3-bit digital output encodes the discrete amplitude levels of the input signal, representing

2^3 different levels, ranging from 0 to 7, as described in Figure 4.

The system-level simulations verify the basic functionality of the STT-ADC, given its use of sequential logic and optimized signal processing. The ability of the architecture to adjust dynamically to the slope of the input signal ensures efficient tracking, even in varying conditions. These results pave the way for further exploration into improving resolution and integrating the design into practical applications, where minimal power consumption and reliable performance are critical.

3 Circuit-Level Implementation

To evaluate and compare performance under similar operating conditions, three ADC architectures were implemented using SKYWATER $130nm$ CMOS technology: the Flash ADC, based on the structure described in [1], the Tracking-Type ADC (TT-ADC) [2], which has only been demonstrated at the system level and has not been implemented in the literature, and the proposed Slope Tracking Type ADC (STT-ADC). The STT-ADC was developed using carefully optimized building blocks, including a Sample-and-Hold circuit, a Digital-to-Analog Converter (DAC), and an operational amplifier designed as a comparator. These implementations enable a comprehensive comparison of power consumption, timing precision, and overall performance for each architecture.

The next step is to design a functional circuit in $130nm$ Complementary Metal-Oxide-Semiconductor (CMOS) technology, based on [9], employing the Synopsys Custom Compiler simulation software. The primary challenges in this process involve the circuit-level implementation of key modules, such as the DAC, Sample and Hold, and comparator based both on digital design [10] and analog design [3]. Each module requires specific design rules and parameter optimization techniques, which must be addressed efficiently with the provided guide on [11]. In particular, when designing an ADC at this level, it is crucial to achieve the desired sampling rate, minimize conversion time, and reduce power consumption, all while maintaining a compact silicon footprint. All modules must be optimized to obtain these ADC circuit-level characteristics.

The Slope Tracking Type ADC module, in simple terms, consists of two main components: the controller and a 3-bit up/down counter. The controller captures the analog input signal, reads the current state of the counter, and supplies the clock, up/down, and enable signals to control the digital counter.

Furthermore, each module will be thoroughly examined, with a focus on both operational principles and circuit-level implementation.

3.1 Digital Components Design

3.1.1 Combinational Logic

All digital components are implemented at the transistor level in a $130nm$ CMOS Process Design Kit (PDK). In digital design, as explored in [10], the foundational elements are combinational modules, which are constructed using logic gates. In CMOS technology [11], the low-level transistor-efficient logic gates are the basic inverter (NOT), NAND, NOR, XOR/XNOR, and a non-restoring 2-to-1 multiplexer (MUX) [11]. All of these logic gates are implemented employing the minimum transistor sizing based on a 2-to-1 inverter [11].

A combinational building block needed for the circuit implementation is full-carry adder [10]. This component is implemented with the NAND-based design proposed in [12]. Figure 7 shows the implementation of an N-bit ripple-carry adder employing a full adder.

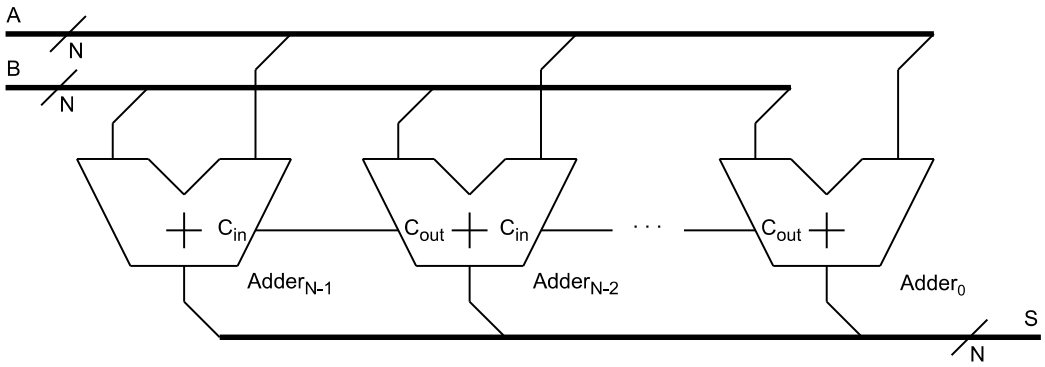


Figure 7: N-bit Ripple-Carry Adder.

3.1.2 Sequential Logic

The next step is to implement the sequential logic [10], where the outputs depend on both the inputs and the circuit's current state. The fundamental cell in sequential logic is the flip-flop or register, which is realized through combinational logic arranged in a feedback loop, as detailed in [11].

With these components implemented in $130nm$ CMOS technology, the core of the circuit can be constructed. The up/down counter is controlled by three signals: CLK, $Up/Down$, and EN. As shown in Figure 8, the positive edge of the CLK signal triggers the register to store the output of the full-adder. The adder computes the sum of the current state of the counter and the output of a multiplexer, which selects either 0x1 or 0xF for a 3-bit counter. Here, adding 0xF is equivalent to subtracting 0x1, enabling the counter to increment or decrement. This setup allows the counter to count up or down on each rising edge of CLK, provided that EN is asserted.

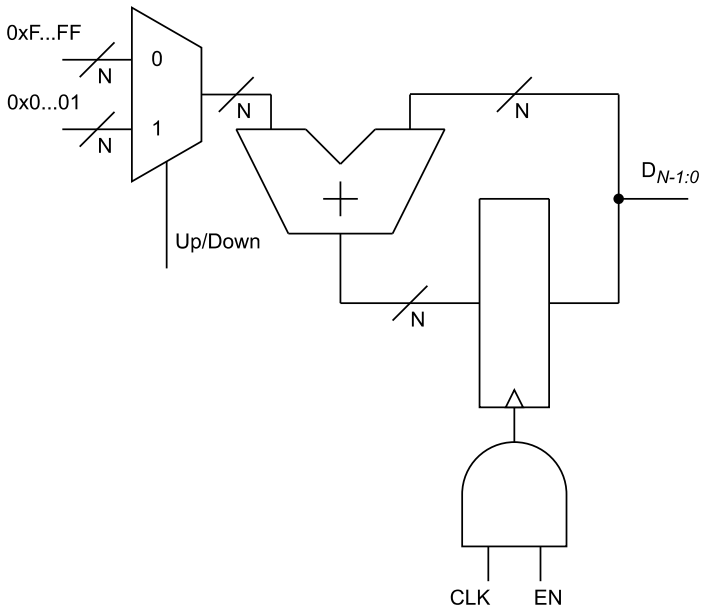


Figure 8: Up/Down Counter with Enable

3.2 Analog Components Design

The analog components present in the STT-ADC architecture are the Sample & Hold (S&H), the Digital-to-Analog Conver (DAC), and the Operational Amplifier (Op-Amp) as comparator.

3.2.1 Sample & Hold

The basic principle of the S&H circuit [3] is to pass the analog signal when the CLK signal is asserted and hold it last value when the CLK signals changes to zero. This circuit is constituted by two main components, a switch controlled by CLK and a hold capacitor connected to discharge. The implementation of the sample & hold circuit is employing a transmission gate [11] as a switch and a CMOS capacitor [11] in the schematic shown in [3] and depicted in Figure 9. This design leverages a CMOS transmission gate for minimal leakage and robust signal integrity, crucial in scaled-down technology $130nm$.

3.2.2 Digital-to-Analog Converter (DAC)

Another essential analog component is the Digital-to-Analog Converter (DAC) [3]. This component provides a Direct Current (DC) voltage level to the controller, which is used to compute the clock signal, CLK, for the counter. The DAC in this design converts an N-bit digital signal into a specific DC voltage level. Implementation in CMOS technology without an operational amplifier is achieved by employing a CMOS voltage divider to produce N discrete voltage levels between GND and a reference V_{ref}. An N-to-1 non-restoring multiplexer [11] is then connected to each voltage level to select and

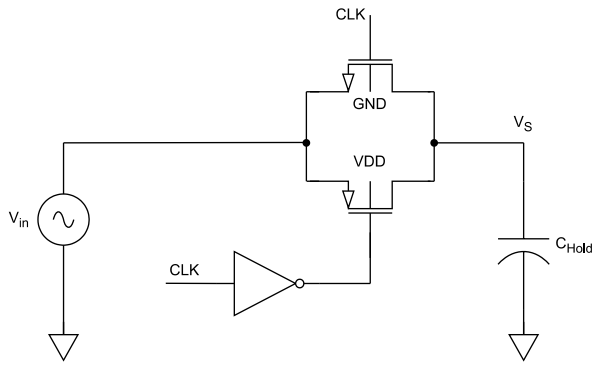


Figure 9: Sample & Hold CMOS Circuit Implementation.

output the corresponding DC voltage. The select N-bit bus of the multiplexer is connected to the digital output of the counter, $D_{N-1:0}$, allowing the DAC to output the voltage level corresponding to the counter's current state. The non-restoring MUX is essential as it directly passes the voltage from the selected node in the CMOS voltage divider to the output.

Figure 10 shows the schematic of the proposed CMOS DAC, which is based on voltage dividers and non-restoring multiplexers. As depicted, all transistors that constitute the voltage divider must have the same aspect ratio, w/L, to ensure equal resistance across each transistor. This configuration allows the reference voltage, V_{ref}, to be divided into uniformly distributed voltage levels between GND and V_{ref}. It should also be noted that the number of transistors in the CMOS voltage divider is $2^N - 1$, where N is the resolution of the DAC.

3.3 Operational-Amplifier (Op-Amp)

To build modules such as a multiplexed comparator or a derivative sign detector, it is essential to design and implement a CMOS Op-Amp [3]. These analog circuits require careful attention to transistor sizing. Even when the same topology is selected [3], the operating points and electrical characteristics of each Op-Amp can vary significantly, impacting overall performance.

3.3.1 VerilogA Model

Before constructing a real transistor-based comparator, a block verification is carried out. In transistor-level design, there can be implemented very complex modules such as an Op-Amp in VerilogA compact modules, which provide a guide to understand the behavior the circuit should have. The VerilogA code for an ideal comparator is described as follows:

```
// VerilogA for VerilogTests, comparator, verilog
```

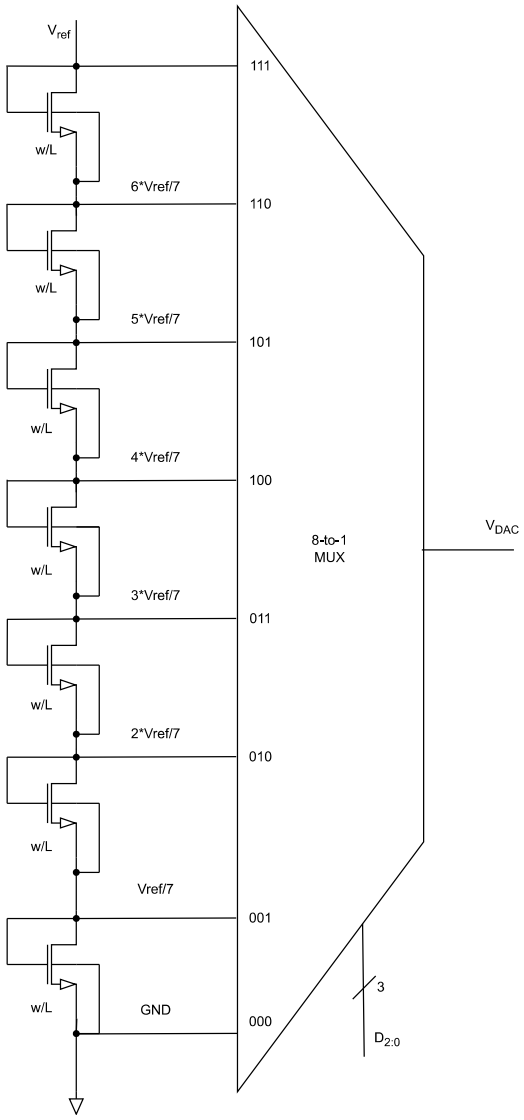


Figure 10: 3-bit CMOS DAC Implementation.

```
‘include "constants.vams"
‘include "disciplines.vams"

module Comparator(V_plus, V_minus, VDD, VSS, V_out);

input V_plus, V_minus;
inout VSS, VDD;
output V_out;

parameter delay=0, ttime=1p;
```

```
electrical V_plus, V_minus, VDD, VSS, V_out;
real result;

   analog begin
   @(cross((V(V_plus)-V(V_minus)),0) or initial_step)

      if (V(V_plus)>=V(V_minus))
         result=V(VDD);
      else
         result=V(VSS);

      V(V_out)<+ transition(result,delay, ttime);

   end

endmodule
```

This ideal module outputs V_{DD} when $V_{plus} >= V_{minus}$ and V_{SS} (GND) otherwise. After verifying that the ideal comparator produces the desired behavior in simulation, the design and implementation of a real CMOS Op-Amp is now ready to proceed.

3.3.2 Topology Selected

When designing an Op-Amp, the first step is to select an appropriate topology, such as those provided in [3]. For the intended application, the Op-Amp will function as a comparator, requiring rail-to-rail output response in reaction to minimal changes at its differential input. Achieving this performance demands a high DC gain and a fast slew rate. Figure 11 shows the schematic of the topology best suited for the comparator application: a two-stage CMOS Op-Amp with PMOS transistors at the differential input, as proposed by [3].

It is important to note that the reference voltage V_{bias} must be within a specific range to ensure that the voltage at the node connecting the gate terminals of transistors M_8 and M_5 is $V_{G_{8,5}} = VDD - |V_{TH_P}|$, assuming a negligible overdrive voltage $V_{OV_{8,5}} \approx 0$. This condition maximizes both the input and output swing of the amplifier [3]. The reference voltage V_{bias} is generated using a CMOS voltage divider composed of two NMOS transistors. Each transistor's size is carefully adjusted to achieve the desired voltage $V_{G_{8,5}}$. The threshold voltage V_{TH_P} can be determined through a DC analysis (I_D vs. V_{SG}) of the transistor or obtained from the transistor's specifications in the PDK. Additionally, all PMOS bulk terminals should be connected to V_{DD} and all NMOS bulk terminals to GND.

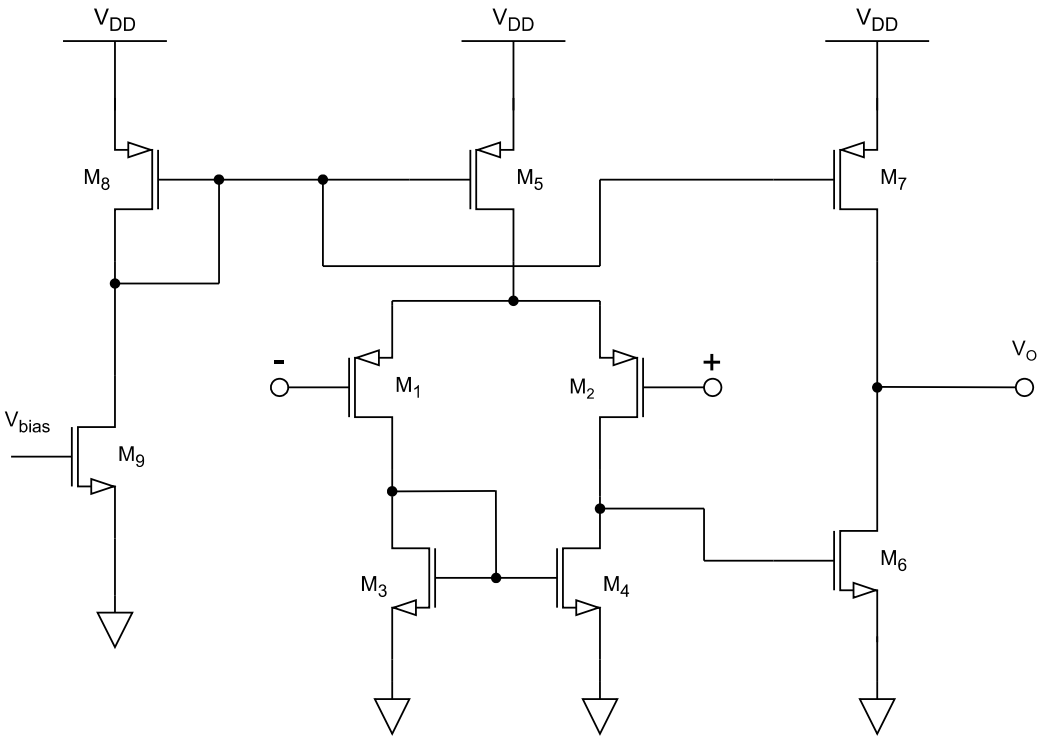


Figure 11: Two-Stages CMOS Op-Amp.

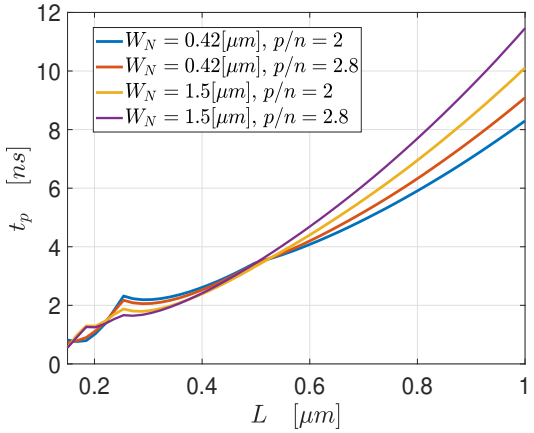
3.3.3 Sizing by Sweeping

As an initial guideline, the width of each PMOS transistor, W_P, is set to twice the width of each NMOS transistor, W_N. For simplicity, all transistors share the same length, L. In this initial design approach, w_N and L are set to the minimum values permitted by the PDK.

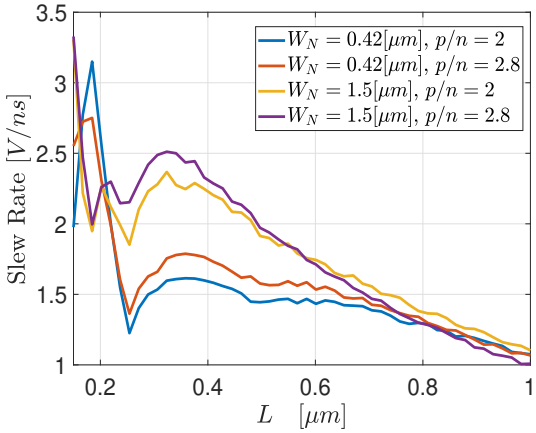
To achieve optimal transistor sizing, a parameter sweep is conducted. The three main parameters to sweep are L, W_N, and the p/n ratio, which represents the PMOS to NMOS width ratio. Following the sweep, four key electrical characteristics of the comparator are measured: propagation delay (t_p), slew rate (SR), total power consumption, (P), and DC gain (G). The optimization process aims to minimize t_p and P, while maximizing SR and G.

This process involves measuring curves as a function of L ranging from its minimum length value ($0.15[\mu m]$ in the SKYWATER $130nm$ PDK) to $1[\mu m]$, with 50 data points. To simplify computation time and optimize analysis, W_N is set to $0.42[\mu m]$ (minimum width) and $1.5[\mu m]$ to simplify time computation and optimization analysis. Lastly, the p/n ratio is set to values of 2 (initial approach) and 2.8 for simplicity. Figure 12 shows the sweeping analysis of the main electrical characteristics of the two-stages CMOS Op-Amp.

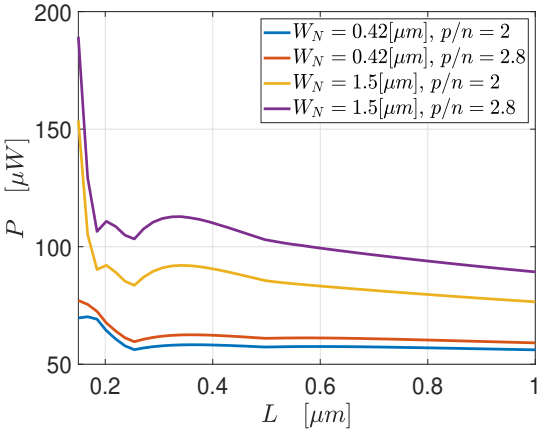
After analyzing the four parameter curves illustrated in Figure 12, the optimal sizing values were



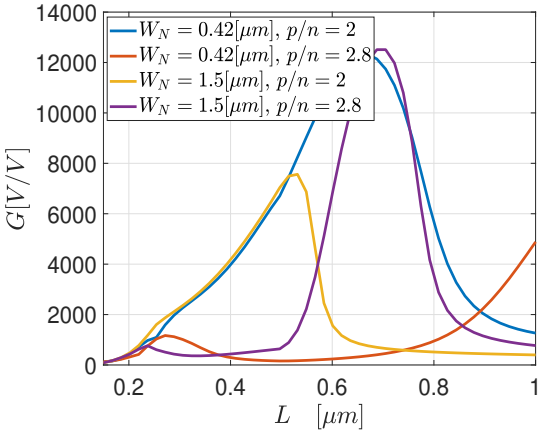
(a) Op-Amp Delay Sweeping Measurements.



(b) Op-Amp Slew Rate Sweeping Measurements.



(c) Op-Amp Power Sweeping Measurements.



(d) Op-Amp Gain Sweeping Measurements.

Figure 12: CMOS Op-Amp Sweeping Analysis Curves.

determined to be $W_N = 0.42[\mu m]$, $L = 0.4[\mu m]$, and a p/n ratio of 2. These values were carefully selected to minimize power consumption while achieving a significantly high DC gain, as illustrated in Figures 12c and 12d, respectively. Additionally, the delay curves present a relatively flat trend, maintaining monotonicity in a zone of slow growth, as suggests Figure 12a. Figure 12b exhibits, that the SR value is also near its local maximum within the range of $0.2[\mu m]$.

3.3.4 Op-Amp Characteristics

Now that the Op-Amp is designed and optimally sized, a characteristics analysis is required to quantify the performance and operating region of the CMOS amplifier. This evaluation includes examining electrical parameters and behavioral responses under varying environmental conditions and operating points.

The electrical characteristics of an Op-Amp provide essential information about its operational region, maximum absolute values, and appropriate operating conditions. While there are many elec-

trical characteristics to consider, this research focuses on power consumption, transport delay, SR, offset voltage between differential inputs at open circuit, Common-Mode Rejection Ratio (CMRR), and Power Supply Rejection Ratio (PSRR).

Table 1: CMOS Op-Amp Typical Electrical Characteristics @$T = 25[^{\circ}C]$

Parameter	**Description**	**Value**
P	Total Power Consumption	58.18 $[\mu W]$
t_p	Propagation Delay	2.61 $[ns]$
SR	Slew Rate	1.6 $[V/ns]$
G	DC Gain	71.98 [dB]
BW	Bandwidth	1.702 $[MHz]$
V_{off}	Differential Input Offset Voltage	0.161 $[mV]$
$CMRR$	Common-Mode Rejection Ratio	90.57 [dB]
$PSRR$	Power Supply Rejection Ratio	116.97 [dB]

Table 1 presents the electrical characteristics of the Op-Amp at the corner of the typical-typical (TT) process [11] and a standard ambient temperature of $T = 25[^{\circ}C]$. It is important to note that these typical characteristics may vary significantly based on post-layout implementation or fabrication processes. Therefore, measuring the circuit at different operating points and process corners is essential [11]. The critical values affecting amplifier performance are also those that ensure optimal sizing. Key parameters such as power consumption, delay, SR, and gain are vital to achieving proper module electrical behavior.

The performance characteristics provide a graphical analysis of the amplifier's behavior under various conditions. Figure 13 illustrates the transient response of the Op-Amp as it transitions from low to high at both its input and output. The test involves applying a square V_{pulse} signal and comparing it with a fixed DC voltage. Notably, to fully capture t_p and SR, the measurement process shown in Figure 13 includes both rising and falling transient responses.

To ensure proper frequency operation, an Alternate Current (AC) analysis is required [3]. The Bode plot is the most widely used tool for illustrating and understanding an AC response [13]. This plot provides both the Op-Amp's DC gain G and bandwidth BW. Figure 14 shows the frequency response of the CMOS amplifier. To determine G, the magnitude plot is measured at low frequencies, below $1[kHz]$. In contrast, BW is defined as the frequency at which the gain decreases by $3dB$ from the DC level or reaches a phase shift of -5°. The bandwidth is determined by the condition that occurs first, at a lower frequency.

A desired property of an Op-Amp is linearity. This characteristic not only ensures proper operation,

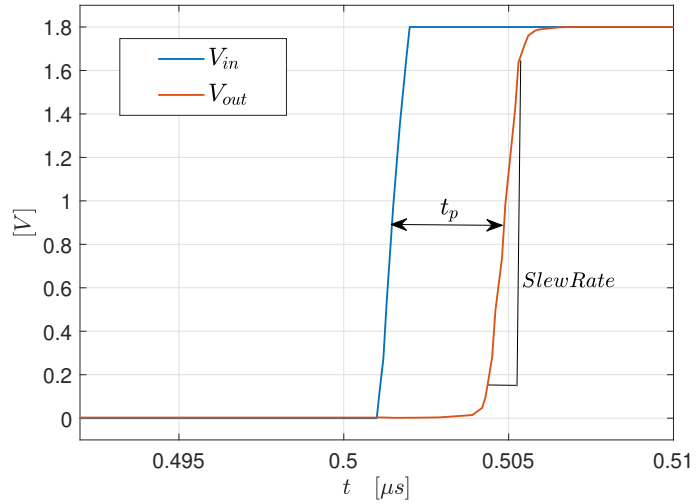


Figure 13: CMOS Op-Amp Transient Response.

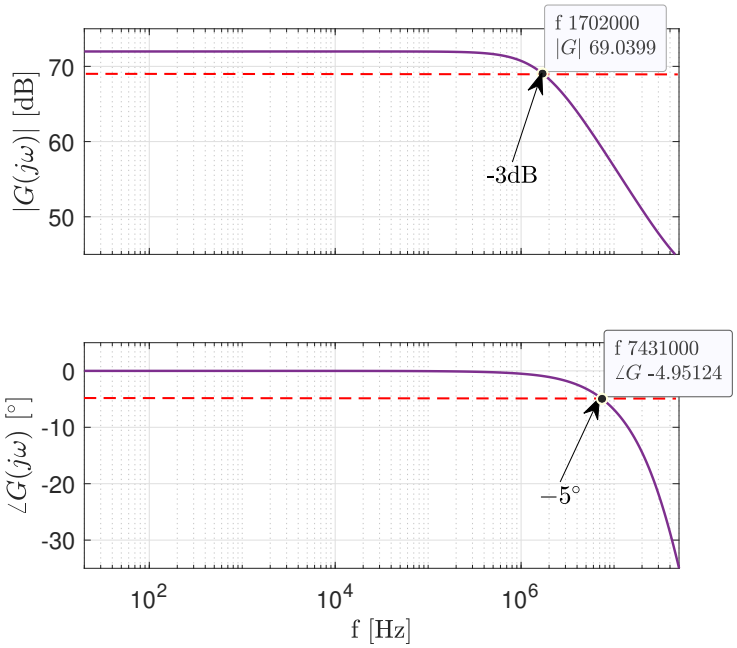


Figure 14: CMOS Op-Amp Bode Plot.

but also provides a straightforward way to predict its behavior, simplifying both digital and analog designs that involve comparators. A direct way to get the linear region of the amplifier is a DC sweep with the amplifier in buffer connection [3]. If the amplifier is linear, the V_{in} vs. V_{out} curve should be a linear function with unitary slope.

Figure 15 shows the DC sweep curve of the CMOS amplifier, plotting V_{in} vs. V_{out}. As illustrated, the Op-Amp exhibits linear behavior from GND to $0.819V_{DD}$. This curve defines the range of input

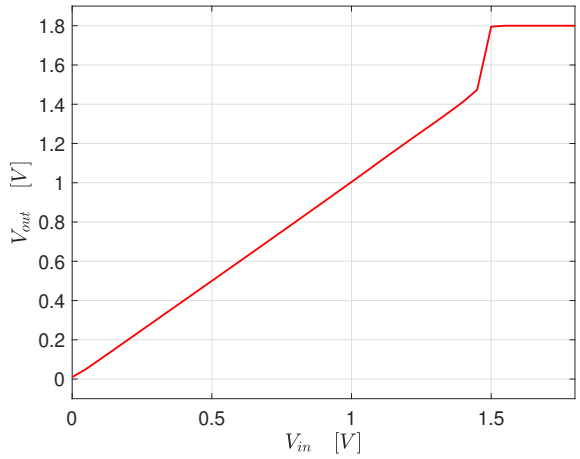


Figure 15: CMOS Op-Amp DC Linearity Analysis.

voltages that can be processed with linear behavior. In this research, to ensure proper linear operation, all signals entering the differential inputs of each comparator are constrained within a range of $0[V]$ to $1[V]$.

Temperature is a variable that affects circuit operation and causes parameter variations. To ensure that the Op-Amp will perform reliably under these changes once fabricated, temperature sweeps and process corner analyses are necessary.

Figure 16 shows the four main electrical characteristics of the CMOS amplifier under different fabrication process corners: Slow-Slow (SS), TT, and Fast-Fast (FF) and a temperature sweep from $0[°C]$ to $100[°C]$. As depicted in Figures 16c and 16d, the amplifier's power and DC gain are the most significantly affected electrical parameters under temperature variation. Conversely, fabrication process corners have a minimum impact on delay and SR, as Figures 16a and 16b show respectively.

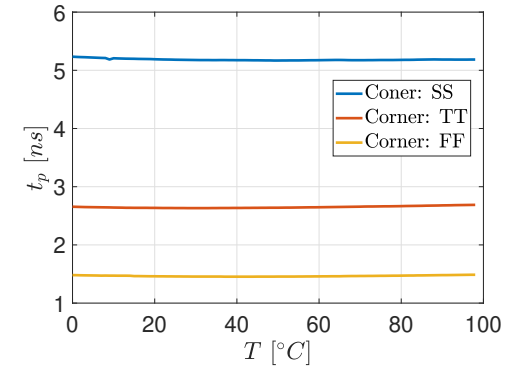
These results aim to ensure the environmental robustness of the Op-Amp. With these considerations in place, the CMOS amplifier is now ready to be used as a comparator in both analog and digital circuit designs.

3.4 Slope Sign Detector

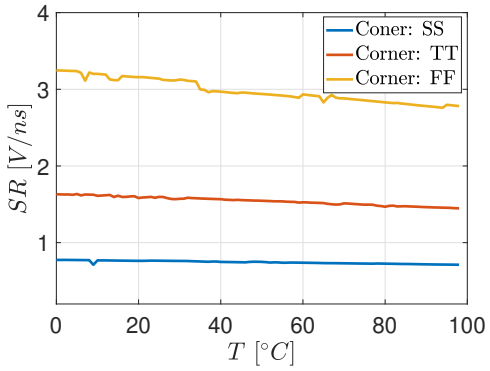
The discrete derivative of a signal could be expressed as a difference equation [14] :

$$x'[n] = x[n] - x[n-1] \tag{1}$$

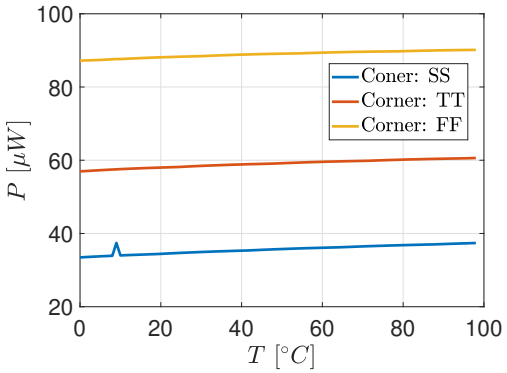
The sample-and-hold $S\&H$ circuit shown in Figure 9 directly computes the $x[n-1]$ signal when its clock CLK transitions to 0. The difference between the instantaneous value of the input signal, $V_{in}(t)$



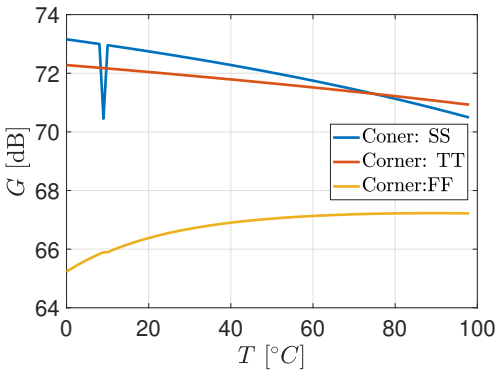
(a) Op-Amp Delay Corners Measurements.



(b) Op-Amp Slew Rate Corners Measurements.



(c) Op-Amp Power Corners Measurements.



(d) Op-Amp Gain Corners Measurements.

Figure 16: CMOS Op-Amp Temperature Sweeping Analysis.

and the sampled value, $V_{sp}(t)$, represents the sampled derivative of the signal. When the sample-and-hold CLK is asserted, this difference is zero, as $V_{in}(t)$ is equal to $V_{sp}(t)$. To generate a digital control signal representing the current derivative's sign, the sampled derivative is compared to GND. In this configuration, the *Slope* signal is set to 1L if the derivative is positive and to 0L otherwise. To implement a complete derivative sign detector, the comparator output is then connected to a register, which synchronizes and captures only the logical values for subsequent processing.

Figure 17 presents a time diagram illustrating the operation of the slope sign detector circuit. The input signal is a sine wave oscillating between $0[V]$ and $1[V]$ at a frequency of $12.5[kHz]$, chosen to emulate a typical analog signal in many signal processing or control system applications. The clock signal (CLK) operates at a much higher frequency of $250[kHz]$, which is 20 times the frequency of the input signal ($20 \cdot f_{in}$), ensuring sufficient sampling resolution to capture the input signal's dynamic behavior accurately.

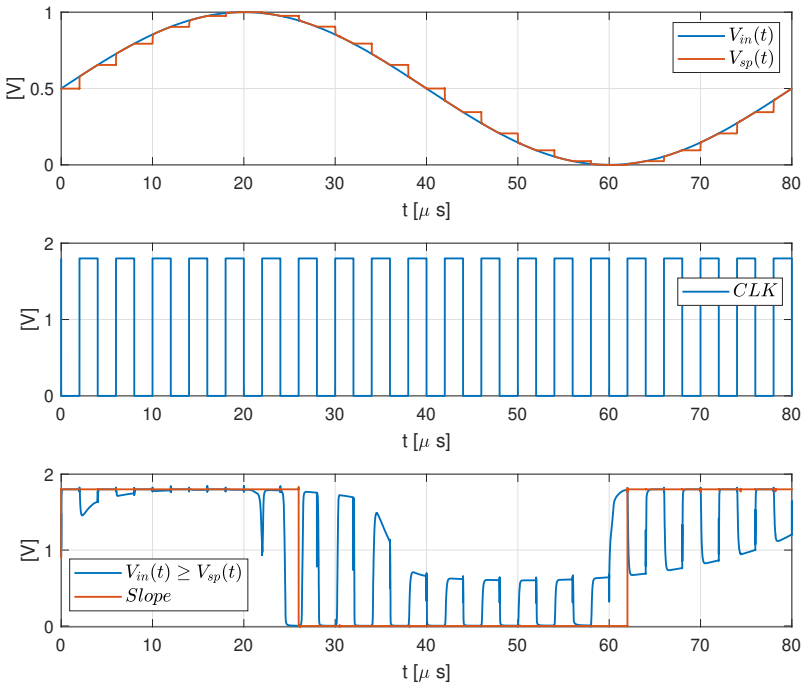


Figure 17: Slope Sign Detector Signals.

3.5 Controller Operation

The controller comprises both analog and digital components. Upon entering the controller, the input signal is sampled and held to ensure proper circuit operation and to determine the derivative's sign, which controls the up/down counting behavior. Additionally, this sampled analog signal is compared to an analog conversion of the counter's output. The result of this comparison is sent to a selector (multiplexer), which retains the original signal if the derivative sign is positive or passes the complement if the derivative is negative. This multiplexed comparator enables level-crossing detection, which generates the clock signal for the counter. Finally, the enable logic uses the current counter state and the derivative sign signal to ignore the counter clock signal when the ADC reaches its maximum level with a positive derivative sign or its minimum level with a negative derivative sign. This condition can be expressed as a Boolean equation employing the System Verilog syntax explained in [10]:

$$EN = \sim (\sim |(D_{N-1:0}) \cdot \sim (Slope) + \&(D_{N-1:0}) \cdot Slope) \tag{2}$$

The Boolean equation 2 ensures the system enters a power-saving state during idle signal conditions, crucial for embedded applications requiring low standby power. Where, $D_{N-1:0}$ is the digital output of the counter and the system, and *Slope* is the digital control signal indicating the derivative sign of the input signal. Here, a logical 1 represents a positive slope, and 0 indicates a negative slope. signal

also governs the operation of a power gating module, as detailed in [11], which supplies power to the multiplexed comparator. This power gating mechanism is a crucial design feature aimed at enhancing energy efficiency. By selectively activating the comparator only when the counter is required to count up or down, the system significantly reduces power consumption during idle states. When the input signal reaches its maximum or minimum value, as determined by the counter's digital output and the *Slope* signal, the EN signal disables the counter and the multiplexed comparator entirely. This ensures that no unnecessary power is consumed by components that are not actively contributing to the system's operation.

Now, all the digital and analog components are implemented using CMOS $130nm$ SKYWATER technology. This advancement has enabled the consolidation of the entire ADC system into a single transistor-level module. By integrating all components—including the sample-and-hold circuit, comparator, multiplexer, counter, and power gating module—within the same fabrication process, the design achieves a high level of compactness and efficiency.

4 Results

To implement the complete ADC circuit, the connections among all the developed internal modules adhere to the schematic shown in Figure 2. For a quantitative understanding of the circuit's operation, the proposed topology is compared with the current state-of-the-art ADC architectures, Flash ADC [1] and TT-ADC [2] at circuit-level implementation. Among these, the simplest and most commonly implemented design is the Flash ADC [1]. The two circuits are evaluated under specific design corners, including variations in fabrication process and temperature, as outlined in [11].

Both ADC designs are implemented using the $130nm$ SKYWATER PDK with a 3-bit resolution. This choice simplifies the simulation process, reducing computational complexity while providing signals that are easier to analyze and interpret.

Figure 18 shows the behavioral simulation of the proposed ADC scheme. As it was expected, the circuit level implementation operates similarly as the block-system one, with the difference of voltage disturbances and delay in response. The input signal is between $0[V]$ and $1[V]$ at $12.5[kHz]$, process corner: TT, and $T = 25[^{\circ}C]$, with an ADC sample frequency of $75 \cdot f_{in}$.

Figures 19 and 20 illustrate the behavior of the STT-ADC implemented in $130nm$ technology with ramp and triangular waveforms, respectively. All these tests are under TT conditions @ $T = 25[^{\circ}C]$. The timing diagrams depict both the analog input signal and the corresponding DAC voltage levels. Additionally, the digital output, expressed in hexadecimal format, is presented, aligning with the ADC transfer characteristic shown in Figure 4.

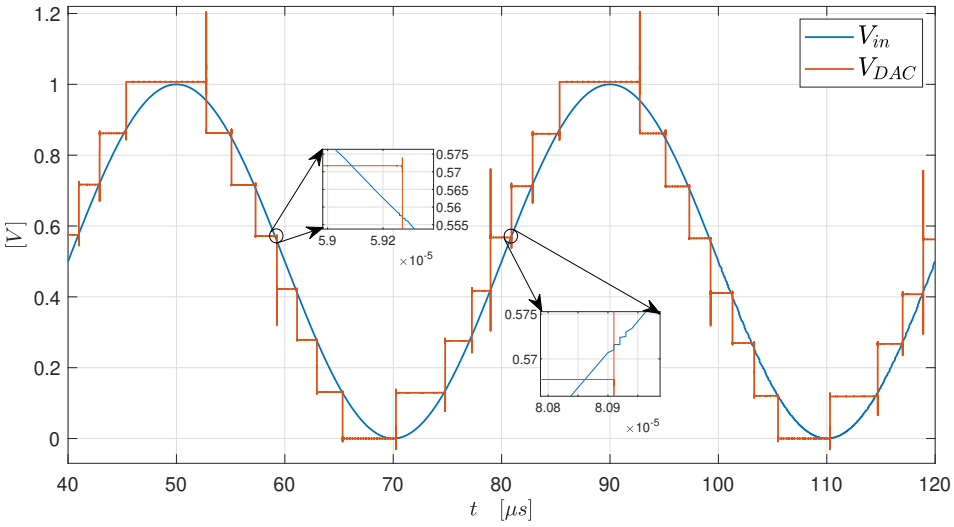


Figure 18: STT-ADC Implemented in 130nm Technology Timing Diagram with Sine Wave-from.

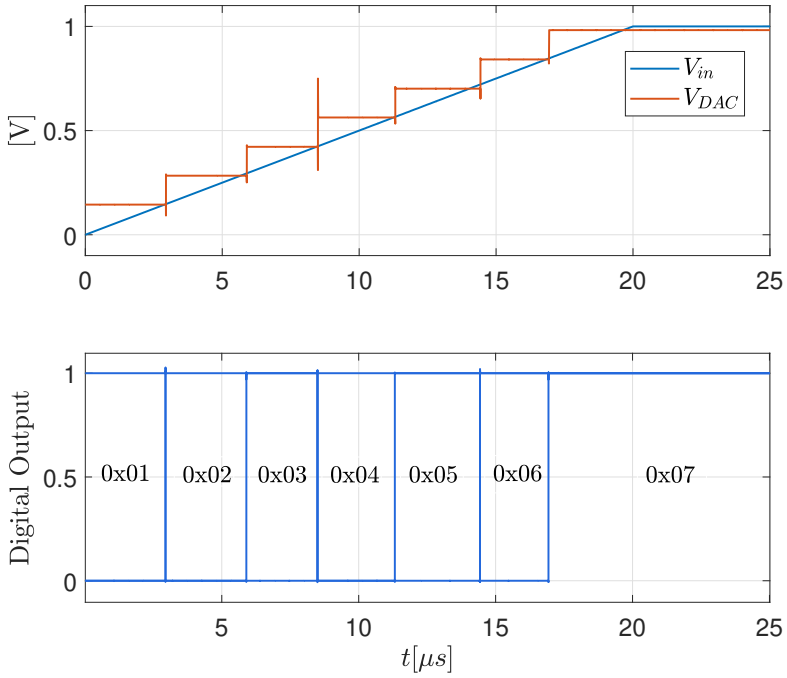


Figure 19: STT-ADC Implemented in 130nm Technology Timing Diagram with Ramp Wave-from.

Figure 21 shows the behavioral simulation of the current state-of-art TT-ADC [2] scheme implemented in 130m technology. As expected, the circuit-level implementation performs comparably to the block-level design, with minor differences caused by voltage disturbances and notable timing delays. The input signal ranges between $0[V]$ and $1[V]$ at a frequency of $12.5[kHz]$, under process corner TT and $T = 25[^{\circ}C]$, with the ADC sampling at a frequency of $75 \cdot f_{in}$.

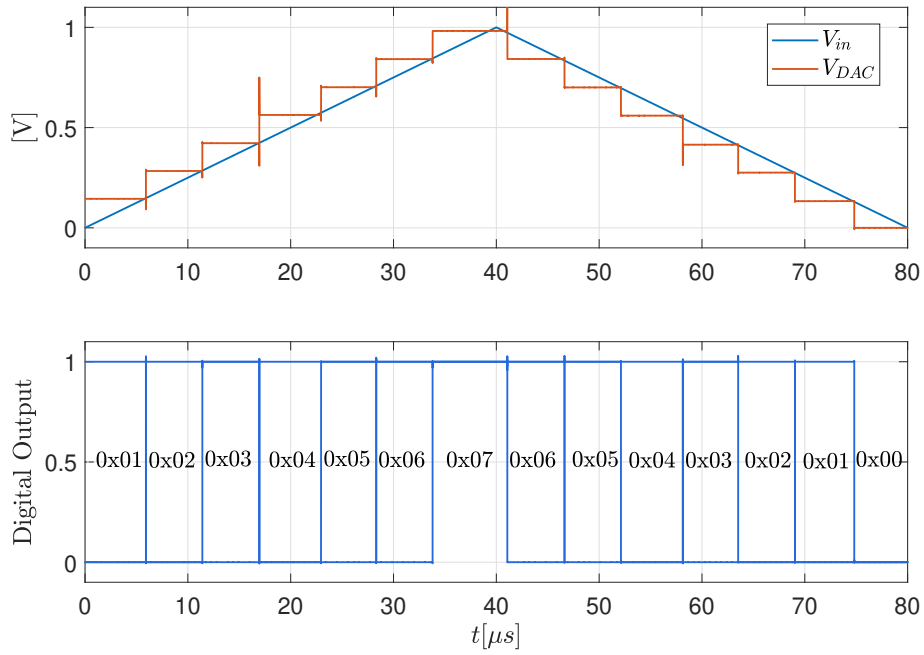


Figure 20: STT-ADC Implemented in 130nm Technology Timing Diagram with Triangle Wave-from.

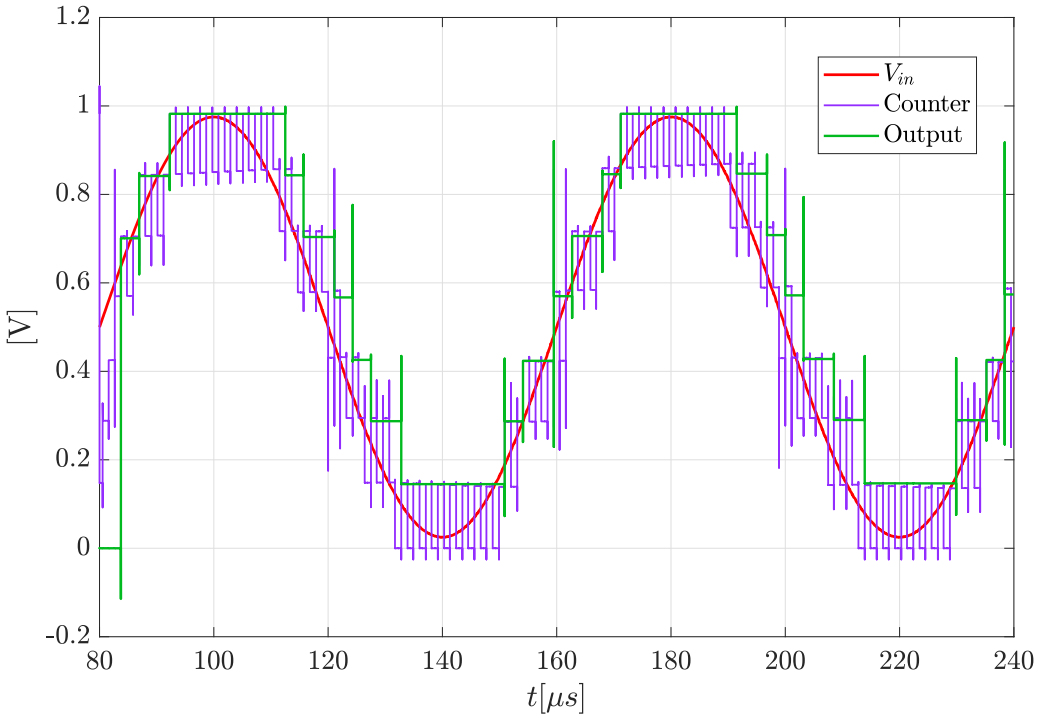


Figure 21: TT-ADC Implemented in 130nm Technology Timing Diagram with Sine Wave-from.

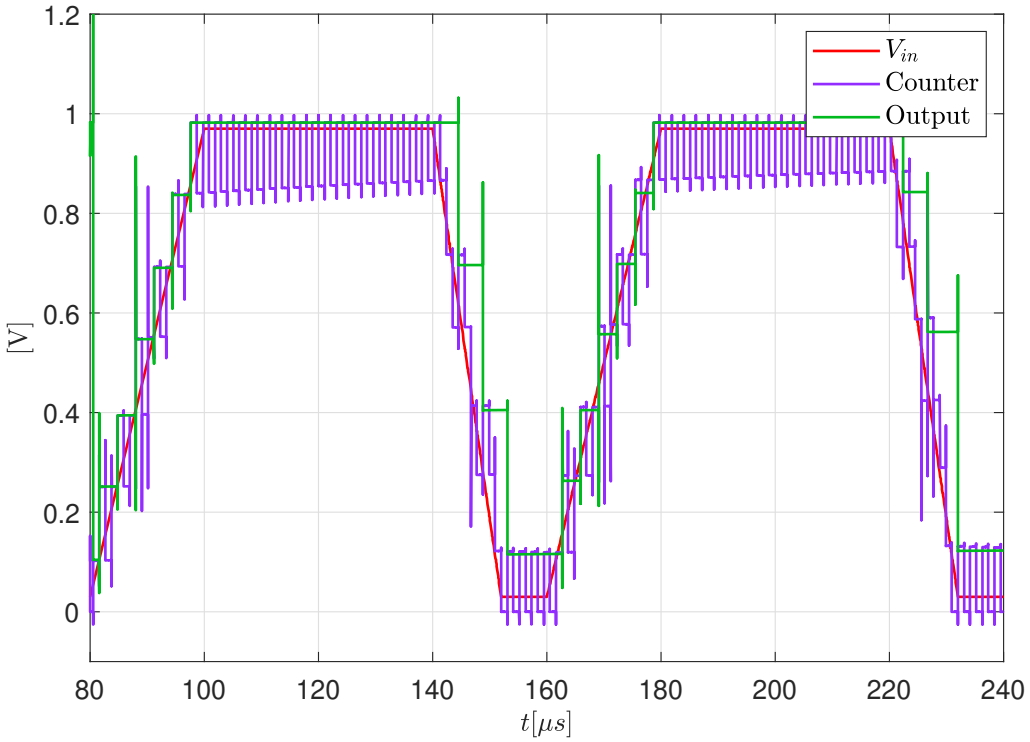


Figure 22: TT-ADC Implemented in 130nm Technology Timing Diagram with Ramp Wave-from.

Figure 22 illustrates the response of the Tracking-Type ADC (TT-ADC) [2] in 130nm CMOS technology when subjected to a ramp input signal ranging from $0[V]$ to $1[V]$. The input frequency is $f_{in} = 12.5[kHz]$, and the sampling frequency is $f_s = 75 \cdot f_{in}$. The figure shows the TT-ADC's sampled digital output alongside the input ramp signal and its corresponding DAC voltage levels. As expected, the TT-ADC exhibits a stepped response, with its digital output incrementing in uniform steps as the input ramp signal increases linearly. Due to its sequential nature, the TT-ADC captures the signal with noticeable delay, particularly at higher input slopes, resulting in minor discrepancies between the input signal and the DAC output. This behavior highlights the TT-ADC's dependence on sampling rate and resolution for accurate tracking of signals with varying slopes.

To ensure a fair comparison between the current state-of-the-art Flash ADC [1], TT-ADC [2], and the proposed STT-ADC, two key metrics will be evaluated: the average total power consumption over one complete cycle of an input sinusoidal signal, and the average propagation delay. The propagation delay is defined as the time interval between a crossing point in the sampled input signal and the corresponding transition in the output digital signals, encompassing both rise and fall times as described in [11].

This average propagation delay, denoted as $t_{p_{cross-out}}$, is calculated by considering all crossing points within the sinusoidal cycle. These metrics provide a comprehensive view of the performance

and efficiency of the proposed STT-ADC relative to the Flash ADC under similar operating conditions.

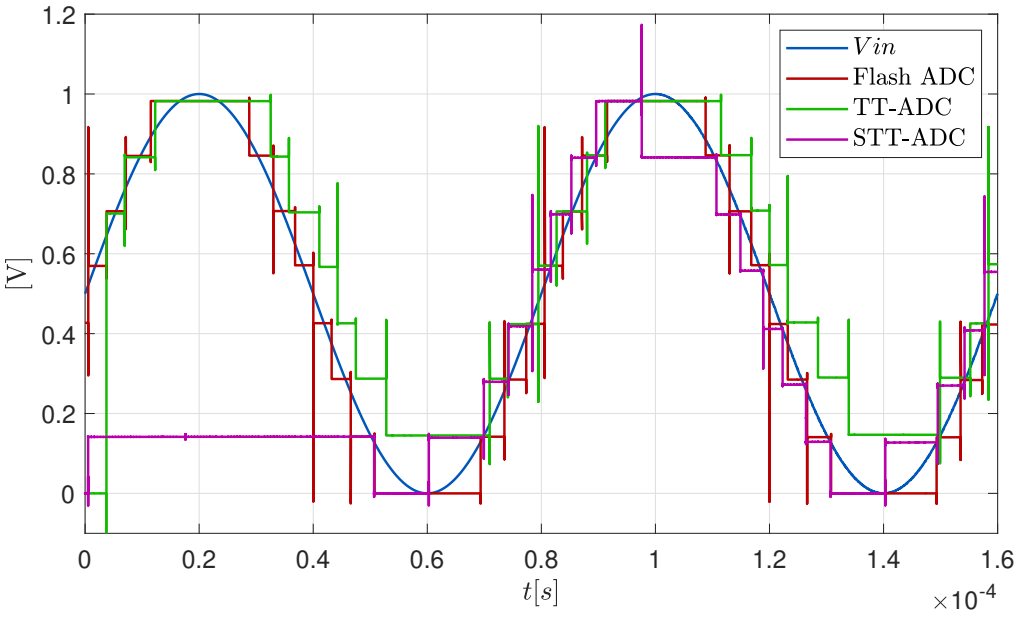


Figure 23: ADC Topologies Comparison at Circuit-Level Implemented in 130nm Technology

Figure 23 presents a comparative analysis of the three ADC topologies—Flash ADC, Tracking-Type ADC (TT-ADC), and the proposed Slope Tracking Type ADC (STT-ADC)—implemented at the circuit level using 130nm CMOS technology. The input signal is a sine wave with a frequency of 12.5$[kHz]$, sampled at a rate of $f_s = 75 \cdot f_{in}$, and the figure illustrates two complete periods of the input waveform. Each ADC's output, represented as a sequence of discrete digital values, is plotted alongside the input signal and the corresponding DAC output levels. The Flash ADC [1] demonstrates the fastest response time with minimal latency but at the cost of higher power consumption. The TT-ADC [2] showcases efficient power usage but introduces significant delay due to its sequential sampling approach. In contrast, the STT-ADC achieves a balance between the two, providing low power consumption and competitive delay performance. This comparison highlights the strengths and trade-offs of each architecture under identical operating conditions.

Tables 2, 3, and 4 present the performance measurements of the proposed STT-ADC compared to the TT-ADC [2] and Flash ADC [1] under various conditions, including typical operation, timing specifications, and power consumption. Under typical operating conditions (Table 2), the STT-ADC achieves a power consumption of 136.25 $[\mu W]$, which is approximately 70% lower than the Flash ADC (458.56 $[\mu W]$) and 32% higher than the TT-ADC (102.93 $[\mu W]$). In terms of delay, the STT-ADC exhibits a minimal increase of 3% compared to the Flash ADC while outperforming the TT-ADC with a 90% reduction in delay.

Converter Type	**Corner: TT @ $T = 25[^{\circ}C]$, $f_{in} = 12.5[kHz]$ (Typical Operation)**		
	f_s	$P[\mu W]$	$t_{p_{cross-out}}[ns]$
Flash-ADC	$75 \cdot f_{in}$	458.56	172.32
TT-ADC	$75 \cdot f_{in}$	102.93	1827.33
STT-ADC	$75 \cdot f_{in}$	136.25	177.66

Table 2: Typical Conditions Measurements

Converter Type	**Corner: SS @ $T = 100[^{\circ}C]$, $f_{in} = 12.5[kHz]$ (Timing Specifications)**	
	f_s	$t_{p_{cross-out}}[ns]$
Flash-ADC	$75 \cdot f_{in}$	189.03
TT-ADC	$75 \cdot f_{in}$	1929.00
STT-ADC	$75 \cdot f_{in}$	224.30

Table 3: Worst-Case Delay Measurements

Converter Type	**Corner: FF @ $T = 100[^{\circ}C]$, $f_{in} = 25[kHz]$ (Power Consumption Specifications)**	
	f_s	$P[\mu W]$
Flash-ADC	$75 \cdot f_{in}$	741.61
TT-ADC	$75 \cdot f_{in}$	200.31
STT-ADC	$75 \cdot f_{in}$	244.50

Table 4: Worst-Case Power Consumption Measurements

For the worst-case timing scenario at process corner SS and $T = 100[^{\circ}C]$ (Table 3), the STT-ADC demonstrates competitive performance, with a measured delay ($t_{p_{cross-out}} = 224.30\,[ns]$) that is 88% faster than the TT-ADC ($1929.00\,[ns]$) and only 18.7% slower than the Flash ADC ($189.03\,[ns]$).

Lastly, under worst-case power conditions at process corner FF and $T = 100[^{\circ}C]$ (Table 4), the STT-ADC consumes $244.50\,[\mu W]$, which is 67% lower than the Flash ADC ($741.61\,[\mu W]$) but 22% higher than the TT-ADC ($200.31\,[\mu W]$). These results highlight the STT-ADC's efficiency and balanced trade-off between power and delay, making it a practical choice for power-sensitive applications requiring improved timing performance.

5 Conclusions

A Slope Tracking Type Analog-to-Digital Converter has been presented. The development process of the module spans from the system-level concept to the implementation of individual components at the transistor level, culminating in the final schematic design using $130nm$ SKYWATER technology [9]. The proposed STT-ADC outperforms the current state-of-the-art Flash ADC [1] in terms of power efficiency, consuming significantly less power under typical and worst-case conditions. When compared to the TT-ADC [2], the STT-ADC achieves enhanced functionality by providing timing information while maintaining competitive power efficiency, albeit with a slightly higher power consumption. In terms of timing specifications, the STT-ADC exhibits a minimal delay of $t_{p_{cross-out}} = 224.30\ [ns]$ under worst-case conditions, which is 88% faster than the TT-ADC ($t_{p_{cross-out}} = 1929.00[ns]$) and only 18.7% slower than the Flash ADC ($t_{p_{cross-out}} = 189.03[ns]$). These results demonstrate that while the TT-ADC achieves minimal power consumption, it does so at the expense of timing precision, whereas the STT-ADC provides a balanced trade-off between power efficiency and timing performance. The potential scalability of the STT-ADC suggests the possibility of achieving higher bit resolution while maintaining reduced power consumption and competitive timing performance.

6 Future Work

Despite demonstrating an outstanding ADC performance, the circuit has certain limitations. Firstly, the input voltage swing must remain between $0[V]$ and $1[V]$ to ensure proper functionality. This constraint necessitates a selected range of analog signals, excluding those with intermediate steady voltage levels or intermediate voltage amplitudes. For audio processing applications, the proposed STT-ADC performs effectively across all its attributes. However, to broaden the range of compatible input waveforms, future work proposes an Enhanced STT-ADC capable of tracking signals independently of their voltage-level crossings. This novel topology incorporates one of the state-of-the-art architectures, the TT-ADC [2], to achieve robust tracking capabilities. Additionally, a refined version of the slope detection module will modify the output digital signals, enabling the entire module to fully support slope-tracking features.

Figure 24 illustrates the schematic of the Enhanced STT-ADC circuit. This system incorporates a controller that determines whether the current value of the TT-ADC should be decremented by 0x1 or remain unchanged. This decision is based on the slope of the input signal and the current output of the TT-ADC module. The purpose of this multiplexed subtraction mechanism is to provide the output with additional information about the signal's current level and its monotonic behavior. For instance, if the input signal is at its minimum value, the TT-ADC detects the next level due to its inherent characteristic of capturing the upper limit of the counter swing.

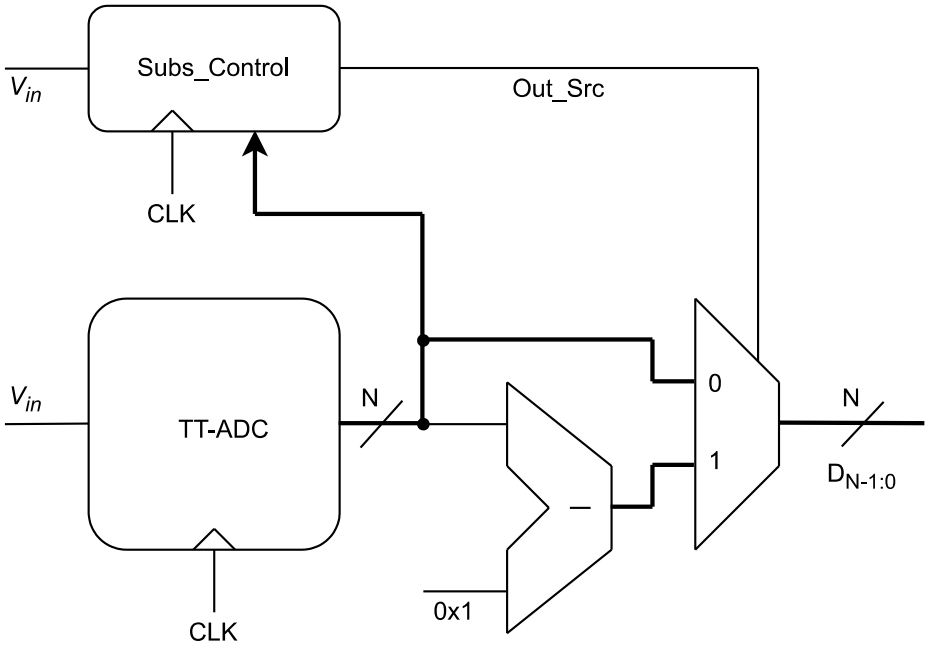


Figure 24: Enhanced STT-ADC Architecture Proposal.

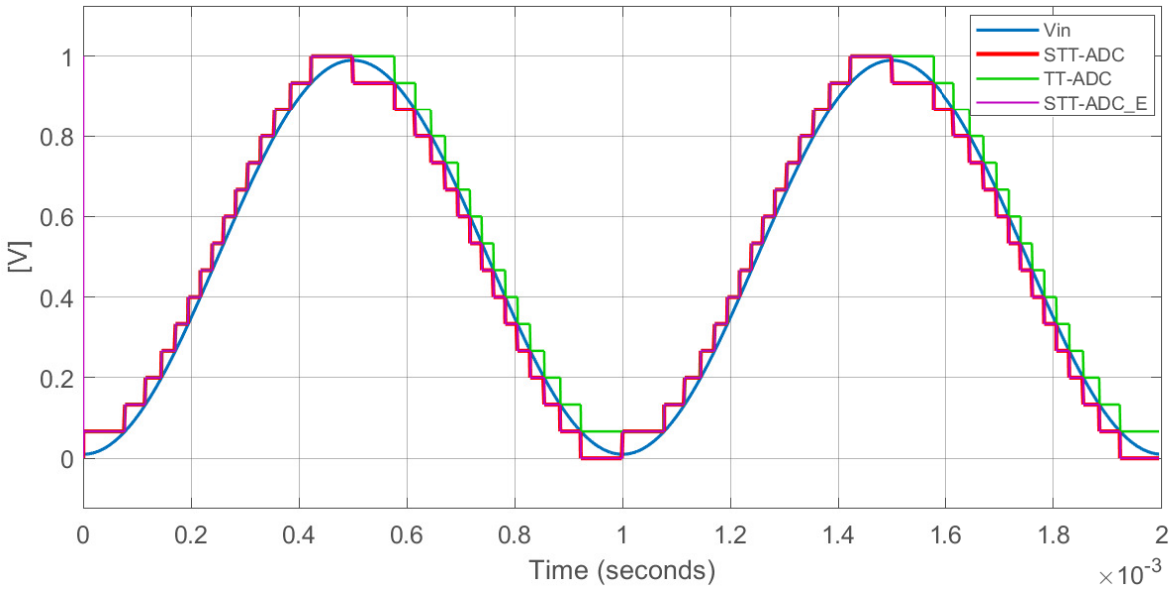


Figure 25: ADC Architectures First Comparison.

Figures 25 and 26 illustrate the system-level behavior of the proposed STT-ADC, the current state-of-the-art TT-ADC [2], and the future work proposal, the Enhanced STT-ADC. The first comparison (Figure 25) demonstrates that the Enhanced STT-ADC performs equivalently to the proposed STT-ADC under standard conditions. However, Figure 26 highlights a limitation: when the input signal does not intersect with the DAC output, the ADC is unable to track the signal unless the voltage swing remains within the specified range.

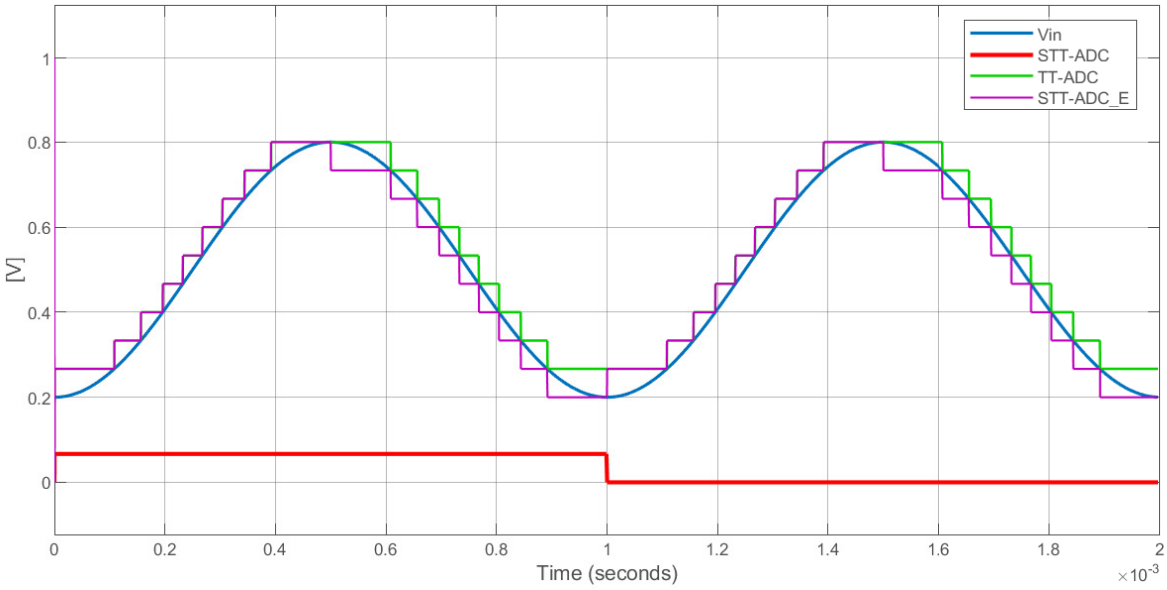


Figure 26: ADC Architectures Second Comparison.

The Enhanced STT-ADC addresses these limitations by offering more sophisticated capturing and quantization of the input signal, along with refined tracking methods. Future work will explore circuit-level implementations, hybrid analog-digital scaling to achieve higher resolutions without compromising delay or power efficiency. Moreover, layout design validation and analysis of fabrication-specific variations will ensure the architecture's robustness for real-world applications.

Acknowledgments

We extend our gratitude to Synopsys Chile for the invaluable support provided to USFQ in the use of their entire platform of design and simulation tools. Their support has been crucial for the development of our research and academic projects. Synopsys Chile's support and commitment fostering innovation in scientific research are truly appreciated.

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