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Process Variation Sensing and Compensation Employing a Ring Oscillator-Based Architecture in SkyWater 130nm Technology.

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RESUMEN

Este proyecto de titulación presenta el diseño de un Compensador de Variación de Proceso, cuyo objetivo es mejorar el rendimiento de los circuitos integrados mitigando los efectos causados por las variaciones en el proceso de fabricación. Para lograrlo, se implementa un sensor de variación de proceso, compuesto por un Oscilador de Anillo, un Conversor de Frecuencia a Digital (FDC) y un Comparador Digital para cada uno de los principales extremos del proceso de fabricación. Mediante el uso de este sensor, se detectan las variaciones de proceso y se compensan en un circuito subsecuente. Además, se incluye un generador de rampa (circuito subsequente) en el diseño para probar y validar la funcionalidad del compensador.

***Palabras clave*:** Compensador de Variación de Procesos, Oscilador de Anillo, Conversor de Frecuencia a Digital, Comparador Digital, Generador de Rampa.

ABSTRACT

This thesis project presents the design of a Process Variation Compensator, aimed at enhancing the performance of integrated circuits (IC) by mitigating the effects of manufacturing process variations. To accomplish this, a process variation sensor is implemented, consisting of a Ring Oscillator, a Frequency-to-Digital Converter (FDC), and a Binary Comparator for each main process corner. Through the use of this sensor, process variations are detected and compensated in the subsequent circuit. A Ramp Generator is included in the design to test and validate the functionality of the compensator.

***Keywords*:** Process Variation Compensator, Ring Oscillator, Frequency-to-Digital Converter, Binary Comparator, Ramp Generator.

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DEDICATORIA

Dedicamos este trabajo a nuestras familias, quienes han sido nuestro mayor apoyo durante toda la etapa universitaria. Gracias por acompañarnos con paciencia, por alentarnos en los momentos difíciles y por creer en nosotros incluso cuando dudábamos. También queremos dedicar este logro a quienes fuimos al empezar esta carrera. A esas versiones de nosotros que, a pesar de las dudas y obstáculos, decidieron seguir adelante. Este proyecto representa el esfuerzo, la constancia y todo el aprendizaje acumulado a lo largo del camino.

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1 Introduction

As semiconductor technologies advance to the nanometer scale, process variations caused by fluctuations in manufacturing, voltage, and temperature become increasingly impactful, posing major challenges to integrated circuit (IC) performance and reliability [1, 2]. These variations can alter key parameters such as operating frequency and power consumption, often compromising functionality [3, 4]. The proposed topology incorporates a compensation mechanism that is evaluated under the five main process corners: Slow-Slow (SS), Slow-Fast (SF), Typical-Typical (TT), Fast-Slow (FS), and Fast-Fast (FF), which represent different combinations of NMOS and PMOS performance characteristics [5]. Among these, SS represents the slowest transistor behavior, FF corresponds to the fastest transistor behavior and thus the highest circuit speed, and TT represents the nominal case, reflecting standard transistor dimensions and typical operating conditions. Given their high sensitivity to such changes, ring oscillators are well-suited for detecting and compensating process-related deviations [6].

Traditional mitigation strategies involve post-fabrication calibrations, which are costly and do not address fluctuations during operation [7–9]. For this reason, more adaptive and integrated solutions are needed to maintain system performance under varying conditions [10].

This article presents a novel architecture targeting process variation corners, combining a ring oscillator, a Frequency to Digital Converter (FDC), and a binary comparator into a compensator system that detects and corrects deviations in real time [3,6]. To validate this module, an analog ramp generator is implemented, it operates under any process variation corner, allowing validation of the compensator's response to controlled variations [11–13]. This approach provides two main advantages: improved IC yield by reducing rejections due to process inconsistencies—thereby minimizing electronic waste [14, 15]—and reduced reliance on overdesign, promoting more efficient use of resources and energy [10]. Together, these benefits contribute to a more sustainable and cost-effective IC production flow.

To demonstrate the effectiveness of the proposed solution, this article is structured as follows. Section II describes the compensation system architecture and its key modules. Section III details the circuit-level and layout implementation. Section IV presents experimental validation under various process scenarios, followed by a discussion in Section V. Section VI concludes by summarizing the main contributions and implications for future IC design.

2 Proposed Architecture

The proposed architecture for the process variation compensator enables real-time monitoring by combining analog sensing with digital processing. It incorporates a ring oscillator, an FDC, and a binary comparator to detect deviations caused by process variations. Based on predefined referenced values for different process corners, the system applies corrective logic to maintain performance consistency across varying conditions [5].

As shown in Figure 1, the comparator—depicted in Figure 1—utilizes a subtraction-based structure along with basic logic gates (AND, OR, NOT) to determine whether the measured response aligns with one of the standard process corners (SS, SF, TT, FS, FF). It then generates the necessary control signals to ensure the circuit operates reliably and within the intended specifications.

2.1 Ring Oscillator

The ring oscillator in this architecture is designed to detect process variations by generating a frequency that reflects changes in propagation delay caused by manufacturing conditions [6, 16]. As shown in Figure 2, the oscillator consists of three key components: a current source, eleven starved

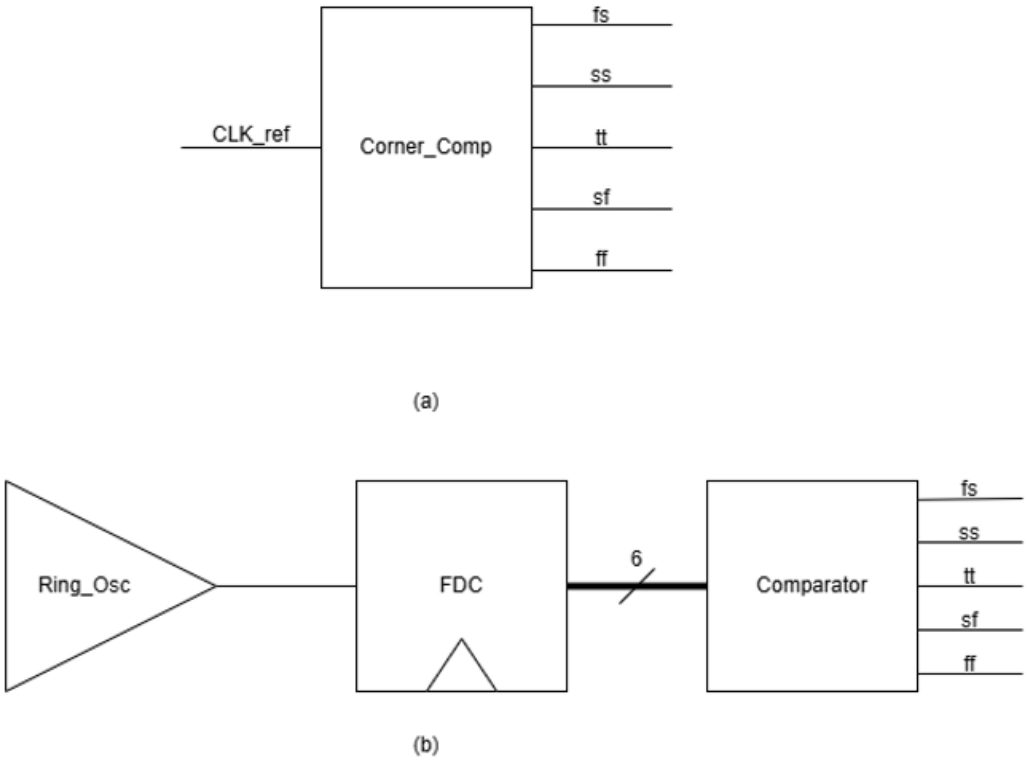

Figure 1: (a) Corner Compensator and Ramp Generator, which produces $V_{\text{ramp\_gen}}$ based on process corners. (b) Internal blocks of the Corner Compensator: Ring Oscillator, FDC, and Comparator.

inverters, and two registers.

The oscillator is powered by a current source, which provides a controlled bias rather than a fixed voltage supply. This improves oscillation stability and increases the circuit's sensitivity to process-induced variations [17, 18]. At the core are eleven strangled inverters—standard CMOS inverters with reduced transistor sizing (typically the NMOS)—which intentionally introduce additional delay to enhance sensitivity [6, 19]. Using an odd number of inverters ensures sustained oscillation.

The output is then passed through two D flip-flop registers, which capture the signal synchronously and convert it into digital form for further

processing by the FDC [19]. This configuration enables the ring oscillator to serve as a highly effective sensor for detecting process variation across different corners.

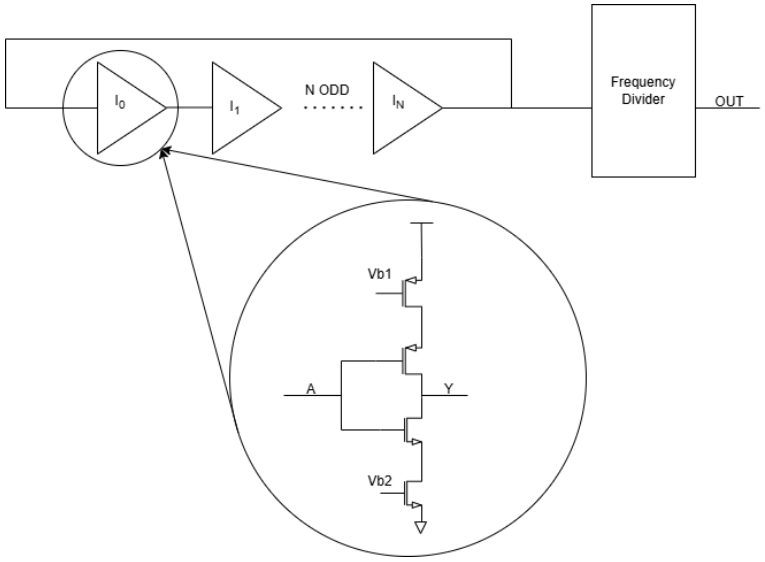

Figure 2: Block Diagram of the Ring Oscillator Used on the Compensator

2.2 Frequency to Digital Converter (FDC)

The Frequency-to-Digital Converter (FDC) is responsible for converting an input frequency signal into a corresponding digital value, using a reference clock as a baseline. In this project, the output of the FDC is defined as the ratio between the input frequency (f_{in}) and the reference frequency (f_{ref}), following the approach presented in [20] and illustrated in Figure 3. A reference frequency of 1.2 MHz was used for this design, and the input frequency is the output of the ring oscillator.

$$f_{\text{MAX}} < (2^{N_{\text{cnt}}} - 1) f_{\text{REF}} \tag{1}$$

Based on the frequency range of the proposed ring oscillator, a 6-bit FDC was selected to ensure sufficient resolution and accuracy in the conversion process.

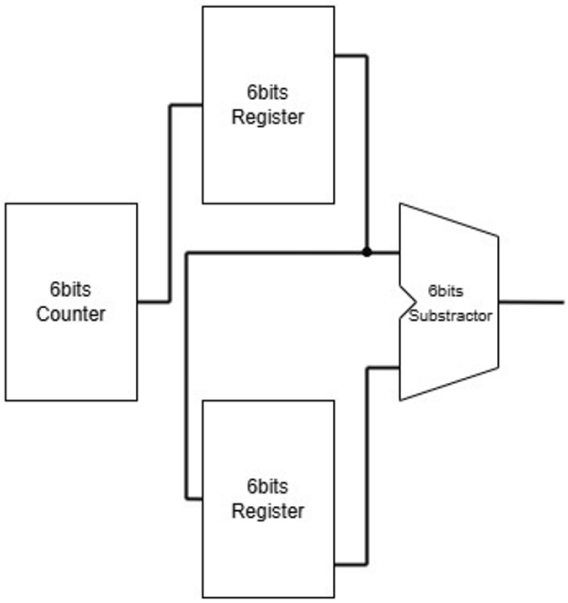

Figure 3: Block Diagram of the FDC.

2.3 Binary Comparator

The binary comparator consists of combinational logic that evaluates the output of the FDC against predefined threshold values. Based on the result of this comparison, specific components within the system are selectively activated or deactivated to meet the operational requirements.

As shown in Table 1, the ring oscillator generates output frequencies that vary across different fabrication process corners. Consequently, the corresponding digital output ranges of the FDC for each corner are summarized

in Table 2.

Accordingly, each threshold value used by the binary comparator is defined as the upper limit of the corresponding FDC output range for each process corner.

Table 1: Frequencies Provided By Ring Oscillator Across Process Corners

Process Corner	**Frequency (MHz)**
Corner fs	6.45 MHz
Corner ss	9.74 MHz
Corner tt	23.66 MHz
Corner sf	43.95 MHz
Corner ff	45.89 MHz

Table 2: Control Signal Mapping Based on FDC Output

Output FDC	**fs**	**ss**	**tt**	**sf**	**ff**
0–6	1	0	0	0	0
7–9	0	1	0	0	0
10–20	0	0	1	0	0
21–38	0	0	0	1	0
39–63	0	0	0	0	1

3 Circuit-Level and Layout Implementation

The digital logic circuit was implemented at the full-custom level using the SKYWATER 130 nm Process Design Kit (PDK), and standard cell libraries provided by the manufacturer were employed. To verify the cor-

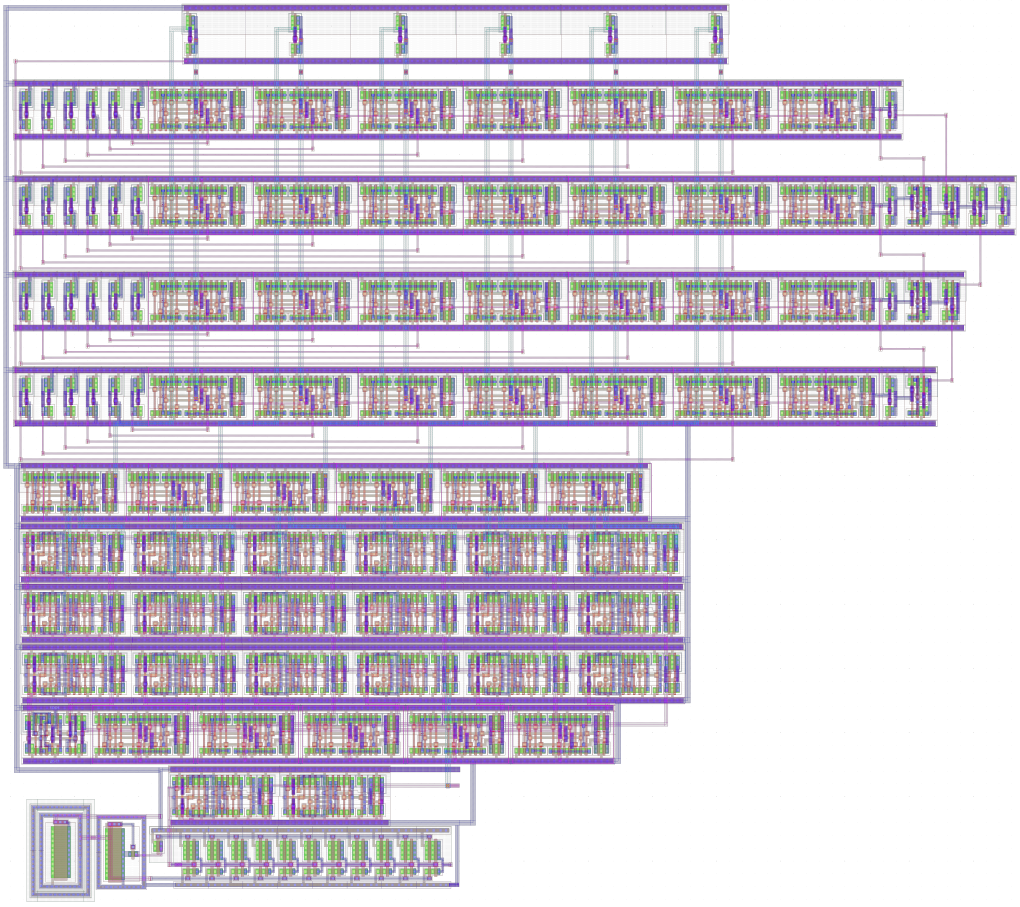

Figure 4: Process Variation Compensator Layout implementation in SKYWATER 130nm PDK.

rectness of the layout design, standard verification tools were employed, including Design Rule Check (DRC), Layout Versus Schematic (LVS), and Layout Parasitic Extraction (LPE), as provided by the SkyWater 130 nm PDK.

4 Experimental Validation and Results

As shown in Figure 5 in The architecture is divided into two main blocks: the Ramp Generator, which produces a time-based signal for controlled testing, and the Corner Compensator, which evaluates the digital output from the FDC.

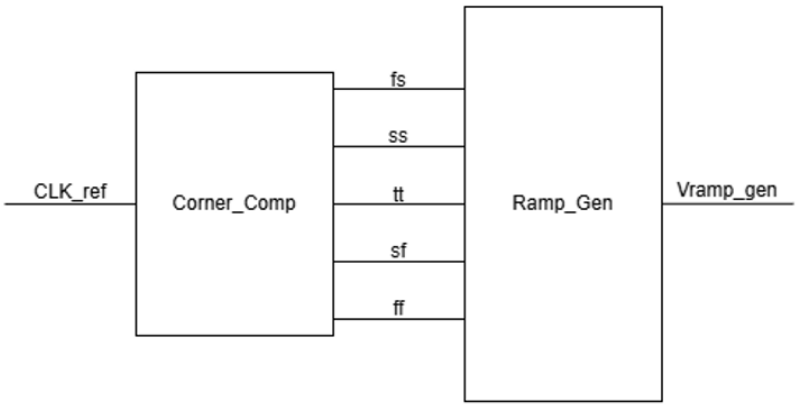

Figure 5: (a) Corner Compensator and Ramp Generator, which produces $V_{\text{ramp\_gen}}$ based on process corners. (b) Internal blocks of the Corner Compensator: Ring Oscillator, FDC, and Comparator.

The waveform results shown in Figure 6 confirm the expected oscillatory behavior of the ring oscillator across multiple process corners. As presented in Table 1, the output frequency of the oscillator varies significantly depending on the specific corner. This variation is primarily attributed to the sensitivity of transistor delay to process and voltage fluctuations. Despite these variations, the circuit consistently exhibits stable oscillation across all evaluated corners, thereby validating the robustness and reliability of the proposed design under different manufacturing conditions.

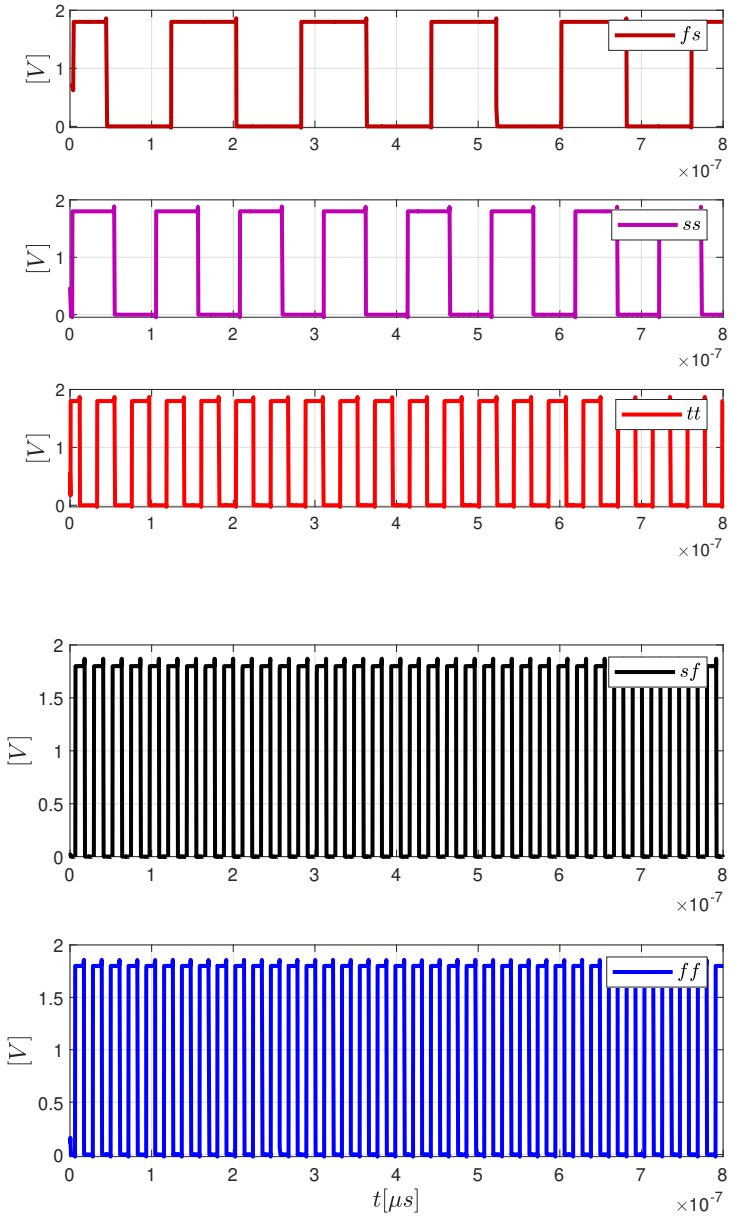

Figure 6: Post-Layout Ring Oscillator Simulation Results.

Table 3: Ring Oscillator Frequency and FDC Output

Process Corner	**Frequency (MHz)**	**FDC Output (Digital Value)**
Corner fs	6.45 MHz	0-6
Corner ss	9.74 MHz	7-9
Corner tt	23.66 MHz	10-20
Corner sf	43.95 MHz	21-38
Corner ff	45.89 MHz	39-63

The post-layout simulation results show in Table 3 confirm that the digital output of the FDC responds as expected to variations in the input

frequency. Furthermore, the system exhibits robust functionality across all evaluated process corners, with the FDC accurately tracking frequency changes and maintaining consistent performance. These findings validate the reliability of the design and its suitability for integration into frequency-sensing digital systems, even under process-induced variability. The post-layout simulation results of the binary comparator, illustrated in Figure 7, demonstrate correct and reliable operation under extracted layout conditions. The comparator accurately detects whether the output of the Frequency-to-Digital Converter (FDC) falls within the valid frequency range defined for each process corner. When the measured frequency corresponds to the expected range, the comparator enables the output; otherwise, it remains inactive.

The post-layout simulation results of the ramp generator, illustrated in Figure 8, demonstrate the effective performance of the proposed compensator across all evaluated process corners. The waveform $V_{\text{ramp-gen}}$ adjusts dynamically based on the output of the binary comparator, which activates the appropriate current source corresponding to the detected process corner. Each corner configuration (FS, SS, TT, SF, FF) produces a distinct ramp profile, verifying that the system correctly interprets the frequency ratio from the Frequency-to-Digital Converter (FDC) and enables the appropriate path.

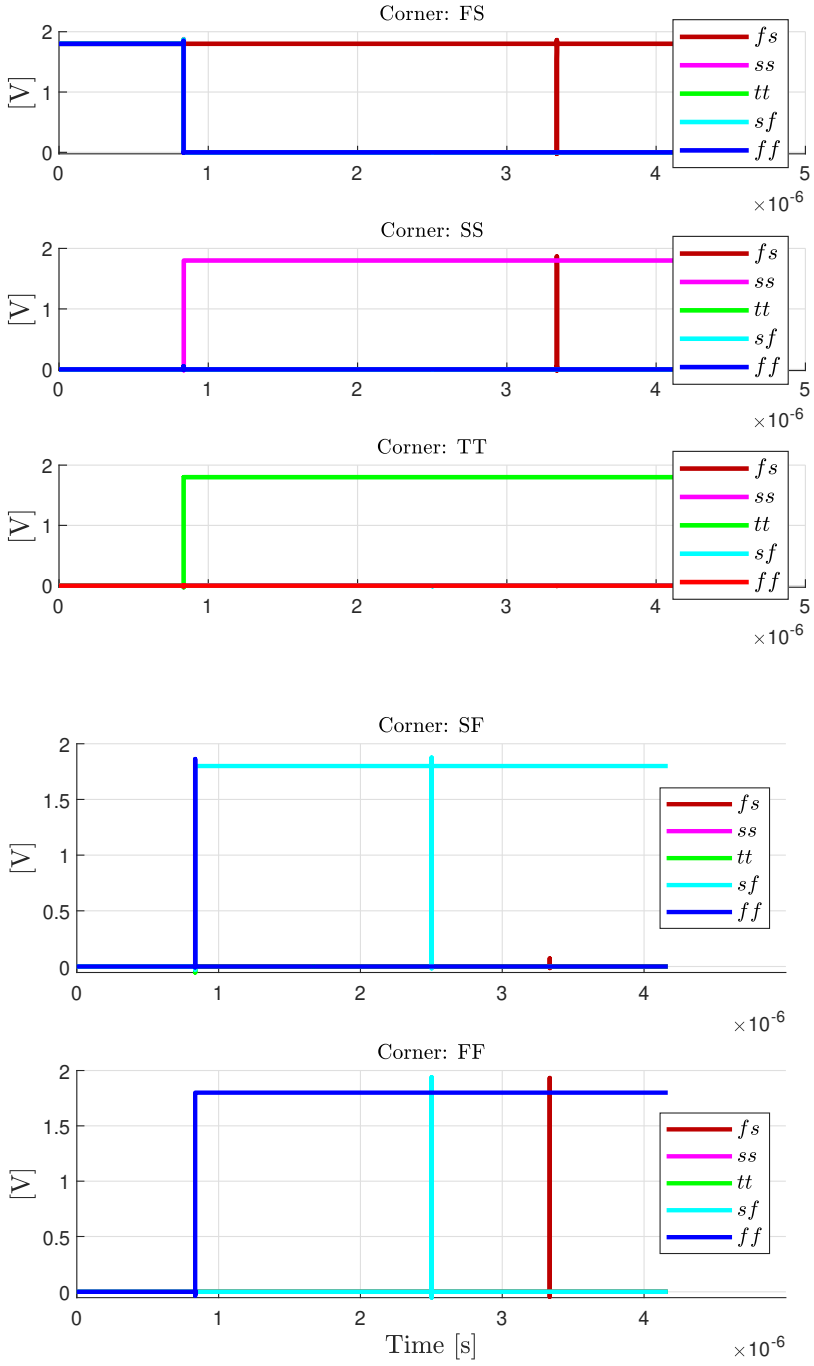

Figure 7: Post-Layout Binary Comparator Simulation Results.

5 Conclusion

This article presented the design and validation of a Process Variation Compensator implemented using the SkyWater 130 nm PDK. The archi-

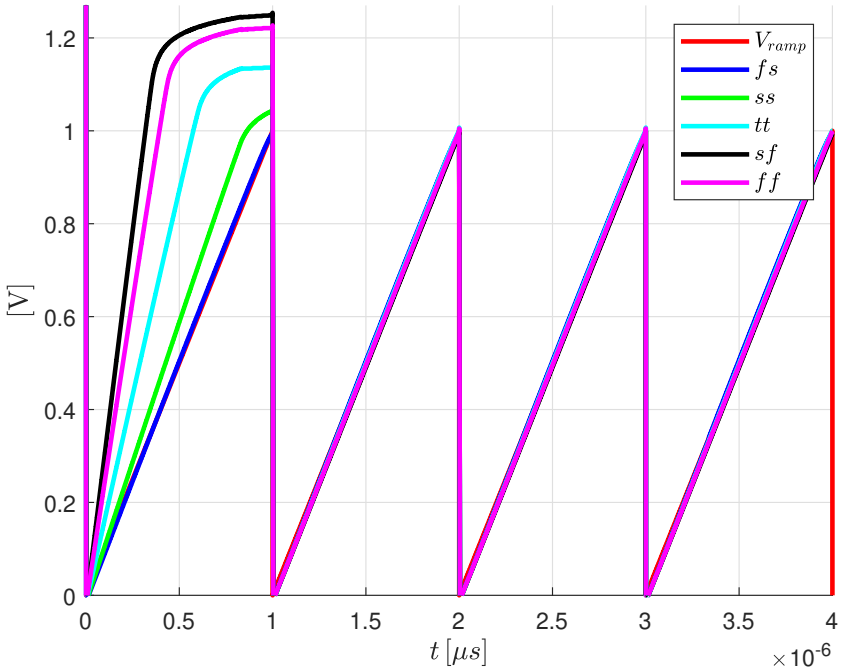

Figure 8: Post-Layout Compensator applied in Ramp Generator Simulation Results.

tecture consists of a ring oscillator, an FDC, and a digital comparator, enabling real-time detection and classification of process variation corners based on frequency response.

Post-layout simulations confirmed the expected behavior across the main process corners. The ring oscillator produced distinct output frequencies for each variation, which were digitized by the FDC. The digital comparator then correctly identified the process condition and generated the appropriate control signals. A ramp generator was also used to validate the system's effectiveness under dynamic testing conditions.

Although the design effectively compensates for process variations, it does not yet account for temperature-induced changes. Addressing these effects

remains part of our future work to further improve the adaptability and robustness of the system. Overall, the compensator demonstrated stable and reliable performance, showing strong potential for integration into variation-aware and adaptive IC designs.

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