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Design of a Dynamic Comparator with Self-adjustable Offset in CMOS 65nm

Tesis en torno a una hipótesis o problema de investigación y su contrastación

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Design of a Dynamic Comparator with Self-adjustable Offset in CMOS 65nm

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RESUMEN

Este trabajo presenta el análisis y diseño de un comparador dinámico enfocado en la reducción del voltaje de offset. El comparador de dos etapas utiliza un amplificador inversor flotante en la primera etapa para minimizar la sensibilidad a las variaciones del voltaje de modo común de entrada (i-Vcm). Las simulaciones mostraron un voltaje de offset de 3.18 mV y un nivel promedio de ruido de 699.80 µV en diferentes valores de i-Vcm. Los análisis de energía y retardo revelaron trade-offs bajo variaciones de temperatura, voltaje de alimentación y esquinas de proceso. Las mediciones de los chips fabricados confirmaron cambios mínimos en los valores de offset y ruido con la variación de i-Vcm, demostrando baja sensibilidad. Debido a desajustes de fabricación, el voltaje de offset varió de -5.63 a 6.78 mV en 15 chips.

Se evaluaron una técnica de reducción de carga capacitiva y un método de calibración junto con otras dos técnicas: inyección de corriente mediante gate bias y a través de transistores en paralelo. Todas las técnicas se probaron bajo condiciones idénticas, centrándose en la precisión de salida, tiempo de calibración, consumo de energía, retardo e impacto en el área. El método de calibración propuesto mejoró el rendimiento de todas las técnicas, aunque con tiempos de calibración más largos. La técnica de carga capacitiva obtuvo los mejores resultados, logrando un offset de 1-sigma de 0.223 mV con el método de calibración propuesto.

Estos resultados confirman la efectividad de la técnica de reducción del voltaje de offset para mejorar la precisión y confiabilidad del comparador dinámico. Trabajos futuros podrían enfocarse en minimizar el ruido, optimizar el consumo de energía y reducir el retardo para mejorar la eficiencia general.

Palabras clave: Comparador dinámico, voltaje de offset, calibración, diseño CMOS, eficiencia energética.

ABSTRACT

This work presents the analysis and design of a dynamic comparator focused on offset voltage reduction. The two-stage comparator employs a floating inverter amplifier in the first stage to minimize sensitivity to input common-mode voltage (i-Vcm) variations. Simulations showed an offset voltage of 3.18 mV and an average noise level of 699.80 µV across different i-Vcm values. Energy and delay analyses revealed trade-offs under temperature, supply voltage, and process corner variations. Measurements from fabricated chips confirmed minimal changes in offset and noise values with varying i-Vcm, demonstrating low sensitivity. Due to manufacturing mismatches, offset voltage ranged from -5.63 to 6.78 mV across 15 chips.

A capacitive load reduction technique and calibration method were evaluated alongside two other techniques: current injection by gate biasing and through parallel transistors. All techniques were tested under identical conditions, focusing on output accuracy, calibration time, energy, delay, and area. The proposed calibration method improved performance for all techniques, although with longer calibration times. The capacitive load technique achieved the best results, with a 1-sigma offset of 0.223 mV using the proposed calibration.

These results confirm the effectiveness of the offset reduction technique in improving comparator accuracy and reliability. Future work could focus on further minimizing noise, optimizing energy use, and reducing delay for enhanced efficiency.

Key words: Dynamic comparator, offset voltage, calibration, CMOS design, energy efficiency.

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INTRODUCTION

Motivation

Comparators are essential building blocks in many electronic systems due to their ability to detect voltage differences and produce a digital output based on this difference. They are especially valuable in applications requiring quick decision-making, such as analog-to-digital converters (ADCs) (Hershberg, et al., 2021), where their fast response directly impacts overall system performance. ADCs rely on comparators to reduce the time needed to analyze signals by using the high-speed processing capabilities of the digital domain (Goll & Zimmermann, 2015).

These are widely used in technologies such as Ultra-Wideband (UWB) (Hung, Chang, & Lee, 2017), where they decode received signals before further processing in Digital Signal Processing (DSP) circuits. They also play an important role in Software-Defined Radio (SDR) (Sakr, Hussein, Fahmy, & Abdelghany, 2020), allowing ADCs and DACs (digital-to-analog converters) to be placed closer to the antenna, making system reconfiguration easier and more efficient. In these systems, the circuit compares an input signal (voltage, current, or charge) with a reference signal and outputs a digital logic state that indicates if the input is greater or smaller than the reference (Goll & Zimmermann, 2015).

In IoT sensors and wearable devices, as discussed in (Renteria-Pinon, Tang, & Tang, 2023), circuits select sampling points for real-time quantization. The processor predicts an upper and lower threshold for each sampling point, and a comparator checks if the input signal falls within these thresholds to determine if the prediction was accurate. This highlights the useful role of comparators in real-time signal processing.

Another application of dynamic comparators can be found in the design of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) for implantable biosensors

(Zhao, Li, Zhang, Liu, & Zhu, 2022; Shifman & Shor, 2024). In the design shown in (Zhao, Li, Zhang, Liu, & Zhu, 2022), a dynamic comparator with low offset and low kickback noise was used. The complete SAR ADC system includes two identical binary-weighted capacitive DACs, the dynamic comparator, SAR logic, a clock generator, and sampling switches. The low-offset comparator detects the differential voltage on the top plates of the capacitive DAC (CDAC) and sends the comparison results to the SAR logic block, enabling precise and efficient signal conversion.

In neuromorphic computing (Kim, et al., 2023; Rafiq, Chatterjee, Kumar, Singh Chauhan, & Sahay, 2024; Qi, y otros, 2023), where the circuit mimicks brain functions trying to reach a low-power consumption. One way to reduce power and area usage is by replacing high-precision ADCs, used in a previous neuromorphic circuit architecture, with a 1-bit dynamic comparator. In Spiking Neural Networks (SNNs), a type of neuromorphic network that models the behavior of biological neurons, output spikes (signals representing the firing of a neuron) are generated through a simple comparison between the neuron's membrane potential (represents the current state of the neuron) and a threshold, when this potential exceeds this threshold, the neuron fires and generates an output spike. Instead of using ADCs to detect this threshold crossing, dynamic comparators are employed resulting in lower power consumption and reduced area requirements (Kim, et al., 2023).

Some of the key factors to consider when designing CMOS dynamic comparators are ensuring an output accuracy, the ability to operate at low voltages, high speed, low power consumption, reliability, and minimal offset voltage (Sangeetha, et al., 2019).

Overview of comparators

There are various types of comparators, each suited for different applications. Latched comparators, for example, exploit positive feedback to maintain an input-based decision once the comparator is triggered, ensuring stability in the output. Continuous comparators, on the other hand, constantly track the input signals, adjusting the output.

For high-speed applications, dynamic (or clock-regenerative) comparators are commonly used due to their rapid decision-making enabled by positive feedback. These comparators operate in two clocked phases: a precharge phase during the first clock half-cycle, which set specific nodes to either logic '0' or '1' depending on the latch desing, and an evaluation phase that takes place during the second half-cycle, where the decision is made based on the input voltage difference. This dual-phase operation ensures that the comparator is ready to perform a decision on each clock cycle, making it ideal for high-speed signal processing (Goll & Zimmermann, 2015).

Structurally, dynamic comparators feature two main blocks: a differential input pair, which converts the input voltage difference into currents and can provide voltage gain, and a positive feedback latch to drive the final decision (Razavi, 2015). **Figure 1** shows the StrongARM Latch: during the precharge phase (CLK low), nodes A, B, C, and D are precharged to VDD. When CLK goes high, the differential input pair (VinP and VinN) generates a current proportional to the differential input voltage, providing an initial amplification as the voltage difference $V_A - V_B$ will grow exceeding the VinP - VinN. As nodes A and B discharge, NMOS transistors of the latch start to open the channel, allowing current flow at nodes C and D. This process triggers the PMOS transistors, creating the positive feedback that drives the final decision, forcing one output to Vdd and the other to zero (Razavi, 2015).

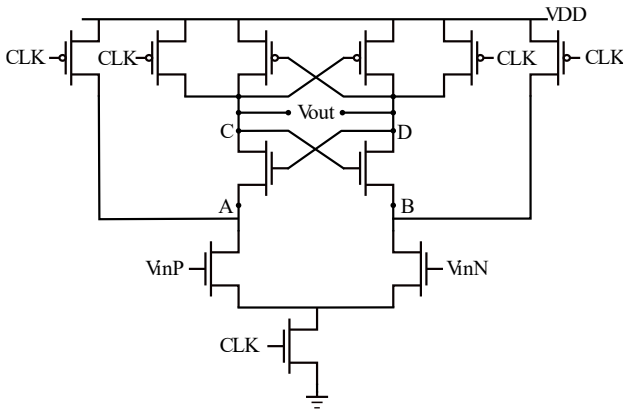


Figure 1: StrongARM Latch (Razavi, 2015)

In addition to the two main blocks, other critical component in dynamic comparators like the strong-arm latch are MOS switches responsible of pre-charging certain circuit nodes—critical for overall performance, either to VDD or GND depending on the design. Although a single NMOS or PMOS can generally handle this role, their on-resistance tends to vary significantly with input voltage. To address this issue, some designs use an NMOS and a PMOS connected in parallel, allowing the circuit to operate effectively across the entire voltage range while maintaining relatively low on-resistance.

Some key characteristics of a comparator are noise and offset. Noise introduces uncertainty in decision-making, with an increasing impact as the input voltage difference becomes close to zero. There are many types of noise sources, including supply voltage, ground noise, thermal noise, and kickback noise, that occurs during fast transitions at the output nodes, often due to positive feedback in the decision phase or resetting the output to a defined voltage.

Offset voltage is the differential input voltage required for switching from positive to negative or vice versa, the ideal offset voltage should be zero. However, this switching point may shift, resulting in a non-zero offset, caused by transistor mismatch at the fabrication process that yields variations of threshold voltage V_{th}, temperature gradients, or asymmetries in the design.

This effect can be minimized with a symmetrical layout and strategic circuit placement to reduce temperature effects from nearby circuitry (Goll & Zimmermann, 2015).

Additionally, noise and offset effects often interact in a comparator leading to incorrect decisions when the input signal is close to the offset voltage, as the noise may change the output in the wrong direction.

Designing and improving dynamic comparators has become essential as technology scales down, particularly due to their zero static power consumption (Krishna & Nambath, 2023). Key improvements focus on making comparators less sensitive to common-mode variation, as disturbances in real-world environments can shift the input levels and reduce decision accuracy. In (Tang, et al., 2020; Canal, Klimach, Bampi, & Balen, 2021), a floating inverter amplifier is used as the first stage, isolated with a floating reservoir capacitor to create virtual supply and ground rails. This design maintains a fixed common-mode voltage at the amplifier output, independent of the input common-mode, enhancing robustness against such variations.

Another key area of improvement is achieving high resolution in detecting small input voltage differences while minimizing delay. In (Krishna & Nambath, 2023), the comparator delay is reduced by using a cascode cross-coupled pair in the preamplifier, which increases gain by enhancing the output impedance through additional transistors. This approach improves delay across the input range, especially for small input differences and higher common-mode voltages, making it ideal for high-speed, high-resolution ADCs.

Reducing power consumption is also critical. In (Canal, Klimach, Bampi, & Balen, 2021), a comparator is designed to operate at low supply voltages by using a positive feedback bulk structure in the floating amplifier of the first stage. This structure reduces the threshold voltage dynamically, increasing transconductance and allowing higher gain and full operation

even with a reduced Vdd. This enables the comparator to operate with lower power consumption, ideal for high-performance and low-power applications.

Lastly, speed improvement is achieved in (Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020) by adding parallel discharge paths at the output, accelerating the discharge rate. This approach reduces delay by approximately 50\% compared to a conventional Strong-Arm Latch comparator, enhancing speed without significant power consumption.

Table 1 provides a quantitative comparison of these techniques. Works (Krishna & Nambath, 2023) and (Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020) show significantly lower delays (0.047ns and 0.167ns): However, (Krishna & Nambath, 2023) has a drawback with a higher offset voltage (11.38 mV) and noise (750 μV), which can affect precision, while (Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020) shows a lower offset, indicating its advantage in high-accuracy applications.

	(Tang, et al., 2020)	(Krishna & Nambath, 2023)	(Canal, Klimach, Bampi, & Balen, 2021)	(Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020)
Process [nm]	180	65	28	65
Supply voltage [V]	1.2	1.1	0.6	1
Offset Voltage [mV]	-	11.38	5	2.05
Noise [μV]	46	750	237	-

Energy [pJ]	0.98	0.081	0.038	0.108
Delay [ns]	11	0.047	5.77	0.167

Table 1: Dynamic Comparators Characteristics Comparison

(Canal, Klimach, Bampi, & Balen, 2021) achieves the lowest energy consumption (0.038 pJ) with a 0.6 V supply, optimized for low-power design. For precision, (Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020) and (Tang, et al., 2020)have the lowest offset voltage (2.05 mV) and noise (46 µV), respectively, making them suitable for noise-sensitive, high-accuracy applications. These are some of the trade-offs between speed, power efficiency, and accuracy, addressing key requirements for high-performance comparator designs, with (Siddharth, Jaya Satyanarayana, Nithin Kumar, Vasantha, & Bonizzoni, 2020) standing out as a balanced option for speed, power consumption, and precision.

Offset reduction techniques

The offset in comparators primarily results from mismatches between the transistors on both sides of the circuit, which ideally should be symmetric but often are not. The transistors that have the most significant impact on the offset are those that are activated first, as opposed to those that are turned on later in the process (Razavi, 2015).

This is a critical limitation, as it can lead to errors in detecting small signals. Several techniques have been developed to reduce offset. One such method is static offset cancellation, which involves adding extra transistors or other components to provide additional load capacitance or current on the unbalanced side. Another approach is dynamic offset cancellation, which incorporates an additional stage before the comparator, that senses the offset and attempts to correct it to prevent it from affecting the latch stage. However, it is important to note that the latch can also contribute to the offset. Therefore, it is possible to apply both

techniques within the same comparator to minimize the overall offset (Goll & Zimmermann, 2015).

Several studies have proposed techniques to reduce offset. For example, as seen in (Tsirmpas, Kontelis, Souliotis, & Plessas, 2024; Jaiswal, et al., 2020; Lee, et al., 2020; Sharma, Srivastava, Hande, Sehgal, & Das, 2023; Ahrar & Yavari, 2021), some approaches control the current flowing to the latch from the output of the first stage. In (Tsirmpas, Kontelis, Souliotis, & Plessas, 2024; Lee, et al., 2020; Sharma, Srivastava, Hande, Sehgal, & Das, 2023; Ahrar & Yavari, 2021), parallel transistors are sequentially activated based on the offset magnitude. In (Jaiswal, et al., 2020), a charge pump is used to provide voltage to two additional transistors, one on each side of the first stage output, to increase or decrease current. In (Ahrar & Yavari, 2021; Yousefirad & Yavari, 2021), body bias control is applied to the differential input pair transistors, adjusting their threshold voltage V_{th} according to the offset.

These methods require sensing the comparator outputs to determine the direction of mismatch and activate its calibration mechanism. As a result, digital control is necessary for effective calibration. **Table 2** shows the calibration techniques used in the referenced works, along with the initial offset values, the calibrated offsets achieved, and their consumed energy.

	(Tsirmpas, Kontelis, Souliotis, & Plessas, 2024)	(Jaiswal, et al., 2020)	(Lee, et al., 2020)	(Sharma, Srivastava, Hande, Sehgal, & Das, 2023)	(Ahrar & Yavari, 2021)	(Yousefirad & Yavari, 2021)
Process [nm]	65	180	14	180	180	180

Supply Voltage [V]	1	1.8	0.9	1.8	1	1
Calibration Technique	Discharge Current	Discharge Current	Discharge Current	Discharge Current	Discharge Current - Body Bias	Body Bias
Initial Offset [mV]	16	2.72	2.073	2.85	19.56	13.2
Calibrated Offset [mV]	1	0.013	0.259	0.445	0.363	0.3
Energy [pJ]	-	0.134	0.214	0.155	0.952 – 10.66	0.036

Table 2: Offset Calibration Techniques

The main objective of this work is to design and characterize a dynamic comparator. This involves analyzing its performance concerning energy consumption, noise, and delay across different input common modes, supply voltages, and temperature variations, as well as different process corners. After that, a compensation method will be introduced to reduce the offset voltage. The rest of the thesis is organized as follows. Chapter “Design of the Two-Stage Comparator” details the design of the two-stage comparator, including the pre-amplifier stage, output latch and layout. Chapter “Simulation and Analysis” focuses on the implementation of the simulations and their results. Chapter “Measurement of Fabricated Chips” presents the measurement setup and the results obtained from 15 fabricated chips, including noise and offset voltage. Finally, Chapter “Offset Reduction Techniques, Calibration, and Comparative

Analysis" introduces the offset reduction techniques, calibration process and a comparative analysis of the simulation results.

DESIGN OF THE TWO-STAGE COMPARATOR

Pre-Amplifier Stage

The first stage of the comparator is a pre-amplifier for the differential input signal (VinP and VinN) that reports the input voltages to a level that the latch can reliably detect. The Floating Inverter Amplifier (FIA) showed in **Figure 2** used in (Tang, et al., 2020; Canal, Klimach, Bampi, & Balen, 2021) is designed to enhance the performance of dynamic comparators, this block introduces combines pre-amplification with improvements in energy efficiency and noise management.

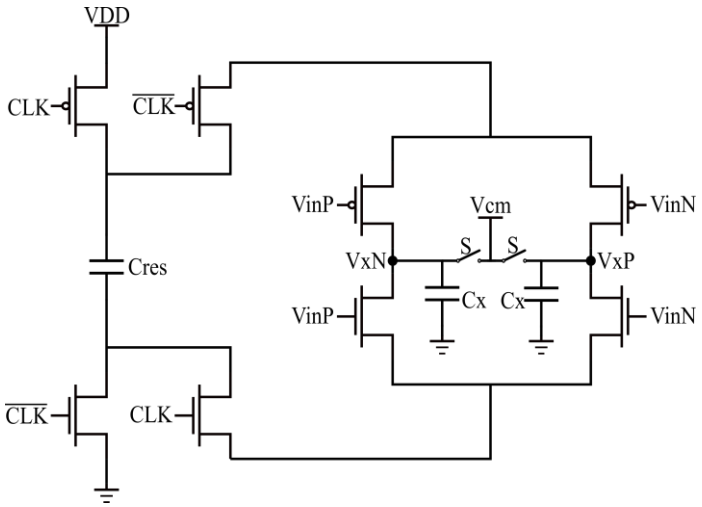


Figure 2: Floating Inverter Amplifier

The architecture integrates a floating reservoir capacitor, Cres, which enhances the stability of the dynamic comparator against variations in process corners and fluctuations in input common-mode voltage. By merging two conventional head and tail capacitors into a single floating reservoir capacitor, this design achieves a significant 75% reduction in total

capacitance (Tang, et al., 2020) showing that this design better adapts to variations in the circuit's operating conditions.

The capacitor Cres is connected through MOS switches controlled by the clock signal. During the low phase of the clock, the capacitor is connected to VDD and ground (**Figure 3a**), allowing it to recharge and maintain a stable reference level. In the high phase, the capacitor connects to the FIA, enabling operation within an isolated voltage domain, as shown in **Figure 3b**. This configuration helps maintain a consistent output common-mode voltage, essential for minimizing the impact of voltage fluctuations in the following stage.

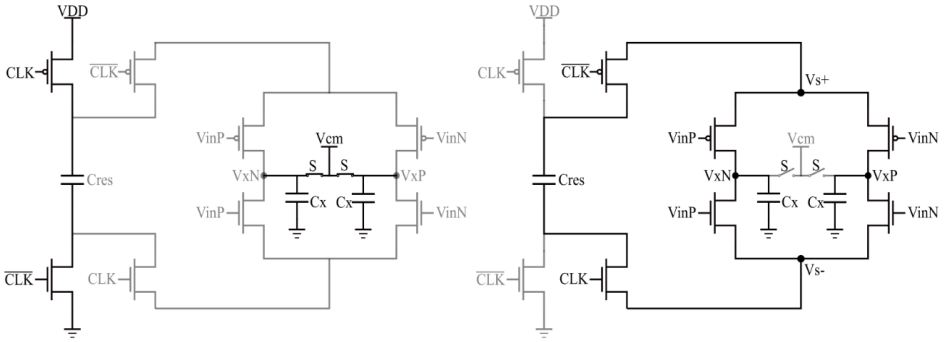


Figure 3: Floating Inverter Amplifier during the clock period

Additionally, this architecture balances the input and output currents of the reservoir capacitor. When the input voltages are equal, such as in a common-mode condition, the design forces the common-mode current entering the integration capacitor (Cx) to zero. This ensures that the output common-mode voltage remains stable without requiring an additional circuit for common-mode feedback.

As explained in (Tang, et al., 2020), this FIA is designed to work in a low-power mode because its transistors operate near the subthreshold region. This means that as the gate-source

voltage V_{gs} decreases, the transistors stay in this low-power region, which significantly reduces energy consumption.

To analyze the gain of the amplifier in this low-power mode, we first study its transconductance, Gm in the subthreshold region. The transconductance describes the relationship between the input voltage and the resulting current. In this region, Gm is calculated based on the amplifier's tail current I_{amp} divided by the thermal voltage U_T and the factor n that depends on the transistor characteristics. The equation (10) shows that in the subthreshold region, the transconductance mainly depends on the tail current:

$$Gm(t) \cong \frac{I_{amp}}{n \cdot U_T} \quad (1)$$

Next, the differential output voltage of the amplifier, $\Delta V_{X,DM}$ depends on the differential input voltage and the transconductance over time. The output voltage can be determined by integrating the previously mentioned factors:

$$\Delta V_{X,DM}(t) = \frac{\int_0^t \Delta V_{I,DM} \cdot G_m(\tau) d\tau}{Cx} \simeq \frac{\Delta V_{I,DM} \int_0^t Iamp(\tau) d\tau}{n \cdot U_T \cdot Cx} \quad (2)$$

The equation (2) shows that the differential output voltage $\Delta V_{X,DM}$ is influenced by the variation of the tail current over time.

The variation in the source nodes of the PMOS and NMOS transistors (V_{s+} and V_{s-}) over time, is defined in equation (3), where ΔV_S is also affected by the tail current and the reservoir capacitance Cres.

$$\Delta V_S(t) = \frac{\int_0^t Iamp(\tau) d\tau}{2 \cdot Cres} \quad (3)$$

Finally, to obtain the amplifier's gain during the comparison time T_{int}, it is been used the equation (4) .

$$A_V = \frac{\Delta V_{X,DM}(T_{int})}{\Delta V_{I,DM}} = \frac{2 \cdot Cres \cdot \Delta Vs(T_{int})}{n \cdot Cx \cdot U_T} \quad (4)$$

This expression shows that the gain mainly depends on the change in source voltage ΔVs , which is determined by how the tail current varies over time. This approach ensures that the amplifier achieves a high gain, even while operating in a low-power mode.

Latch Stage

The second stage is a clocked latch, illustrated in **Figure 4**, responsible for generating a digital output based on the amplified differential input from the previous stage. It receives the pre-amplifier output signals, VxN and VxP. During the low phase of the clock, these nodes are grounded, which resets the latch and prepares it for the next evaluation cycle. In the high phase, the latch is connected to VDD, and it starts the decision process according to the input differential signals.

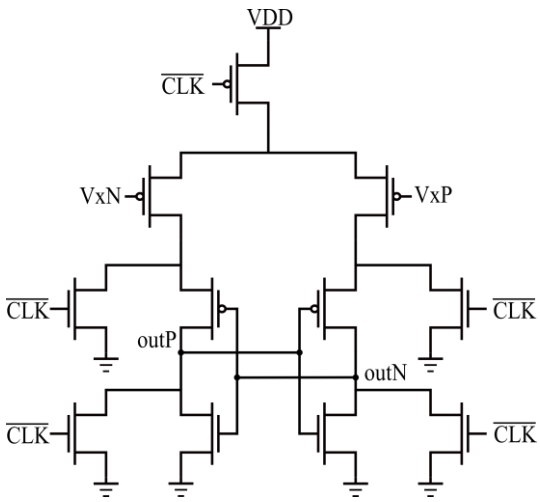


Figure 4: Output Latch

This operates similarly to the StrongArm Latch but with the main modification of the addition of the previous stage, so the input signals in this latch are designed to be insensitive to changes in the input common-mode voltage, this insensitivity improves the reliability of the digital output, as it reduces the effects of input voltage variations.

The comparator's differential output, noted as ΔOut , is obtained by taking the difference (equation (5)) between the two latch outputs: OutP and OutN. Since the output latch signal is taken as digital, ΔOut can be represented as either 1 or -1, as shown in equation (6). When OutP is high and OutN is low, ΔOut is 1. On the other hand, when OutP is low and OutN is high, ΔOut becomes -1.

$$\Delta Out = \mathrm{OutP} - \mathrm{OutN} \quad (5)$$

$$\Delta Out = \begin{cases} 1 \ if \ OutP \ = \ 1 \ and \ OutN \ = \ 0 \\ -1 \ if \ OutP \ = \ 0 \ and \ OutN \ = \ 1 \end{cases} \quad (6)$$

Layout Design

The layout of the complete comparator, shown in **Figure 5**, was created to estimate the occupied area and enable post-layout simulations for more accurate analysis of its performance characteristics. As observed, the FIA occupies more than half of the total area, which is 100.98 μm^2 .

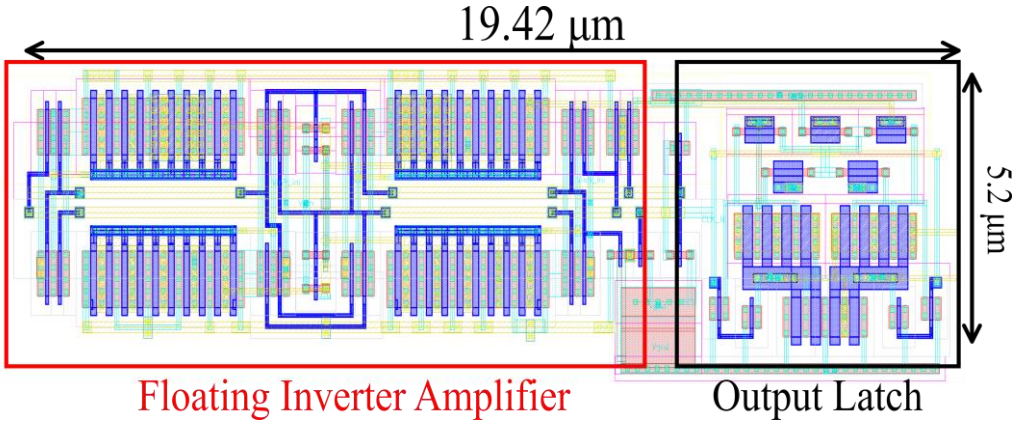


Figure 5: Comparator Layout

SIMULATION AND ANALYSIS

Simulation Setup

The simulation of the two-stage comparator was performed using Cadence Virtuoso in a 65nm commercial technology, focusing on offset, noise, energy consumption, and delay. The setup included configuring the circuit for analysis in nominal conditions with a supply voltage of 1.2 V, a temperature of 27 $°C$, and following simulations under changes across process variation to characterize the comparator's behavior under different fabrication conditions. Finally, simulations across a range of temperatures and supply voltages to examine their effects on performance.

To assess sensitivity, the input common-mode voltage (i-Vcm) was adjusted, while a sweep of the differential input voltage (ΔVin) was used to evaluate both power consumption and delay. Additionally, noise analysis was conducted by enabling transient noise in the simulation, allowing for an evaluation of its impact on the comparator's decision accuracy.

Offset Analysis

To evaluate the offset, a Monte Carlo simulation was conducted, which is convenient for analyzing the effects of random variations, such as mismatches due to the manufacturing process. These random mismatches lead to differences in device characteristics, the Monte Carlo simulation is an effective method to statistically analyze the offset by examining multiple instances of the circuit.

For this analysis, it was applied the methodology described in \cite{offset_meth}, where a differential input voltage ramp, shown in **Figure 6**, is used. This ramp, generated with Verilog-A code, sweeps from the minimum value of -15 mV to a maximum of 15 mV with a step size of 0.2 mV, this differential voltage will be centered around a i-Vcm at the comparator inputs. By applying this ramp, we can track the necessary input level for the comparator output to change its logic state. In an ideal scenario, the transition would occur at zero differential input; however, due to manufacturing mismatches, this switching occurs at a nonzero differential input, showing the offset voltage.

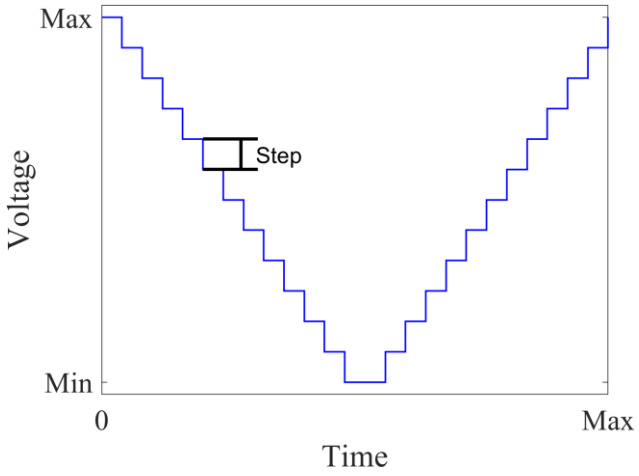


Figure 6: Input Voltage Ramp

The offset voltage is determined by finding the ΔVin at which the differential output transitions from -1 to 1 (or vice versa). This measurement is taken for both the rising and falling

parts of the ramp to obtain an average offset value, an example is shown in **Figure 7** where the offset is given ideally at 0 mV in the ramp during the transitions.

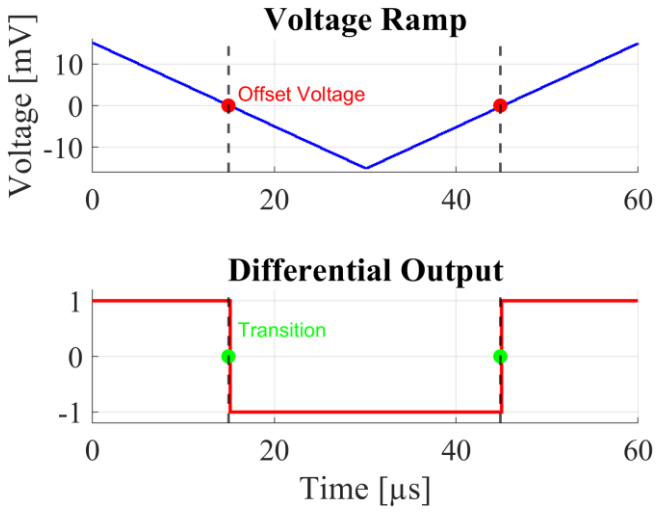


Figure 7: Offset voltage measurement

After completing 1000 Monte Carlo simulation runs, the offset voltage results in a normal distribution, where the mean is expected to be close to zero, and the standard deviation reflects the spread caused by process variations. **Figure 8** shows this distribution when the i-Vcm is set to 600 mV. The offset values follow the normal distribution centered around a mean (μ) of 0.0198 mV, showing that on average, the comparator offset is very close to zero, as expected. The standard deviation (σ) shows a spread of 3.184 mV out from the mean, suggesting that most offset values lie within ±3 mV of the mean, the distribution gives useful information about the offset performance of the comparator, as a low mean and moderate standard deviation indicate that the comparator offset is generally small across the Monte Carlo simulation.

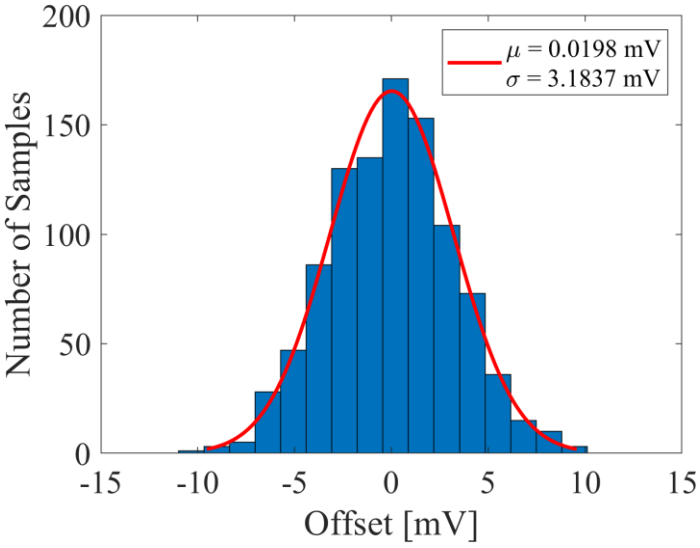


Figure 8: Offset voltage normal distribution for i-Vcm=600 mV

Input-Referred Noise Analysis

Input-Referred Noise (IRN) analysis is essential for assessing how noise influences the comparator's accuracy and stability. Transient noise was used, the noise factor was incrementally adjusted until the simulated noise produced an IRN value comparable to the measurements obtained from the fabricated chip. This process ensured that the noise levels in the simulation matched the real-world conditions, providing a precise representation of how the design would behave in actual noisy situations.

It was characterized by conducting 1000 measurements at each ΔVin step, sweeping from -7 mV to 7 mV in increments of 0.2 mV, this allows us to determine the probability of obtaining specific output values at each ΔVin step. The number of 1's obtained was counted at the $\Delta Vout$, observing that as ΔVin increased, the occurrence of 1's also increased, then, the probability was calculated by dividing the obtained number of 1's by the total measurements (1000 in this case). The obtained curve was used to calculate the standard deviation of the output distribution, which shows the noise impact on the comparator.

For the interpretation of these values, the output data was fit to a Cumulative Distribution Function (CDF). This CDF fitting provides a visual representation of the noise effect by showing the probability trend across ΔVin values, as shown in **Figure 9** for common-mode input voltage of 600 mV, the IRN is 0.692 mV. This shows how noise affects the comparator's switching during the variation of the ΔVin.

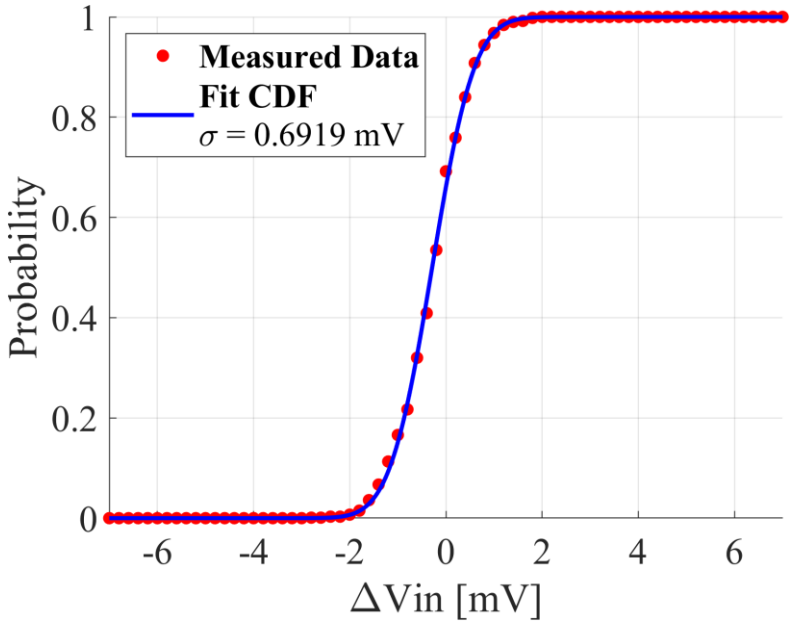


Figure 9: IRN at Input-Vcm=600 mV

The IRN versus i-Vcm plot shown in **Figure 10** provides the noise performance of the comparator across different input conditions, it has a mean value of approximately 699.80 µV , with minimum and maximum values of 637.60 µV and 852.29 µV, respectively. Also, it remains fairly consistent between 300 mV and 800 mV i-Vcm, suggesting that the comparator maintains a consistent noise performance within this range. However, as i-Vcm approaches 900 mV, there is a sharp increase in IRN, which may indicate an increased sensitivity to common-mode variations at higher input levels. This trend suggests that the comparator may work better for applications where the i-Vcm remains within that stable range, as performance gets worse at the extreme.

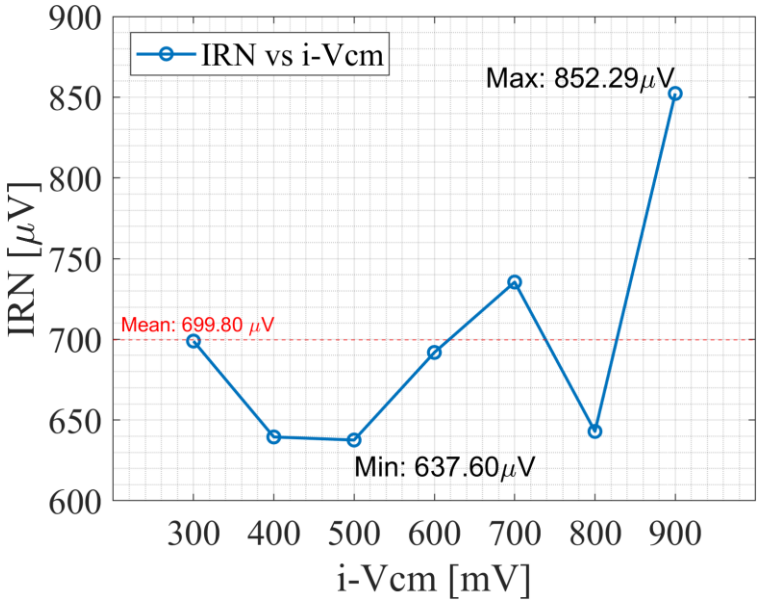


Figure 10: IRN at different Input-Vcm

Energy and Delay Analysis

Energy consumption and delay are two key metrics that impact the efficiency of the comparator. This analysis looks at how energy and delay change with different input conditions, including the i-Vcm and variations in ΔVin . Simulations were performed for three i-Vcm levels (300 mV, 600 mV, and 900 mV) with ΔVin values of 1, 5, 10, 50, and 100 mV for each.

As shown in **Figure 11**, ΔVin has a clear effect: when ΔVin is smaller, the comparator needs more energy and time to make a decision, which increases both energy consumption and delay. For i-Vcm variation, the maximum difference in energy is 0.006 pJ , which is quite small, indicating that FIA keeps the comparator stable against changes in i-Vcm. Similarly, i-Vcm has only a small effect on delay.

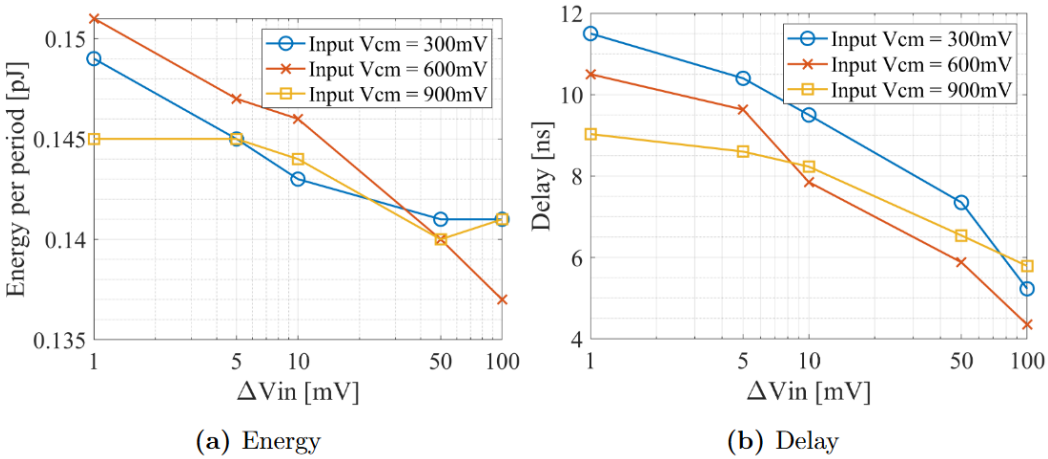
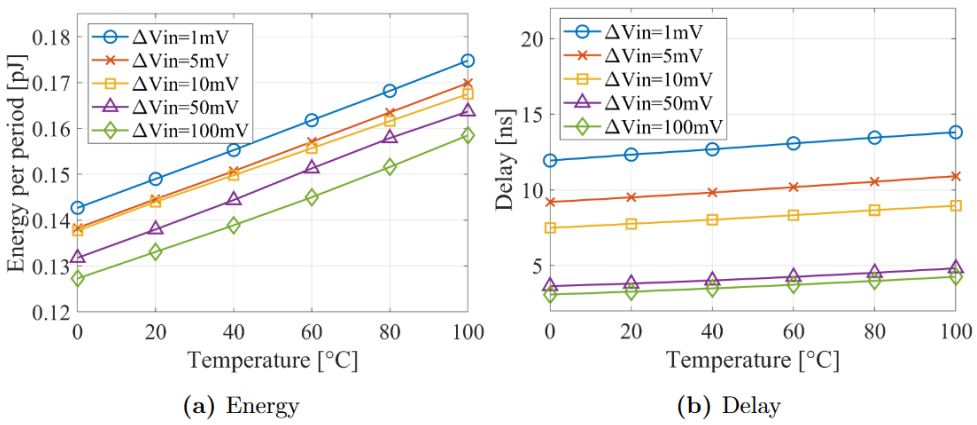


Figure 11: Energy and Delay in input common mode voltage variation

Variations in Temperature and Supply Voltage

The performance of the comparator was analyzed under varying temperature and supply voltage conditions to assess its robustness.

Figure 12 shows how energy consumption and delay change with temperature for different ΔVin in the comparator. In **Figure 12a**, energy consumption increases noticeably with increasing temperature, regardless of the ΔVin value. The increase in energy from 0 $°C$ to 100 $°C$ is approximately 0.032 pJ, which is translated to about 0.0064 pJ per 20 $°C$. This trend shows that the comparator becomes less energy-efficient at higher temperatures. In contrast, **Figure 12b** shows that delay remains relatively stable across the analyzed temperature range, with only a minor variation of around 1 ns between the lowest and highest temperatures. Overall, the results suggest that it mainly affects energy consumption rather than delay, with higher temperatures leading to increased energy use while delay remains mostly unchanged.



(a) Energy (b) Delay

Figure 12: Energy and Delay in Temperature Variation

Figure 13 shows how IRN changes with temperature. As we can see, the IRN varies significantly across the temperature range of 0 °C to 100 °C. The noise level reaches its lowest value, 712.19 µV , at around 80 °C, while the highest noise level, 767.93 μV, occurs at 100 °C. The mean IRN across all temperatures is 732.83 μV, indicated by the red dashed line.

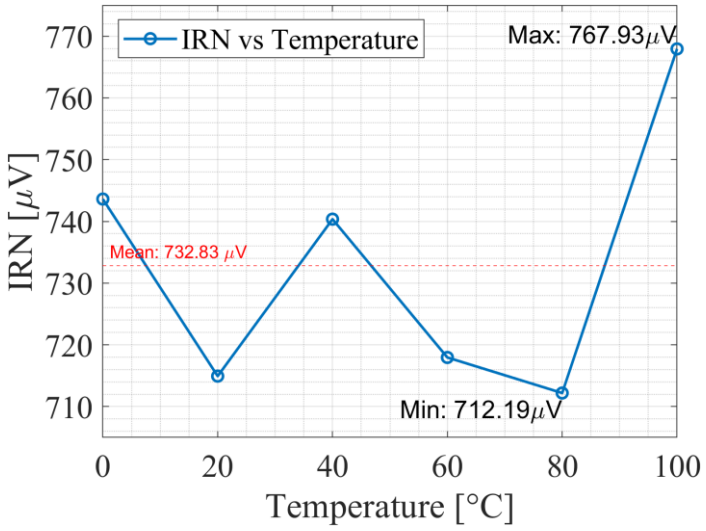


Figure 13: IRN in Temperature Variation

These results suggest that temperature does not have a big impact on the noise levels as opposed to i-Vcm variations, with IRN increasing notably at higher temperatures. Such variations in noise can affect the accuracy and stability of the circuit's performance.

Figure 14 shows how energy consumption per period and delay vary with changes in VDD and ΔVin. In **Figure 14a**, can be observed that energy usage decreases slightly as ΔVin increases across all supply voltages. The lowest energy consumption occurs at VDD = 0.9 V, while the highest is at VDD = 1.2 V, indicating that higher supply voltages result in greater energy usage. The difference between the lowest and highest energy consumption is approximately 0.08 pJ and remains nearly constant across all ΔVin values. This shows that variations in supply voltage have a more significant impact on energy consumption than changes in ΔVin. In **Figure 14b**, the delay also decreases as ΔVin increases. The delay meets its maximum at VDD = 0.9 V and the minimum at VDD = 1.2 V, with a difference of 13 ns at ΔVin = 1 mV, while at ΔVin = 100 mV the difference gets reduced to 5 ns . This shows that a higher supply voltage reduces delay, making the circuit behave faster, but its impact gets reduced as the ΔVin increases, different from energy analysis, where supply voltage consistently affects energy consumption across all the ΔVin values.

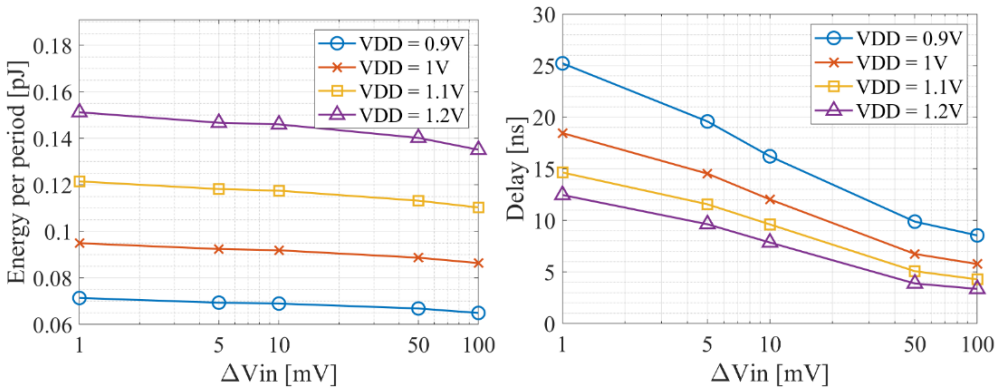


Figure 14: Energy and Delay in Supply Voltage Variation

Increasing the supply voltage leads to higher energy consumption but reduces delay, these trade-offs have to be analyzed based on the performance and power efficiency requirements.

Figure 15 shows the variation of IRN with different VDD. The plot shows that IRN decreases as VDD increases from 1 V to 1.2 V. The highest noise level, 1098.58 μV, occurs at VDD = 1 V, while the lowest noise of 691.87 μV, is observed at VDD = 1.2 V. The mean IRN across all supply voltages is 949.82 μV, which shows that the VDD highly affects noise performance.

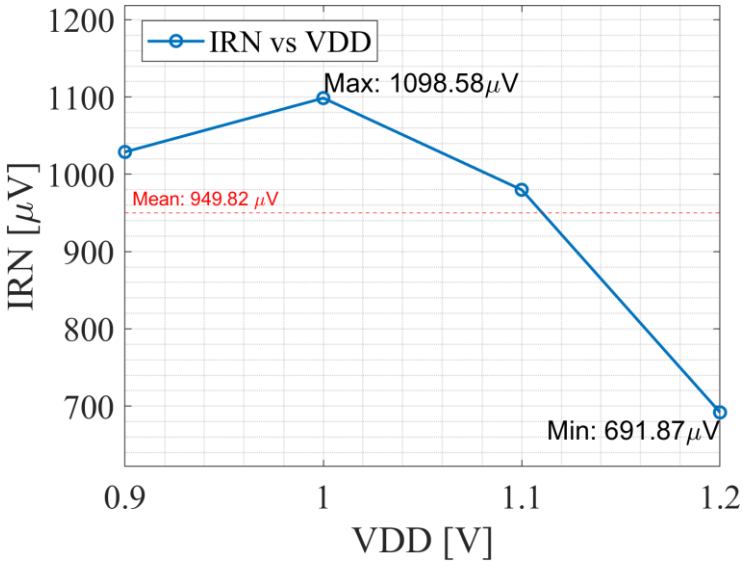


Figure 15: IRN in Supply Voltage Variation

These results highlight the impact of supply voltage on noise levels. Higher supply voltages result in lower IRN, which could improve the precision and stability of the circuit. Therefore, in the need for a low-power application, noise will be affected by reducing the VDD.

Process Variation

To evaluate the impact of process variations, simulations were performed for different process corners: TT (Typical-Typical), SS (Slow-Slow), SF (Slow-Fast), FS (Fast-Slow) and FF(Fast-Fast).

Figure 16 shows the effects of process variation on both energy consumption and delay as the input voltage difference increases.

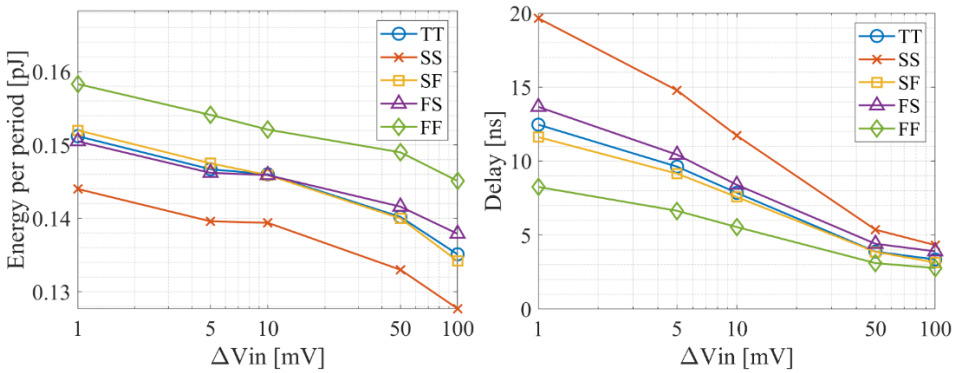


Figure 16: Energy and Delay in Process Variation

In **Figure 16a**, we see that energy consumption decreases as ΔVin increases across all corners. However, the FF corner has higher energy consumption, approximately 0.014 pJ more than the SS corner in each ΔVin variation. This pattern shows that process variations can result in notable differences in energy usage, which could be critical for power-sensitive applications. Delay also is diminished as ΔVin increases in **Figure 16b**, with SS showing the longest delay and FF the shortest. In general, corners with lower energy consumption, such as SS, tend to have longer delays, while those with higher energy usage, such as FF, exhibit shorter delays. At ΔVin = 1 mV, the impact of process variation on delay is most noticeable, with a difference of 11 ns between the SS and FF corners. However, this difference gradually decreases as ΔVin increases, reducing to about 3 ns at ΔVin = 100 mV. This correlation shows that circuits operating in processes that make the circuits consume more energy may also perform faster.

Thus, the difference in energy and delay across the corners highlights the importance of considering process variation when designing for consistent speed, given that delays and energy consumption can change considerably depending on the specific process.

Figure 17 shows the IRN across different process corners. The SS corner has the highest IRN with 894.01 μV, showing that it is more sensitive to noise, while the FF corner has the lowest at 601 μV. Comparing this with the energy and delay results, circuits in the SS corner consume less energy but experience higher noise levels and longer delays. On the other hand, the FF corner has lower noise and shorter delays but consumes more energy. This comparison points out how process variations impact performance and energy efficiency, with each corner exhibiting trade-offs between noise sensitivity, delay, and power consumption.

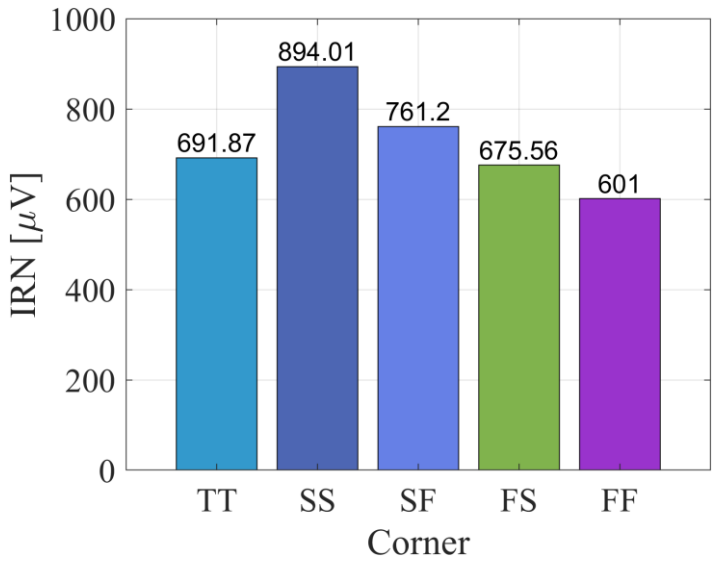


Figure 17: IRN in in Process Variation

MEASUREMENT OF FABRICATED CHIPS

Measurement Setup

The comparator analyzed in **Chapter "Design of the Two-Stage Comparator"** and with simulation results shown in **Chapter "Simulation and Analysis"** was fabricated. Fifteen chips were tested using a supply voltage of 1.2 V and a common-mode voltage of 0.6 V. The comparator inputs (VinP and VinN) were set to a differential input $\Delta Vin = VinP - VinN$ from -6 mV to 6 mV, with steps of 0.2 mV. If the offset voltage fell outside this range, the window was adjusted to ensure accurate measurement. This setup was tested at input common-mode voltages of 300 mV, 400 mV, 500 mV, and 600 mV. For each ΔVin step, an FPGA was configured to take 3000 measurements of the comparator outputs to determine the probability of obtaining a "1" in all the samples. This process was repeated 10 times for each step to obtain an average for each measurement, this process is similar to the one performed with the IRN in the simulation. After obtaining the average probability of 1's for each step, the data was fitted to a CDF, where the mean (μ), represents the offset of the comparator, and the standard deviation (σ), represents the IRN. An example of the measured data for one chip with an input common-mode voltage of 600 mV is shown in **Figure 18**, where the offset voltage is 2.59 mV and the IRN is 728.2μV.

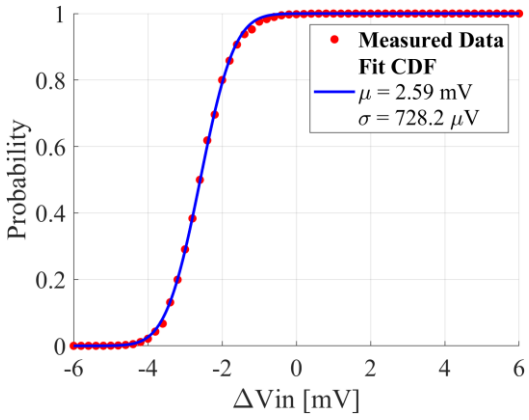


Figure 18: CDF for Chip 4 at i-Vcm = 600 mV

Figure 19 shows an image of the setup used for measuring the chips. It includes the required voltage sources, the FPGA, and the chip test board.

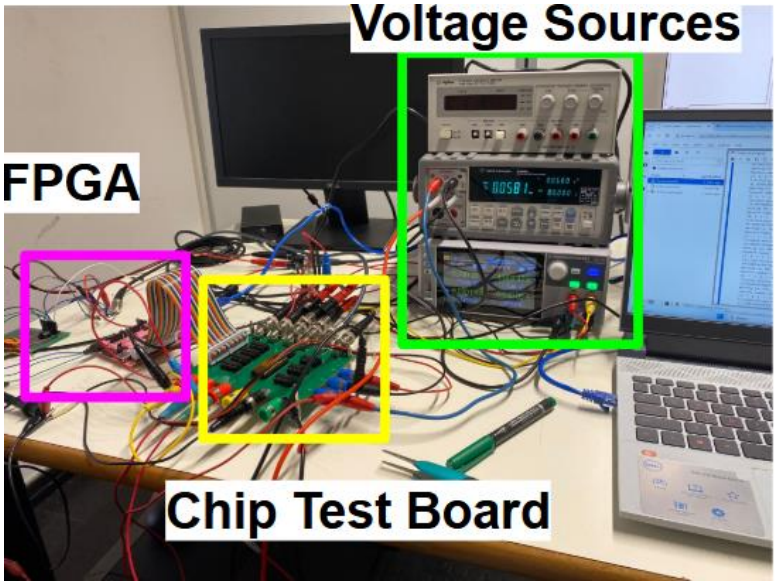


Figure 19: Measurement Setup

Noise and Offset Results

Noise and offset measurements were taken from 15 fabricated comparator chips to evaluate performance.

The measured offset voltage for the 15 chips is shown in **Figure 20**, tested under four input common-mode voltages of 300 mV , 400 mV, 500 mV, and 600 mV. The offset values span from a minimum of -5.63 mV in chip number 6 to a maximum of 6.78 mV in chip number 11, both of which occur at i-Vcm = 600 mV. Overall, the offset values remain relatively consistent across different i-Vcm levels for each chip, with only minor variations. Except for chips 2 and 15, where a minor spread on the offset voltage can be seen, suggesting that i-Vcm changes have minimal impact on offset in most cases.

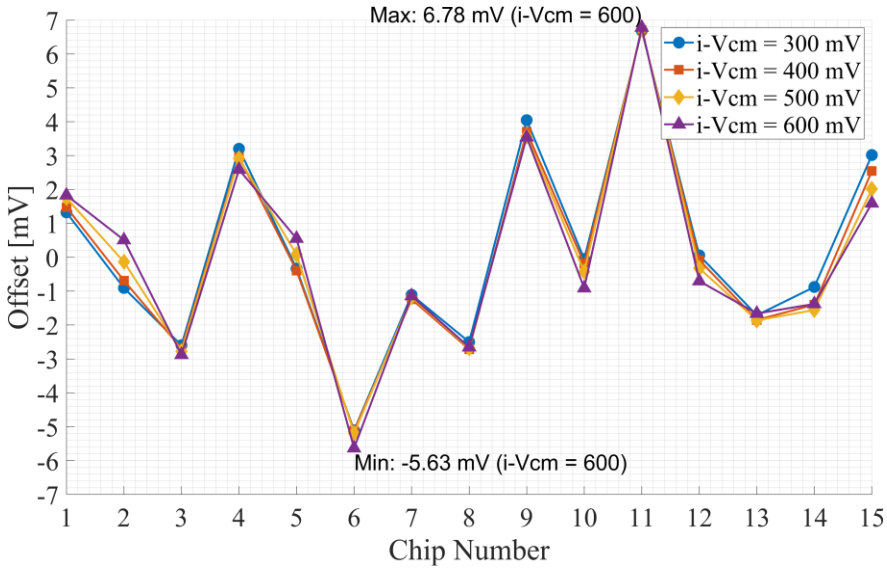


Figure 20: Measured offset in chips for different i-Vcm

Figure 21 shows the average offset voltage across all the chips at each input common-mode voltage level. The mean offset decreases as i-Vcm increases, starting from a maximum of 3.006 mV at i-Vcm = 300 mV and reaching a minimum of 2.968 mV at i-Vcm = 500 mV. This trend indicates that the offset voltage in i-Vcm variation is almost imperceptible.

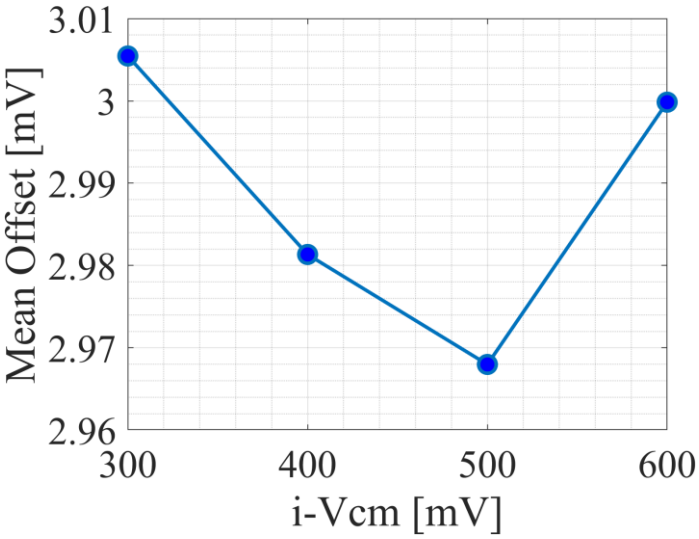


Figure 21: Mean offset in chips for different i-Vcm

Figure 22 shows the input-referred noise measurements for the 15 chips, at the four tested input common-mode voltages. The IRN values range from a minimum of 646.67 μV at

i-Vcm = 400 mV in the chip number 3 to a maximum of 1076.89 μV at i-Vcm = 600 mV in the chip number 6. In contrast to the offset plot, the IRN values for each chip show a more noticeable spread at each i-Vcm level, indicating that noise is more sensitive to changes in i-Vcm. However, there is no clear trend in the noise values across i-Vcm levels. For some chips, a particular i-Vcm results in minimum noise, while for others, the same i-Vcm shows maximum noise. This suggests that additional factors beyond i-Vcm influence noise performance. The variability in noise performance across all chips is also significant, indicating that process variation has an impact on noise as well.

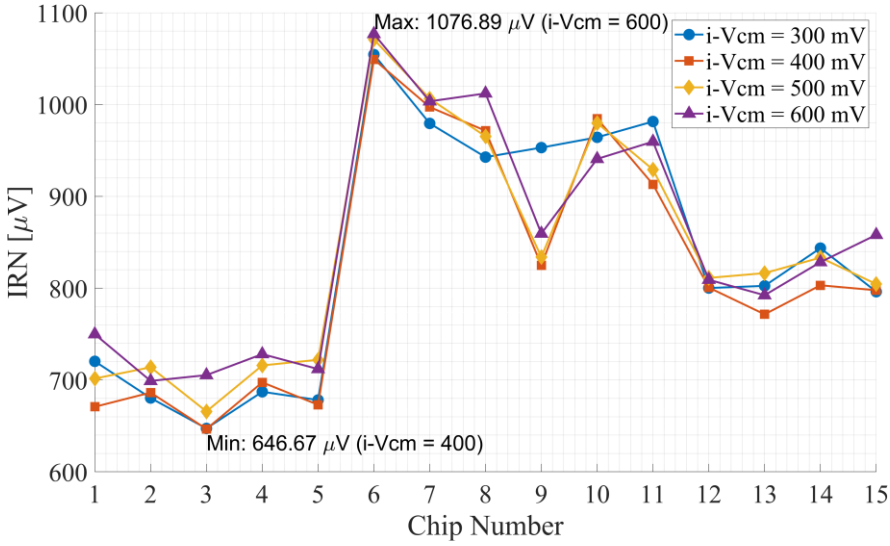


Figure 22: Measured noise in chips for different i-Vcm

Figure 23 shows the average noise across the 15 chips at each i-Vcm level. The mean noise does not change considerably with i-Vcm. The lowest mean noise is observed at i-Vcm = 400 mV, with a value of 819.21 μV. Noise increases slightly at 500 mV and reaches a maximum of 848.99 μV at 600 mV. This pattern suggests that noise is lowest around the 400 mV input common-mode voltage but increases at higher i-Vcm levels. Compared to the offset mean plot, this suggests a possible trade-off between offset and noise performance.

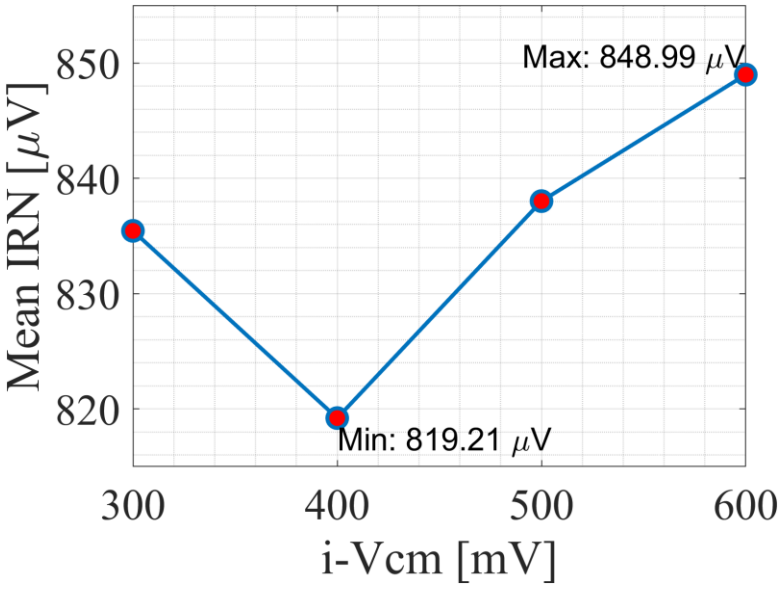


Figure 23: Mean noise in chips for different i-Vcm

OFFSET REDUCTION TECHNIQUES, CALIBRATION, AND COMPARATIVE ANALYSIS

Selected Offset Reduction Techniques

After the measurement of the fabricated chips, the comparator exhibits an offset in the millivolt range, similar to the results seen in simulations. To reduce this offset, a self-calibration technique could be applied. Several offset calibration techniques can be used to achieve this goal. In this case, a load capacitance adjustment method was chosen, where the load capacitance is modified according to the mismatch.

Some modifications to the original comparator design were made in the Output Latch Stage. Adjustments were required, such as the sizing of the input transistors that receive the output signals from the first stage (VxP and VxN) and the head transistor triggered by CLK signal. To achieve an accurate offset compensation, 22 capacitors were added, as shown in **Figure 24**. Eleven capacitors were placed on each side of the latch in parallel, where each capacitor can be added to the load of the node through the activation of a transmission gate. This setup combines a MIM capacitor (C0) with 10 NMOS transistors (C1-C10) connected as capacitors (Drain-Source-Bulk connected to ground node). The use of a MIM capacitor combined with NMOS capacitors proves effective in reducing silicon area while achieving a fine offset granularity of 0.5 mV.

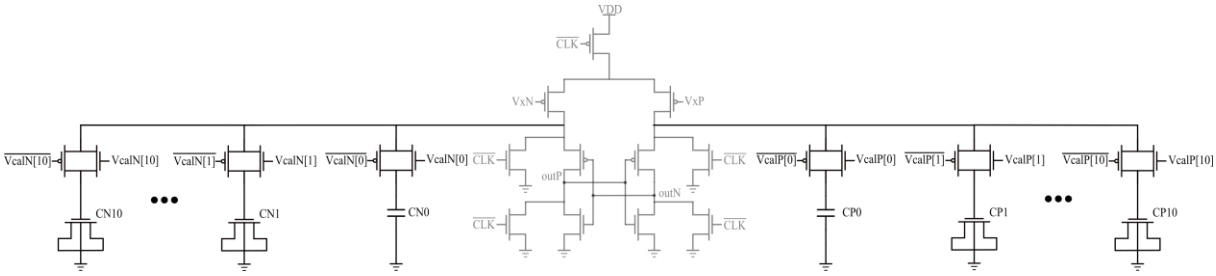


Figure 24: Capacitive Load added to the Latch Stage

As shown in **Table 3**, each capacitor compensates for a defined step, with capacitors C1 to C6 capable of being connected to achieve a compensation of up to 5 mV. If greater compensation is required, the MIM capacitor C0 can be used as a baseline to provide the same 5 mV compensation. Larger capacitors (C7–C10) are designed to provide an incremental increase of approximately 1 mV each when connected to the MIM capacitor C0. Without the MIM capacitor, achieving the same granularity would require additional NMOS capacitors, resulting in increased silicon area overhead.

Capacitor	**Size**	**Offset Compensation**
C0 (MIM-Cap)	2.3 μm x 2.3 μm	~ 5 mV
C1	120 nm x 60 nm	~ 0.5 mV
C2	120 nm x 60 nm	~ 0.5 mV
C3	240 nm x 240 nm	~ 1 mV
C4	290 nm x 280 nm	~ 1 mV
C5	350 nm x 350 nm	~ 1 mV
C6	440 nm x 400 nm	~ 1 mV
C7	600 nm x 600 nm	~ 1 mV (with MIM-Cap)
C8	750 nm x 750 nm	~ 1 mV (with MIM-Cap)
C9	950 nm x 950 nm	~ 1 mV (with MIM-Cap)
C10	1.7 μm x 850 nm	~ 1 mV (with MIM-Cap)

Table 3: Capacitors size and offset compensation step

To determine the offset direction, the inputs of the comparator are shorted to the same voltage, creating a ΔV_{in} = 0 mV condition. This setup will indicate which side (OutP or OutN) is stronger due to mismatch, enabling the circuit to apply the calibration technique. The working

principle of the capacitive load technique is based on adjusting the output capacitance to account for mismatch. A capacitance is added to the stronger output side. This additional capacitance slows down the stronger side, by redirecting the current to the capacitor, allowing the weaker side to catch up. As a result, the offset is reduced, shifting it toward the center.

The layout for the additional calibration circuit was also designed. Each side includes 11 transmission gates with a PMOS and an NMOS each, 10 NMOS transistors acting as capacitors, and 1 MIM capacitor, as shown in **Figure 25**. The layout area is 36.5 μm^2 per side, resulting in 73 μm^2 for both sides. Each MIM capacitor occupies an area of 5.3 μm^2 with a total of 10.6 μm^2 for both capacitors.

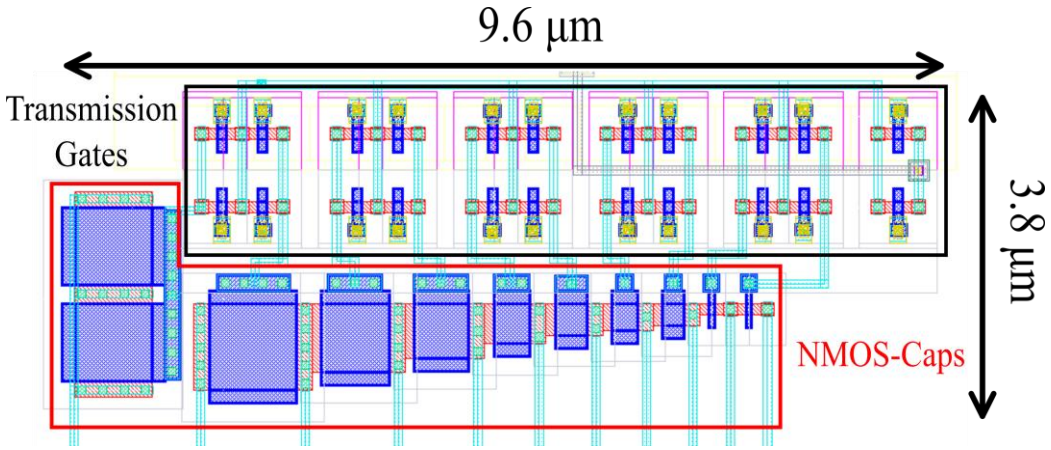


Figure 25: Layout Additional Capacitor Calibration Circuit

To compare the presented technique, two other methods were simulated on the same comparator to evaluate their performance and identify their trade-offs. Both methods were tested under the same setup conditions.

The first method, reported in (Jaiswal, et al., 2020), uses a current injection approach with two additional transistors, one on each side, connected in parallel to the input transistors of the output stage, as shown in **Figure 26**. Depending on the offset direction, these extra transistors either increase or decrease current injection to balance the comparator outputs by

adjusting their gate voltage, which is controlled by the charge pump circuit shown in **Figure 27a**.

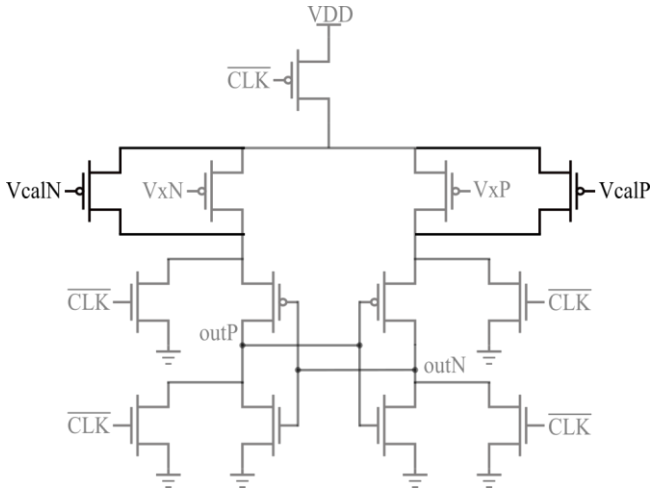


Figure 26: Additional Transistors in the output stage for Charge Pump approach

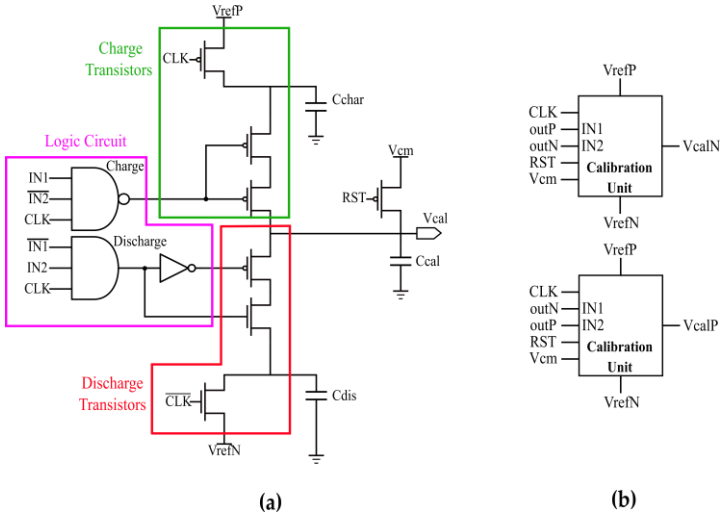


Figure 27: Additional Components for the Gate Voltage Control for Charge Pump approach.

a) Charge Pump Circuit. b) Inputs and Outputs of the Charge Pump circuits

A combination of signals IN1, IN2, and CLK is used, to determine the activation of Charge and Discharge nodes, as illustrated in **Figure 27a**. This decision is implemented using a NAND gate for the Charge signal and an AND gate for the Discharge signal. The logic

equations governing the activation of Charge and Discharge signals are given by Equations (7) and (10), respectively.

$$Charge = \overline{CLK \cdot IN1 \cdot \overline{IN2}} \quad (7)$$

$$Discharge = CLK \cdot \overline{IN1} \cdot IN2 \quad (8)$$

These signals are activated only when CLK is high and IN1 and IN2 have opposite values.

To control whether VcalP or VcalN needs to increase or decrease, the input signals shown in **Figure 27b** are used. For VcalP, the comparator output outP is connected to IN1, and outN is connected to IN2. Connections are inverted in the case of VcalN, with outN connected to IN1 and outP to IN2. This setup ensures that, based on the comparator outputs, one calibration unit charges while the other discharges.

The operation of the charge pump proceeds as follows: the process begins by triggering the RST signal, which sets the capacitor Ccal to an initial voltage corresponding to the circuit's common-mode voltage in this case. When the circuit needs to increase the voltage on Ccal, as illustrated in **Figure 28a**, Cchar is charged to a reference voltage VrefP. After charging, Cchar is connected in parallel with Ccal, creating a slight voltage increase on Vcal due to charge redistribution. Vcal is applied to the gate of the added PMOS transistor, as a result, this voltage increase leads to a controlled reduction in the current flowing into the latch.

Similarly, as one side of the output latch charges, the opposite side discharges. For discharging, as shown in **Figure 28b**, Cdis is connected to a lower reference voltage VrefN. In each clock cycle, Cdis is connected in parallel with Ccal, causing a small reduction in Vcal,

which produces a small increase in current, in contrast to the charging side of the output stage. As a result, this adjustment is applied to the weaker side.

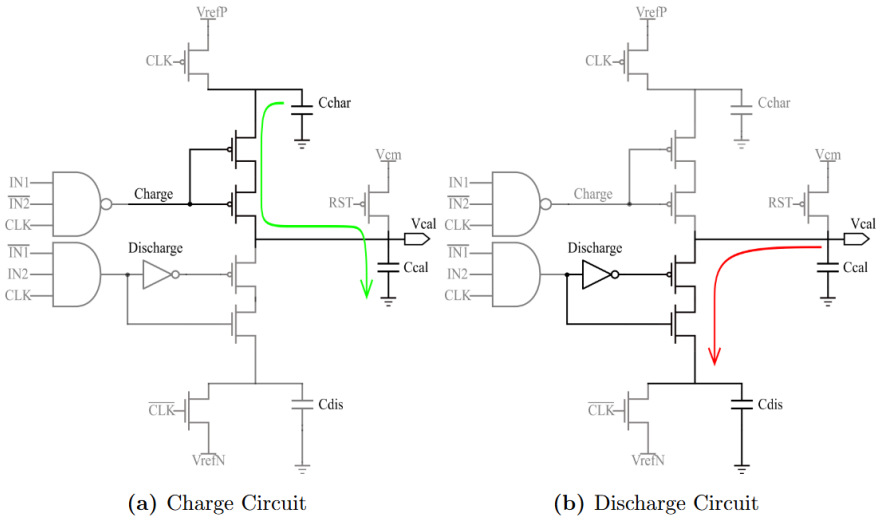


Figure 28: Charging and Discharging of the Charge Pump

To determine the required capacitance for Ccal, Equation (10) was used. This formula is derived from the charge distribution between the capacitors connected in parallel during each clock cycle, based on the reference voltages VrefP and VrefN, as well as the desired voltage step for the gate of the additional transistors in the latch.

$$Ccal = Cchar \cdot \frac{Vref - (Vo + Vstep)}{Vstep} \quad (9)$$

Where Vo is the initial voltage for the Ccal capacitor, set to Vcm, and Vstep is the chosen voltage increment or decrement for VcalP and VcalN.

In this design, VrefP is set to 900 mV, the maximum voltage Ccal can reach, and VrefN is set to 300 mV, the minimum voltage for Ccal. The smallest MIM capacitors available in the chosen technology (a 65-nm commercial node) present an area of 4 μm^2 and a capacitance of 5.63 fF, which are used for Cchar and Cdis. The desired gate voltage step is 2.5 mV, and the

initial voltage Vcm on both sides is 600 mV. Applying the Equation (9), the required capacitance for Ccal is calculated in Equation (10).

$$Ccal = 5.63 \cdot 10^{-15} \cdot \frac{0.9 - (0.6 + 0.0025)}{0.0025} = 669.97fF \quad (10)$$

The layout of the charge pump approach is presented in **Figure 29**. Each side occupies 19.25 μm^2, resulting in a total of 38.5 μm^2 for both sides. Additionally, the MIM capacitors require a combined area of 1266 μm^2 for six capacitors, with three on each side.

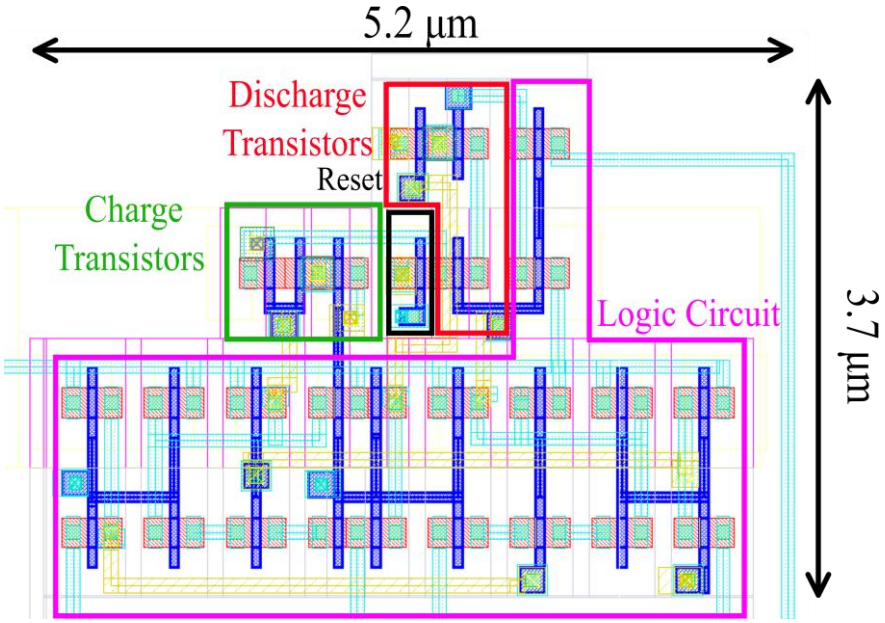


Figure 29: Layout Additional Charge Pump Circuit

The second method used for comparison is based on the approach reported in (Lee, et al., 2020; Sharma, Srivastava, Hande, Sehgal, & Das, 2023), which also uses current injection with a set of additional transistors. This approach was adapted to the output latch as shown in **Figure 30**, with 25 PMOS transistors on each side, connected in parallel with the input transistors of the output stage. Nodes VxN and VxP are used as gate voltage of the additional

transistors. Each transistor includes a PMOS switch that allows it to be attached or detached, depending on the required offset voltage compensation.

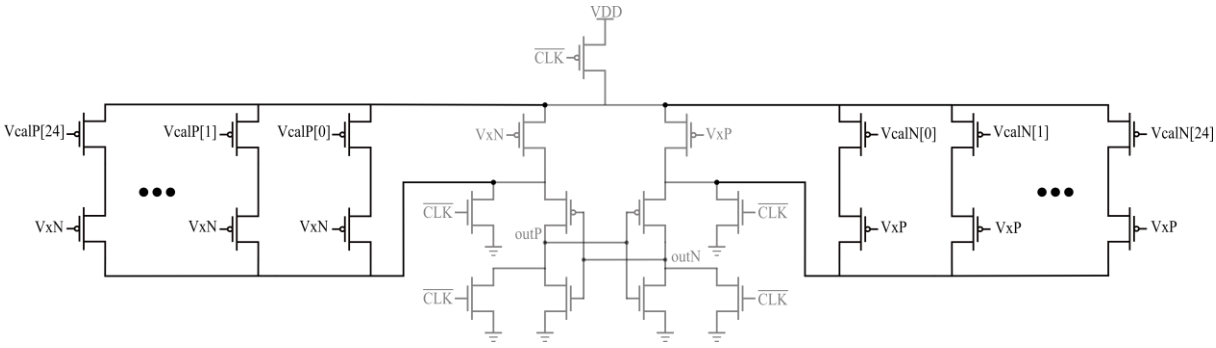


Figure 30: Parallel transistors added to the Latch Stage

The number of additional transistors was selected based on the desired calibration step size. To achieve a more precise calibration and to make a fair comparison with the proposed method, a step of 0.5 mV was chosen. To compensate for offset voltages up to 12.5 mV, Table \ref{t:transis_offset} shows the transistor sizes required and their respective contributions to offset voltage compensation. Since the transistors are connected in parallel, the combined current from all connected transistors is injected into the weaker output side, helping to balance the latch outputs by increasing the current on that side.

Transistor	**Size**	**Offset Compensation (Accumulated)**
0	120 nm x 1.3 μm	$\sim$ 0.5 mV
1	120 nm x 1.3 μm	$\sim$ 1 mV
2	120 nm x 1.3 μm	$\sim$ 1.5 mV
3	120 nm x 1.3 μm	$\sim$ 2 mV
4	120 nm x 1.1 μm	$\sim$ 2.5 mV
5	120 nm x 1 μm	$\sim$ 3 mV
6	120 nm x 1 μm	$\sim$ 3.5 mV

7	120 nm x 900 nm	$\sim 4\ mV$
8	120 nm x 900 nm	$\sim 4.5\ mV$
9	120 nm x 800 nm	$\sim 5\ mV$
10	120 nm x 700 nm	$\sim 5.5\ mV$
11	120 nm x 600 nm	$\sim 6\ mV$
12	120 nm x 600 nm	$\sim 6.5\ mV$
13	120 nm x 500 nm	$\sim 7\ mV$
14	120 nm x 500 nm	$\sim 7.5\ mV$
15	120 nm x 450 nm	$\sim 8\ mV$
16	200 nm x 450 nm	$\sim 8.5\ mV$
17	200 nm x 450 nm	$\sim 9\ mV$
18	200 nm x 400 nm	$\sim 9.5\ mV$
19	300 nm x 300 nm	$\sim 10\ mV$
20	300 nm x 300 nm	$\sim 10.5\ mV$
21	400 nm x 300 nm	$\sim 11\ mV$
22	400 nm x 300 nm	$\sim 11.5\ mV$
23	500 nm x 250 nm	$\sim 12\ mV$
24	600 nm x 250 nm	$\sim 12.5\ mV$

Table 4: Transistors size and offset compensation step

The layout of the parallel transistor approach is shown in **Figure 31**. Each side occupies 61 μm^2 , resulting in a total of 122 μm^2 for both sides.

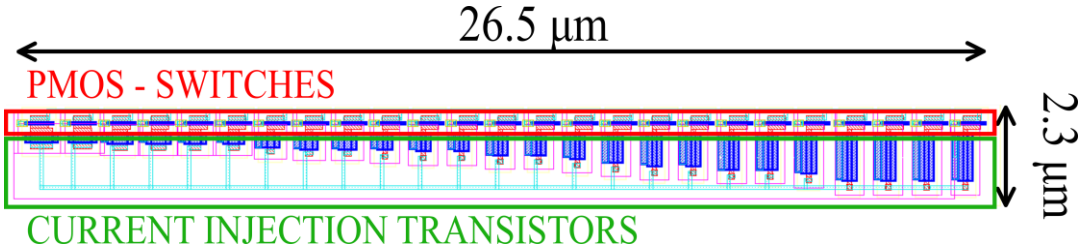


Figure 31: Layout Additional Parallel Transistors approach

Calibration Process

To verify the effectiveness of the calibration technique, two distinct calibration algorithms were implemented and simulated. The first algorithm referred to as the "fast method", prioritizes speed by completing calibration as soon as the first output transition is detected, using a reduced number of clock cycles; however, this comes at the cost of precision. This method was used in works (Tsirmpas, Kontelis, Souliotis, & Plessas, 2024; Jaiswal, et al., 2020; Lee, et al., 2020; Sharma, Srivastava, Hande, Sehgal, & Das, 2023).

When the differential input approaches the offset voltage, the outputs of the comparator present oscillations, as shown in **Figure 32**, where the differential output is compared for cases with and without noise. This behavior complicates calibration, as relying on the first output transition to signal calibration completion may lead to insufficient compensation. The initial transition could be noise-induced, with subsequent outputs returning to their previous state, failing to achieve proper calibration.

To mitigate the effects of the noise, the second algorithm, referred to as the "window-based method" is proposed. This method evaluates a predetermined number of outputs and analyzes whether the result alternates approximately evenly between the two comparator outputs. This minimizes the impact of noise and ensures that the calibrated offset voltage is as near to zero as possible.

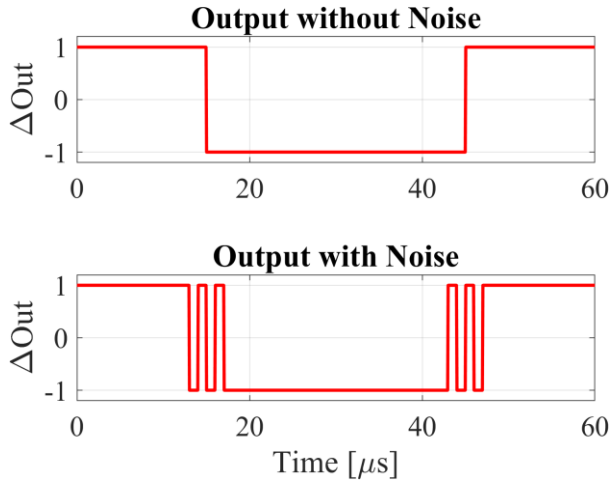


Figure 32: Noise Effect in the Comparator Output

The two algorithms are implemented in synthesizable Verilog code, enabling fabrication of the digital block. Performance is tested using the Analog-Mixed Signal (AMS) simulator in Virtuoso, which performs real-time co-simulation between the digital and analog components (Castaldo & Gibilaro, 2024). **Figure 33** illustrates the setup, where the Verilog Calibration Block inputs include: "Enable", which triggers the calibration; "Reset", which restores the comparator to its pre-calibration state; "outP" and "outN", which indicate the comparator's output state; and "Cal_CLK", a clock signal with the same frequency as the comparator clock but phase-shifted by 1/4 of the period to ensure stable output analysis.

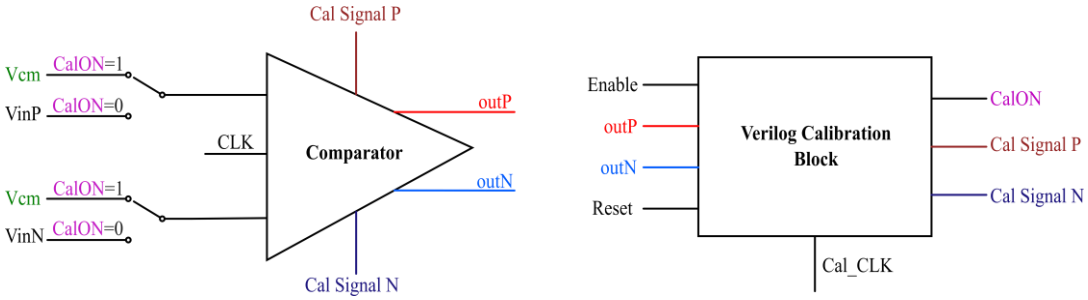


Figure 33: Simulation Setup of the Comparator with the Calibration Block

The outputs are: "CalON", which connects the comparator inputs to Vcm when high ("1") and to VinP and VinN when low ("0"); and "Cal Signal P" and "Cal Signal N", which activate the compensation technique. For the capacitive load method, these correspond to signals VcalP[0:11] and VcalN[0:11], activating transmission gates to connect calibration capacitors. In the charge pump method, they control the Calibration Unit clock, and in the parallel transistors method, they represent signals VcalP[0:24] and VcalN[0:24], which activate or deactivate the MOS switches.

In **Figure 34**, the flowchart of the fast algorithm is shown. This method analyzes the comparator outputs to identify the stronger side due to mismatch and subsequently activates the calibration mechanism. After each activation, the outputs are re-evaluated in the next clock cycle. If the output is the same as the previous one, the algorithm continues the calibration process. However, if the output changes, the algorithm considers that the calibration is complete.

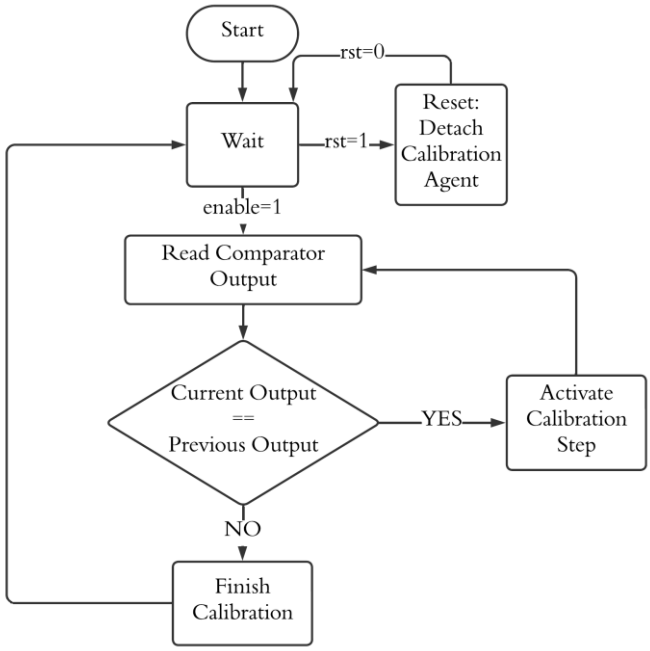


Figure 34: Fast Calibration Method Flowchart

Using the Fast Algorithm, which only checks if the current output matches the previous one, the capacitors are activated in order from the smallest to the largest compensation step. **Figure 35** shows an example of a Monte Carlo simulation with an offset of approximately 7 mV. At the start, an enable signal activates the calibration, and the "CalON" signal indicates that the process has started, connecting the comparator inputs to the same voltage, setting ΔVin to 0.

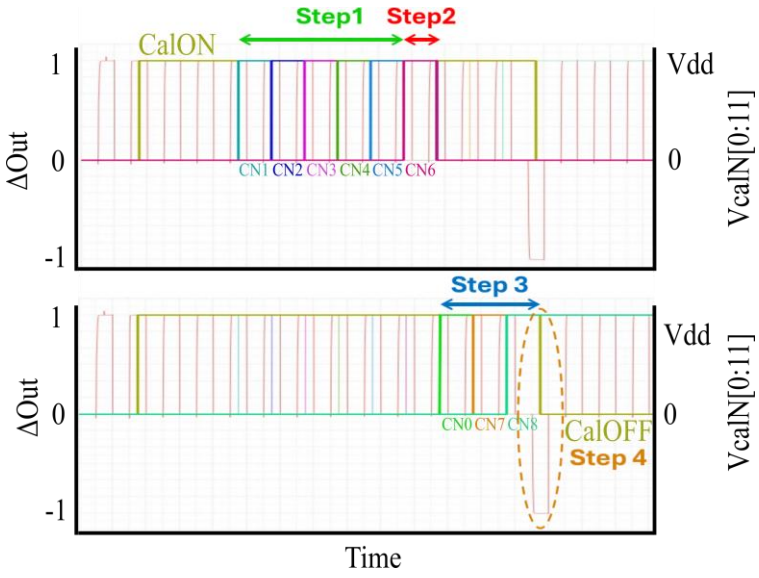


Figure 35: Fast Calibration Method Example

During Step 1, the smallest capacitors (CN1 - CN6) are connected sequentially. These capacitors are designed to compensate for offsets of up to 5 mV. However, since the offset exceeds this range, CN1 - CN6 capacitors are disconnected in Step 2. In Step 3, the larger capacitors are connected, starting with CN0 (MIM capacitor), followed by CN7, and finally CN8. In Step 4, when CN8 is connected, the output logic level reverses compared to the previous state, signaling that the calibration is complete. At this stage, "CalON" is deactivated, marking the end of the calibration process.

The flowchart in **Figure 36** describes the window-based algorithm that exploits the noise present in the circuit. In this method, a fixed number of output readings referred to as

"Window" is set, and the algorithm triggers the comparator and stores a count of the outputs for "Window" times. Afterward, it checks how many of these outputs are "1" and the algorithm verifies whether the total "Count" of 1's falls within a predefined range. This range is set to Window/2 $\pm$ 2. For example, if "Window" is set to 22, an acceptable range for "Count" would be from 9 to 13, as shown in the flowchart. If the "Count" is outside this range, the algorithm proceeds to the next calibration step and repeats the process until the "Count" falls within the desired range, indicating that the offset of the comparator is sufficiently low for the outputs to toggle between logic '1' and '0' due to noise fluctuations. At this point, the calibration is considered to be complete.

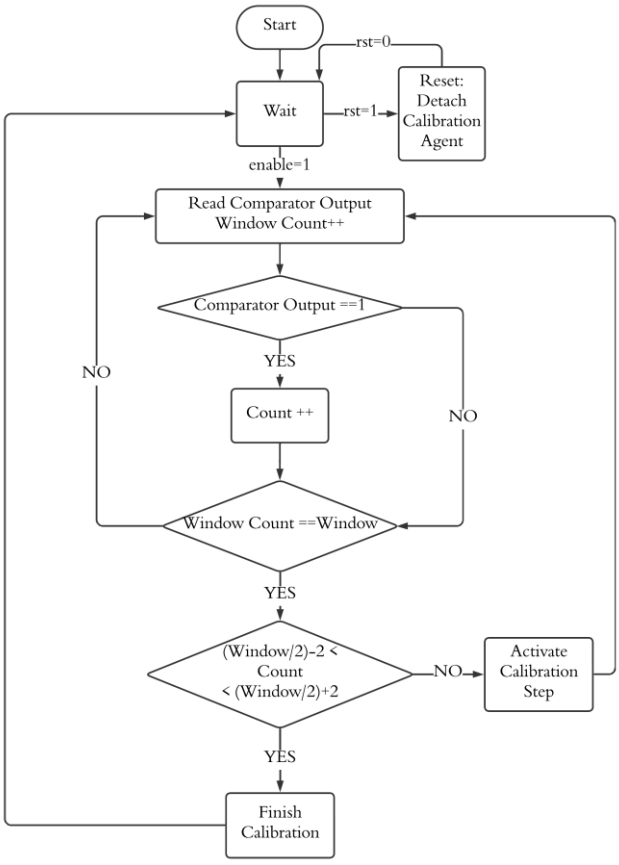


Figure 36: Window Calibration Method Flow Chart

This approach ensures that the algorithm checks for overcompensation, allowing a transition to a smaller step if necessary. The target is to speed up the calibration process by avoiding unnecessary trials with smaller capacitors when a larger offset needs correction.

Figure 37 shows one of the Monte Carlo simulations, where the initial offset is approximately 1.5 mV. In the calibration process, the "CalON" signal is activated to indicate the start of calibration. This connects the comparator inputs to the same voltage, creating the $\Delta Vin = 0\ mV$ condition. In the first window, the count shows outP = 1 occurring 22 times and outN = 1 occurring 0 times, indicating that the offset favors the outP node. This results in the decision to connect the VcalN[0:11] capacitors side. In the second window, the MIM capacitor (CN0) is connected, but after obtaining an outP = 1 count of 0 CN0 is disconnected due to offset overcompensation. The process then moves to smaller capacitors. In the third window, CN3 is connected, resulting in outP = 1 occurring 18 times, indicating further adjustment is needed. In the subsequent window, CN4 is connected, but the count drops to 7, indicating overcompensation again, so CN4 is disconnected. Finally, in the fifth window, the smaller capacitor CN1 is connected, resulting in an outP = 1 count of 12, which falls within the predefined range for calibration. The "CalON" signal is then deactivated, indicating that the calibration is complete.

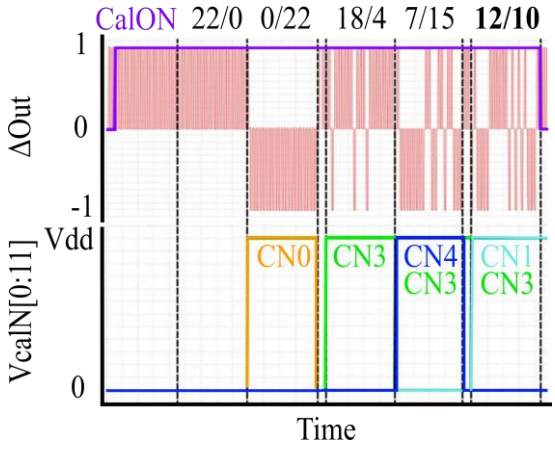


Figure 37: Window Calibration Method Example

For this specific offset, the useful capacitors were CN3 (providing approximately 1 mV compensation) and CN1 (approximately 0.5 mV compensation).

Simulation Results and Comparison

The two calibration algorithms were applied to the three calibration techniques. The comparator was simulated both before and after calibration for each approach using 1000 Monte Carlo simulations. To ensure consistency, these simulations followed the same setup as described in **Chapter "Simulation and Analysis"**. A comparison between pre- and post-calibration was conducted to evaluate how each calibration method impacts key performance metrics of the comparator. The metrics measured included offset voltage, the number of cycles required for calibration, the average energy consumed during calibration, energy per comparison, delay, input-referred noise, and the maximum frequency achievable by the comparator. These results provide insights into how each calibration method influences the comparator's efficiency, accuracy, and speed, allowing the identification of the most effective calibration strategy.

To analyze the offset results, **Figure 38** shows the offset calibration results for the comparator using three different methods: capacitive load (**Figure 38a**, **Figure 38b**, **Figure 38c**) , current injection by gate biasing (**Figure 38d**, **Figure 38e**, **Figure 38f**), and current injection through parallel transistors (**Figure 38g**, **Figure 38h**, **Figure 38i**). Each method is represented in three stages: before calibration, after fast calibration, and after window calibration.

In the "Before Calibration", **Figure 38** (**a, d, g**), a wide spread in offset values can be observed, as expected, with high standard deviations (σ).

Following, "Fast Calibration" histograms are presented in **Figure 38** (**b, e, h**), the offset distribution becomes narrower, indicating that the offset values are less spread out. The lowest σ of 0.452 mV is observed in the parallel transistors approach, although this method also has the highest mean offset. While this calibration reduces the variation, some spread remains.

The "Window Calibration" **Figure 38** (**c, f, i**) show the smallest offset distributions, with both lower mean and standard deviation values. This indicates that window calibration effectively minimizes offset variation, producing values close to zero. This calibration process achieves more accurate results than fast calibration, providing a more reliable offset correction. For applications requiring precise offset control, window calibration would be the preferred approach where the calibration time is not critical.

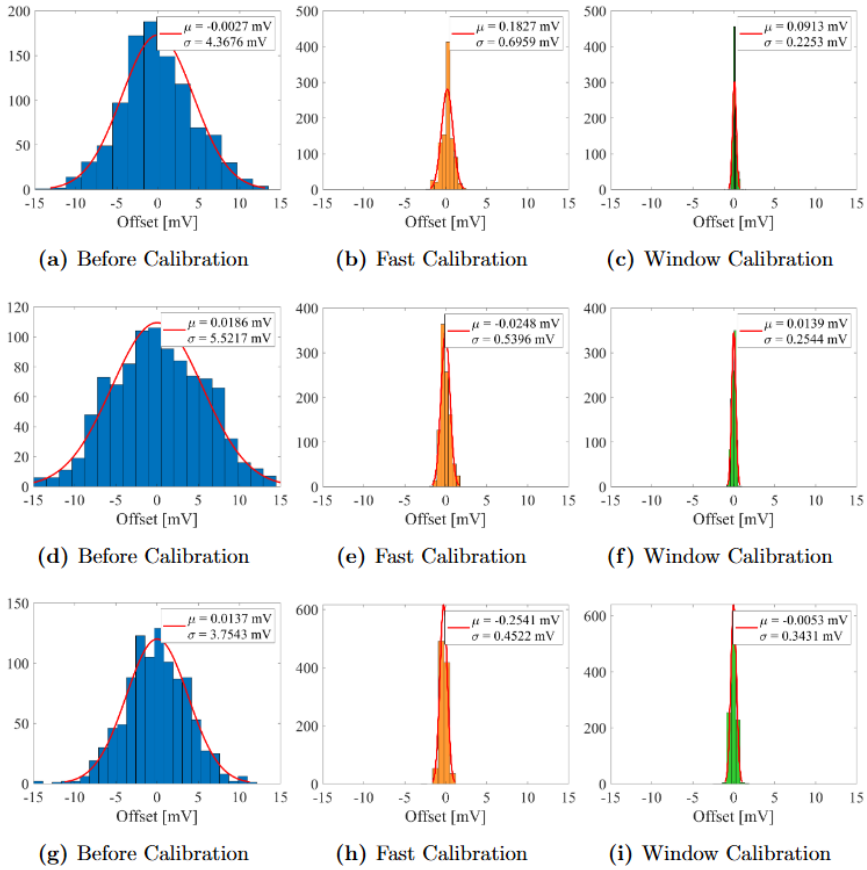


Figure 38: Offset calibration results. a), b), c) Capacitive Method. d), e), f) Current injection: Charge Pump. g), h), i) Current injection: Parallel Transistors

The analysis shows that the charge pump approach achieves the lowest σ in offset, indicating it provides the most precise calibration. However, this method relies on maintaining a stable voltage on a capacitor to polarize PMOS transistors, this approach is vulnerable to leakage over time. These leakage paths cause the stored voltage to gradually decrease, indicating the calibration has to be refreshed periodically to maintain accuracy.

The next best approach is the capacitive load method. Unlike the charge pump method, this method does not require periodic refreshing. The capacitors act as a load on the stronger side of the comparator, helping the calibration remain effective without the need for additional re-calibration.

After discussing offset voltage reduction as the primary goal, we can also analyze other metrics presented in **Table 5**.

An important factor is the number of cycles required to complete calibration. When employing the fast algorithm: the capacitive and parallel transistors techniques demonstrate the lowest cycle counts, with 9 and 10 cycles respectively, these are followed by the charge pump method which requires 15 cycles. In contrast, the window method requires a variable number of calibration cycles due to the iterative nature of the algorithm: the parallel transistors and capacitive techniques have the lowest cycle counts (156 and 166, respectively), while the charge pump technique demands significantly more cycles (310), nearly double with respect of other approaches. This increased cycle count could pose a limitation on the charge pump technique, as it consistently begins calibration from the lowest steps and progresses to the highest, extending the overall calibration time.

Regarding the average calibration energy per comparison, the capacitive load technique is the most efficient, requiring 0.175 pJ for fast calibration and 0.165 pJ for the window calibration algorithm. In contrast, the charge pump technique consumes the most energy, with

0.233 pJ for fast calibration and 0.202 pJ for window calibration. The parallel transistor technique demonstrates a modest performance, with 0.217 pJ for fast calibration and 0.216 pJ for window calibration. When considering energy consumption alongside the number of calibration cycles, the capacitive load method emerges as the most effective approach.

Energy values with no calibration applied are lowest for the charge pump technique (0.131 pJ at 1 mV), followed by the capacitive load technique (0.147 pJ at 1 mV), and the parallel transistors technique consuming the most energy (0.172 pJ at 1 mV). After calibration, energy consumption increases for all methods, with the current injection methods consuming more energy than the capacitive load technique. In terms of delay, the charge pump technique achieves the lowest delay, both with and without calibration. On the other hand, the parallel transistors technique has the highest delay after calibration (6.94 ns at ΔVin = 1 mV), making it less suitable for high-speed applications.

The energy-delay product (EDP) combines energy and delay to evaluate the trade-offs between the said magnitudes. The charge pump technique achieves the lowest EDP at ΔVin = 1 mV, with calibration (0.56 pJ·ns) and without calibration (0.44 pJ·ns), indicating high efficiency. The capacitive load technique also achieves a relatively low EDP without calibration (0.60 pJ·ns at ΔVin = 1 mV); however, after calibration, its EDP increases due to the longer delay, although it improves as ΔVin increases. In contrast, the parallel transistors approach has the highest EDP, making it less efficient when balancing energy consumption and speed.

In terms of noise, the levels before calibration are similar across all methods. After calibration, the capacitive load approach shows only a slight increase of 1 μV in noise, while the parallel transistors technique results in a noise reduction of 15 μV. The charge pump technique shows the highest noise increase after calibration (32 μV), which may be a concern for noise-sensitive designs.

Regarding maximum operating frequency, the charge pump method exhibits the highest frequency capability (107.7 MHz at ΔVin = 1 mV), making it the most suitable for high-speed applications. The capacitive load approach also supports a frequency of 61.3 MHz at ΔVin = 1 mV. The parallel transistors method achieves the lowest maximum frequency (28.37 MHz), which is a trade-off to achieve an accurate calibration of the offset voltage as it needs more transistors to provide a smaller calibration step but this increases the delay, lowering the maximum achievable frequency.

When considering area overhead, the charge pump method has a compact transistor area of 39 μm^2, making it more space-efficient. However, the MIM capacitors occupy the largest area (1266 μm^2). The capacitive load method uses a slightly larger area of 73 μm^2, with a MIM capacitor area (10.6 μm^2). The parallel transistors method requires the most space, with a total area of 122 μm^2.

All three techniques effectively reduce offset voltage, each with specific trade-offs. The charge pump method offers a better offset reduction with the lowest EDP and high speed at a requirement of periodic recalibration due to leakage. The parallel transistors method, while effective, shows the highest EDP and occupies the most area, making it less efficient in balancing energy, speed, and extra area occupancy. The capacitive load approach, while slower and with a higher EDP than the charge pump method, requires no maintenance after calibration, making it ideal for applications where low offset is a priority. Overall, the choice of method depends on the specific requirements for offset reduction, energy efficiency, speed, and area in the target application.

Compensation technique	**Capacitive Load**		**Current Injection (Charge Pump)**		**Current Injection (Parallel transistors)**	
Process [nm]	65		65		65	
Supply Voltage [V]	1.2		1.2		1.2	
Initial Offset Voltage [mV]	4.37		5.52		3.75	
Calibrated Offset [mV]	**Fast**	**Window**	**Fast**	**Window**	**Fast**	**Window**
	μ = 0.183 **σ** = 0.696	**μ** = 0.091 **σ** = 0.223	**μ** = -0.025 **σ** = 0.539	**μ** = 0.014 **σ** = 0.254	**μ** = -0.254 **σ** = 0.452	**μ** = -0.005 **σ** = 0.343
Calibration Periods	**μ** = 9 **σ** = 3	**μ** = 166 **σ** = 42	**μ** = 15 **σ** = 10	**μ** = 310 **σ** = 217	**μ** = 10 **σ** = 5	**μ** = 156 **σ** = 42
Calibration Energy [pJ]	0.175	0.165	0.233	0.202	0.217	0.216
Energy [pJ] w/out calibration	0.1474 @1mV 0.1469 @10mV		0.131 @1mV 0.130 @10mV		0.172 @1mV 0.167 @10mV	
Delay [ns] w/out calibration	4.09 @1mV 3.44 @10mV		3.39 @1mV 3.22 @10mV		7.36 @1mV 5.49 @10mV	
EDP w/out calibration	0.60 @1mV 0.51 @10mV		0.44 @1mV 0.42 @10mV		1.27 @1mV 0.92 @10mV	
Noise [μV]	364.6		359.8		361.1	
Energy [pJ] with calibration	0.165 @1mV 0.164 @10mV		0.207 @1mV 0.192 @10mV		0.211 @1mV 0.209 @10mV	
Delay [ns] with calibration	6.78 @1mV 4.03 @10mV		2.69 @1mV 1.84 @10mV		6.94 @1mV 4.29 @10mV	
EDP [pJ*ns] with calibration	1.12 @1mV 0.66 @10mV		0.56 @1mV 0.35 @10mV		1.46 @1mV 0.89 @10mV	
Noise [μV]	365.3		392.4		345.8	
fmax [MHz]	**μ** = 61.73 - **σ** = 10.5 @1mV **μ** = 97.63 - **σ** = 11.3 @10mV		**μ** = 107.7 - **σ** = 9.7 @1mV **μ** = 147.2 - **σ** = 8.3 @10mV		**μ** = 28.37 - **σ** = 7.8 @1mV **μ** = 54.74 - **σ** = 8.4 @10mV	
Area [μm2]	Transistors: **73** MIMCaps: **10.6**		Transistors: **39** MIMCaps: **1266**		**122**	

Table 5: Calibration Methods Characteristics Comparison

CONCLUSIONS

This work focused on designing a dynamic comparator and analyzing its characteristics through simulations and measurements. Dynamic comparators play a crucial role in circuits for applications such as Software-Defined Radio systems, IoT sensors, biosensors, and neuromorphic systems, where accurate results are essential for signal processing. A primary objective of this work was to enhance the comparator performance by reducing output errors caused by offset due to mismatches, employing calibration techniques to minimize offset voltage. The used design incorporates a floating inverter amplifier in the first stage, which reduces the comparator's sensitivity to variations in input common-mode voltage by creating an isolated voltage domain during comparisons.

Simulations were conducted to evaluate the overall performance of the comparator, focusing on offset, noise, energy consumption, and delay under different conditions. The analysis revealed an offset of 3.18 mV and an average noise level of 699.8 μV across input common-mode voltages. Energy and delay simulations provided insights into performance under different temperatures and supply voltage conditions. Temperature variations have minimal impact on delay and noise but increase energy consumption at higher temperatures. Reducing the supply voltage decreased energy consumption but led to higher delay and noise levels. These results highlight the trade-offs between energy efficiency and speed when adjusting operating conditions. Process variation analysis showed that in the Slow-Slow corner, the comparator consumed less energy with a higher delay, while in the Fast-Fast corner exhibited higher energy consumption and lower delay, demonstrating the influence of process variations on circuit behavior.

The fabricated comparator chips were tested to validate performance with a focus on noise and offset. The results showed that each chip exhibited similar behavior under a defined range of input common-mode voltage, confirming that the design is independent of this variation. As expected, each chip had a different offset voltage, with the highest measured offset at 6.78 mV. The measured noise was minimally affected by the variation in i-Vcm, ranging from 819 to 849 μV across all chips. However, noise measurement could have been affected due to the testing setup, with one chip showing a maximum noise value of 1076.89 μV. These results provide feedback on potential areas for improvement, particularly in applying mechanisms to reduce offset voltage.

Through a comparative analysis of three offset reduction techniques, the strengths and limitations of each method were evaluated in terms of precision, calibration time, and energy. The techniques were tested for their impact on the comparator's energy consumption, delay, and noise, both before and after calibration, with their area impact assessed through layout designs. Each technique presented trade-offs: the charge pump method offered the best energy-delay product, but capacitor leakage over time is a drawback that limits its long-term accuracy. The capacitive load approach performed best overall, reducing offset to 0.223 mV with the window method, without a recalibration requirement. While the exhibited EDP was an improvement over the parallel transistors method, it was still surpassed by the EPD result of the charge pump method. The combination of MIM and NMOS capacitors enabled a reduced silicon area occupancy, and provided precise calibration steps without the need for extra NMOS capacitors, enhancing both area efficiency and calibration precision. Additionally, the window calibration method was demonstrated to be more effective than the fast method found in the reviewed works, improving offset reduction across all three techniques.

The calibration algorithms were implemented in Verilog, and AMS simulation enabled real-time co-simulation and precise analysis of the interaction between the digital and analog blocks. This approach validated the feasibility of fabricating the digital calibration block and proved its effectiveness in controlling the offset calibration circuits.

This work provides specific design strategies and modifications for dynamic comparators that improve accuracy while maintaining a compact area, addressing critical requirements for their targeted applications. The proposed approaches achieve enhanced offset reduction without compromising energy efficiency or delay performance. Future research could focus on further noise reduction and improving energy and delay performance.

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