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Non-Volatile Content-Addressable Memory for Energy-Efficient & High Performance Search and Update Operations

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Non-Volatile Content-Addressable Memory for Energy-Efficient & High Performance Search and Update Operations

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DEDICATORIA

To my parents, who always encouraged me to get a Masters Degree, this work is your fault.

RESUMEN

Dispositivos emergentes como los “double-barrier magnetic tunnel junction” (DMTJ) son candidatos prometedores para enfrentar problemas como el “muro de memoria” y “muro de potencia” de los sistemas informáticos modernos. Los DMTJ ofrecen altas velocidades de escritura y lectura, gran escalabilidad e integración con tecnología CMOS. Por ende son altamente considerados para sistemas informáticos centrados en la memoria, como las “Content Addressable Memories” (CAM), que han tenido éxito comercial en sistemas de redes de alta velocidad. Este trabajo presenta una celda de memoria CAM basada en dispositivos MTJ no volátiles (NV-CAM). Nuestro diseño presenta operaciones de búsqueda y escritura a alta velocidad y bajo consumo. Esto permite utilizarla en aplicaciones que requieren un elevado número de búsquedas/escirturas, como los procesadores asociativos. La celda CMOS/DMTJ propuesta se diseñó utilizando una tecnología CMOS comercial de 65nm y un modelo compacto DMTJ escrito en Verilog-A. A través de una evaluación de la celda mediante simulaciones Montecarlo se obtienen figuras de mérito competitivas en comparación con el estado del arte. Para obtener comparaciones justas, se caracterizaron otras celdas presentadas en la literatura utilizando la misma tecnología y modelo de dispositivo. Nuestra NV-CAM presenta una mejora en los retardos de búsqueda y escritura de alrededor del 75% y 71% respectivamente..

Palabras clave: Content Addressable Memory, CAM, CAM no volátil, unión túnel magnética de doble barrera, DMTJ.

ABSTRACT

Novel devices such as the double-barrier magnetic tunnel junction (DMTJ) are promising candidates to address the current “Memory Wall” and “Power Wall” challenges in modern computing systems. DMTJs feature high write/read speeds, great scalability and integration with CMOS. As such, they are often considered for memory-centric computing systems like Content-Addressable Memories (CAM), which provide a highly parallel in-memory matching operation that has found commercial success in high-speed network systems. This work presents a non-volatile content addressable memory (NV-CAM) based DMTJ technology. Our design features energy-efficient, high performance search and update operations. This enables applications that require a high number of searches/updates, such as associative processors. The proposed CMOS/DMTJ hybrid cell was designed using a commercial 65nm CMOS technology and a Verilog-A based DMTJ compact model. Evaluation of the cell through Montecarlo simulations produce competitive figures of merit when compared to the state of the art. For the sake of fair comparisons, other cells presented in literature were characterized using the same transistor technology and device mode. Our NV-CAM presents an improvement in search and update delays of about 75% and 71% respectively..

Key words: Content-addressable memory, CAM, Non-Volatile CAM, double-barrier magnetic tunnel junction, DMTJ.

Contents

Contents **8**

List of Figures **10**

List of Tables **11**

1 List of Abbreviations **12**

2 Introduction **15**

2.1 Introduction & Motivation 15

2.2 Conventional & Emerging Non-Volatile Memory Technologies For Content-Addressable Memories 16

2.2.1 Resistive Random Access Memory (ReRAM) 17

2.2.2 Phase Change Memory (PCM) 19

2.2.3 Ferroelectric Field Effect Transistor (FeFET) 20

2.2.4 Magneric Random Access Memories (MRAM) 21

Single-Barrier Magnetic Tunnel Junctions (SMTJ) 22

Double-Barrier Magnetic Tunnel Junction (DMTJ) . . . 23

2.3 Organization of the Thesis 25

3 Background **26**

3.1 Content Addressable Memories 26

3.1.1 CMOS CAMs 28

3.1.2 Non-Volatile CAMs Based on STT-MRAM Technology . 30

Voltage Divider Structures 31

Latch Based Structures 32

3.2 Non-Voltatile CAMs Application Space 32

4 Non-Volatile Content-Addressable Memory (NV-CAM) Design 36

4.0.1 Overview of the MTJ Compact Model 36

4.1 17T4MTJ Cell Structure 37

4.2 Cell Operation 39

4.2.1 Write Operation 39

4.2.2 Search Operation 41

4.3 Performance Analysis 44

5 Alternative NV-CAM Cell Architectures 51

5.1 Overview of Alternative Cells 51

5.2 9T2MTJ 51

5.2.1 Cell Schematic and Operating Principles 51

5.2.2 Design and Discussion 54

5.3 10T4MTJ 55

5.3.1 Cell Schematic and Operating Principles 55

5.3.2 Design and Discussion 59

5.4 10T2MTJ 60

5.4.1 Cell Schematic and Operating Principles 60

5.4.2 Design and Discussion 63

5.5 Performance Comparison 64

6 Conclusion 67

6.1 Conclusion 67

6.2 Research Output 68

List of Figures

2.1 Emergent Non-Voltatile Devices 17
2.2 Double Barrier MTJ 24

3.1 CAM Block Diagram 27
3.2 CAM Taxonomy 28
3.3 NOR CMOS Cell and Matchline 29
3.4 NAND CMOS Cell and Matchline 30
3.5 2T2MTJ Circuit Diagram 31
3.6 STT–MRAM NV-CAM Top Level Diagram 32
3.7 AP Architecture Diagram 34

4.1 17T4MTJ Circuit Diagram 38
4.2 17T4MTJ Write Circuit Diagrams 39
4.3 17T4MTJ Write Timing Diagram 40
4.4 17T4MTJ Search Circuit Diagrams 42
4.5 17T4MTJ Search Timing Diagram 43
4.6 17T4MTJ cell Layout 45
4.7 Hybrid 3D CMOS/MTJ Process 46
4.8 17T4MTJ Performance Evaluation Setup 47
4.9 17T4MTJ cell Performance Evaluation 48

5.1 9T2MTJ Circuit Diagram 52
5.2 10T4MTJ Circuit Diagram 56
5.3 10T2MTJ Circuit Diagram 61

List of Tables

4.1 DMTJ device parameters 37
4.2 MAB data encoding 38
4.3 17T4MTJ cell write operations 41
4.4 17T4MTJ cell search operations 44
4.5 17T4MTJ cell search results 49
4.6 17T4MTJ cell write results 50

5.1 9T2MTJ cell write operations 53
5.2 9T2MTJ cell search operations 53
5.3 9T2MTJ transistor sizes 54
5.4 10T4MTJ cell write operations 57
5.5 10T4MTJ cell search operations 58
5.6 10T4MTJ transistor sizes 59
5.7 10T2MTJ cell write operations 61
5.8 10T2MTJ NV-CAM cell search operations 62
5.9 10T2MTJ transistor sizes 63
5.10 NV-CAMs Figures of merit 65

Chapter 1

List of Abbreviations

ACAM	Analog Content Addressable Memory
ACS	Associative Computing Systems
AP	Associative Processor
BCAM	Binary Content Addressable Memory
BEOL	Back End Of Line
CAM	Content Addressable Memory
CBRAM	Conductive Bridging Random Access Memory
CCL	Cross–Coupled Latch
CL	Comparison Logic
DMTJ	Double Barrier Magnetic Tunnel Junction
DRAM	Dynamic Random Access Memory
DSA	Differential Sense Amplifier
EC	Coercive Electric Field
FDSOI	Fully–Depleted Silicon On Insulator
FE	Ferroelectric Layer
FeFET	Ferroelectric Field Effect Transistor

FEOL Front End Of Line

FIMS Field Induced Magnetic Switching

FL Free Layer

FM Ferromagnetic Layer

FOM Figures Of Merit

FPGA Field Programmable Gate Array

HDD Hard Disk Drive

HKMG High–K Metal Gate

HPC High Performance Computing

HRS High Resistance State

IL Interfacial Layer

IMC In–Memory Computing

LRS Low Resistance State

MAB Memory Array Block

MFIS Metal–Ferroelectric–Insulator–Semiconductor

MFS Metal–Ferroelectric–Semiconductor

ML MatchLine

MLC Multi–Level Cell

MLS Match-Line Sensing Network

MLSA Matchline Sense Amplifier

MRAM Magnetic Random Access Memory

MSN Matchline Switching Network

MTJ Magnetic Tunnel Junction

MW	Memory Window
NVCAM	Non-Volatile Content Addressable Memory
NVM	Non-Volatile Memory
OxRAM	Metal Oxide Resistive Random Access Memory
PCM	Phase Change Memory
PDF	Probability Density Function
PDK	Process Design Kit
PL	Pinned Layer
PLA	Programmable Logic Array
PU	Processing Unit
PUF	Physically Unclonable Function
ReRAM	Resistive Random Access Memory
SA	Sense Amplifier
SER	Search Error Rate
SIMD	Single–Instruction–Multiple–Data
SN	Search Logic Network
SOT	Spin Orbit Torque
STT	Spin Transfer Torque
TCAM	Ternary Content Addressable Memory
TMR	Tunnel MagnetoResistance
VCMA	Voltage Controlled Magnetic Anisotropy
VDN	Voltage Divider Network
WER	Write Error Rate

Chapter 2

Introduction

2.1 Introduction & Motivation

Computing systems based on Von Neumann architecture present a data-transfer bottleneck, caused by the increasing disparity between the processing units and the relatively slower access times of main memory. This is often referred to as the "memory wall" [1]. Moore's Law has further aggravated this bottleneck throughout the past decade. The increase in transistor density, accompanied by the exponential rise in leakage current due to scaling down voltage and feature sizes in advanced technology nodes, has created critical power dissipation challenges that threaten to exhaust the capabilities of conventional cooling solutions, a problem known as the "power wall" [2].

In–Memory computing (IMC) rises as an alternative to overcome the "memory wall", operating in-situ, employing the memory cells for storage and processing [3], without the need for data movement. One of such IMC approaches are Content Addressable Memories (CAMs), which provide a highly parallel in-memory matching operation that has found commercial success in high-speed network systems [4]. CAMs are non-random access memory structures where an input query word is looked into the entire memory content, signaling the matching data [5]. CAMs implement two basic operations. The write operation stores/updates information in the memory array, while the search operation compares the input query word to every stored entry/word simultaneously, obtaining the matching address or addresses during a single clock cycle. CAMs show promising characteristics for a diverse range of applications such as finite

state machines, pattern matching, and associative computing [6].

While novel system architectures based on conventional CMOS technology can partially alleviate the "memory wall" and "power wall" problems, they still require novel devices to fully address these challenges. Non-volatile emergent memory devices such as the STT-MRAM feature zero standby leakage, high write/read speeds, great scalability and integration density [7]. As such, they are considered promising candidates to realize memory-centric computing systems [8].

2.2 Conventional & Emerging Non-Volatile Memory Technologies For Content-Addressable Memories

Non-Volatile CAMs (NV-CAMs) can be built from various emerging non-volatile memory (NVM) devices. These devices include two-terminal switching elements such as Phase Change Memories (PCM), Resistive Random Access Memories (ReRAM) and Magnetic Random Access Memories (MRAM), as well as the three terminal Ferroelectric Field Effect Transistor (FeFET). Ongoing research on these technologies is driven by the potential to offer significant advantages over traditional memory solutions such as transistor-based SRAM and non-volatile Flash. One key advantage of these emerging NVMs is scalability, which allows for the development of high-density memory architectures such as crossbar arrays [9].

PCM, ReRAM, and MRAM devices are fabricated using the back-end of line (BEOL) processes, where the devices are integrated between metal layers. This method of integration facilitates compatibility with existing CMOS technology, a factor which is crucial for their effective application in IMC architectures [10], [11], [12]. On the other hand, the FeFET is fabricated using front-end-of-line (FEOL) processes, which involve different material requirements. Hafnium oxide (HfO_2)-based FeFET devices exhibit full CMOS compatibility due to the the massive use of HfO_2 in the fabrication of high-k metal gate (HKMG) MOSFETs introduced by Intel in the 45nm node back in 2007 [13].

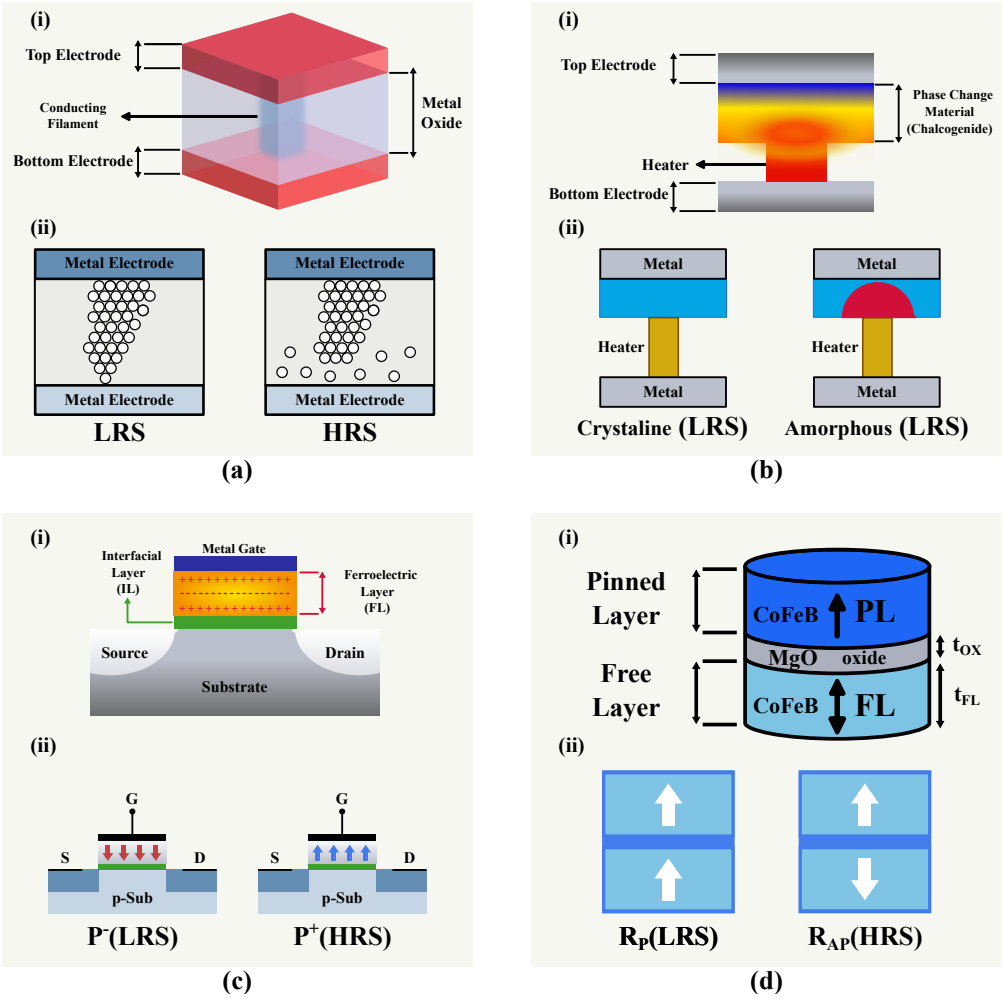

Figure 2.1: Promising emergent non-volatile storage devices. (a) Resistive Random Access Memories, (b) Phase Change Memories, (c) Ferroelectric Field Effect Transistor, and (d) Magnetic Tunnel Junction.

2.2.1 Resistive Random Access Memory (ReRAM)

ReRAM research began in the 1960s with the study of the conductive properties of numerous metal oxides, but the potential of these devices as a scalable alternative to existing volatile and NV memories finally picked up during the 2000s [14]. For the past 20 years, ReRAMs have been studied for several applications including in-memory computing [15], cryptography, Physically Unclonable Functions (PUFs) [16], and neuromorphic circuits [17]. Resistive memory technologies have been developed by industrial players for high-density standalone memories such as SandDisk's 32Gb memory device integrated with 24nm technology [18]. Additionally, Panasonic [19], Intel [20] and TSMC [21] have

showcased ReRAM integration as an embedded non-volatile memory (eNVM) alternative.

Although all of the devices discussed in this section are resistive in nature, the term ReRAM is typically used for insulator-based stacks with a defect-based switching mechanism [14]. The structure of a typical ReRAM cell is shown in Fig. 2.1 (a), and consists of an oxide layer sandwiched between two metal contacts. The oxide acts as an insulator, resulting in a high resistance across the ReRAM cell. A localized conductive filament is used to store the state of the device. When the filament is fully set, it forms a path that connects the top and bottom metal electrodes, corresponding to a Low Resistance State (LRS). On the other hand, if part of the filament is destroyed, the ReRAM is in a High Resistance State (HRS).

According to the type of defect used in the switching media, the device is classified into an Oxide ReRAM (OxRAM) or Conductive Bridging ReRAM (CBRAM). ReRAM switching is based on reduction-oxidation (redox) processes caused by fast-moving ions like oxygen vacancies in the case of OxRAM and highly diffusive metal ions like copper or silver in the case of CBRAM.

To obtain a working device, every cell has to undergo a process called FORMING in which the filament is created by applying a high voltage. This process constitutes a practical limitation for integration with different selector devices (like CMOS transistors), since the FORMING voltage may be too high for some technology nodes [14]. Once the filament is created, the cells can switch between the LR and HR states by recreating (SET) and breaking (RESET) the conductive path.

In terms of performance, the speed of the set/reset operation has been shown to span the $10ns$ - $100\mu s$ range with a typical endurance of 10^6 cycles [9]. The dielectric layer is progressively damaged during switching operations, causing an eventual failure due to dielectric breakdown. ReRAM devices are also limited by the switching current (usually greater than $10\mu A$) as data retention is heavily degraded at lower values, resulting in room temperature data loss within seconds [14].

2.2.2 Phase Change Memory (PCM)

Phase change memory research began in 1968 when a fast, reversible switching effect was observed in $Si_{12}Te_{48}As_{30}Ge_{10}$ (STAG) material compositions [22]. However, difficulties due to device degradation and instability slowed down progress. PCMs exploit the phase change properties of chalcogenide glasses, and new alloys like GeTe-Sb_2Te_3 [23] led to renewed interest in the technology from the early 2000s [24]. Academic literature on phase change memories has focused on various applications including its use as a storage class memory replacement [9], content addressable memories [25] and neuromorphic systems [17]. In the last decade, PCM technology has also been adopted by the industry with Micron announcing massive production in 2012 [26], and Samsung producing an 8 Gbit chip in 20nm technology [27].

In a PCM cell, the crystal switches between two states (phases); an amorphous state (HR phase) where the resistance is high, and a polycrystalline state (LR phase) that shows a low resistance. The structure of a typical PCM cell is shown in Fig. 2.1 (b). The phase change material, typically a Chalcogenide glass, is connected to a metal electrode on one side, and a resistive heating element (metal heater) on the other side. The heater is connected to a second metal electrode, and it is activated by sending a current into the device.

To switch between states, a voltage pulse is applied. To write a '0' (RESET) the cell receives a short high-voltage pulse heating the crystal and causing it to switch from a polycrystalline state to an amorphous state. The reverse process of writing a '1' (SET) requires a long low amplitude pulse that causes the material to revert to a polycrystalline state. The RESET process consumes high power (and energy) while the longer SET process limits the writing speed of the cell [9]. In addition to the extreme states, it is possible to cause the cell to switch to several intermediate stages, allowing the storage of multiple bits per cell in what is called a multi-level cell (MLC) [24].

In terms of performance, PCM memories can be compared to Dynamic Random Access Memories (DRAM) and SRAM. When compared to S/DRAM, PCMs feature much slower latency with writing speeds typically above the $100ns$ and a limited endurance in the 10^6-10^9 range [9]. PCMs also feature a higher write energy than other technologies including magnetic Hard Disk

Drives (HDDs) and NAND Flash [24]. Reductions in write latency and energy consumption are active areas of research, and while individual devices have been shown to achieve fast $25ns$ cycles with an endurance up to 10^{12}, low $10\mu A$ RESET current and 10 year data retention [22], arrays of PCMs still need to catch up.

2.2.3 Ferroelectric Field Effect Transistor (FeFET)

Research on ferroelectric materials used for modulating the conductivity of a semiconductor began in Bell Labs in 1957 [28]. In 1974 the first Metal–Ferroelectric–Semiconductor (MFS) transistor was presented using bismuth titanate ($Bi_4Ti_3O_{12}$) deposited on silicon [29]. However, the development of suitable devices was hindered by the lack of scalable ferromagnetic dielectrics, gate leakage, low data retention, and demanding integration [9],[28]. Other technologies with similar structures such as the floating-gate transistor saw much greater adoption. Finally, in 2011, evidence for ferroelectric properties in SiO_2 (silicon oxide) doped HfO_2 was discovered [30], leading to the development of promising scalable FeFET devices. In 2016, one–transistor (1T) FeFET-based eNVM arrays in NOR and AND configurations were demonstrated in a $28nm$ HKMG process, showing data retention up to $250°C$ with an endurance of 10^5. Later, in 2017, a 32 Mbit FeFET eNVM was reported with $10ns$ switching speed, 10^5 cycle endurance, and data retention up to $300°C$ [31]. Applications for FeFETs also include neuromorphic computing [28], and IMC circuits, particularly NV-CAMs [32], [33].

The simplest FeFET structure is the Metal–Ferroelectric–Semiconductor (MFS), in which a layer of ferroelectric material is deposited over the transistor channel. However, due to integration drawbacks, a buffer layer was added leading to the preferred Metal–Ferroelectric–Insulator–Semiconductor (MFIS) structure. Fig. 2.1 (c) shows the structure of an MFIS FeFET cell. The ferroelectric layer (FE) is used to store information in the form of two equivalent polarization states P^- and P^+, which remain stable even when no electric field is being applied. The states are associated with the presence of permanent dipoles within the cell [28]. The interfacial layer (IL) is used to separate the FE and the transistor channel. The main functions of this layer include preventing the

diffusion of elements between the FE layer and the substrate, enabling deposition and growth of the FE layer, and providing a good channel-interface to maintain high transistor performance [28].

To switch between polarization states, a field larger than the coercive electric field (EC) is applied to the cell. The polarized FE layer induces a field in the FET channel due to the polarization charge, resulting in a change in threshold voltage (v_{th}). For an n-channel device, when polarization points downwards, minority carriers are attracted to the channel increasing conductivity and causing a low threshold voltage (Erased state). Meanwhile, if polarization is pointing upwards, minority carriers are repelled and a high threshold voltage appears (Programmed state). The threshold difference between the erased and programmed state is known as the Memory Window (MW). Similar to PCMs, FeFETs programmed/erased using incremental pulses have been shown to achieve discrete, intermediate threshold voltage levels enabling MLC capabilities [34].

In terms of performance, HfO_2 cells show great scalability, but suffer from a limited endurance in the 10^4 to 10^5 range [9]. Data retention problems occur due to the presence of a depolarization field caused by the non FE layers of the device [28]. To mitigate this field, high EC values are preferred, but these lead to a faster degradation of the IL layer from repeated program and erase cycles. Preventing IL degradation without affecting data retention is a current area of research [35].

2.2.4 Magneric Random Access Memories (MRAM)

MRAM devices are one of the most promising NVM technologies offering a better performance in switching speed, write energy, data retention, and endurance compared to the other technologies discussed in this section [8]. Spin Transfer Torque MRAM (STTMRAM) devices in particular feature sub $10ns$ writing speeds with above 10^{12} cycling endurance [9], sparking interest in research for applications such as cache memories [36], neural networks [37], hardware accelerators [8], and cryptography [38], amongst others. Industry-led research has shown high-density integration architectures like the DMTJ crossbar array presented by Samsung in 2022 [39]. Additionally, STT-based

devices have been successfully commercialized by Everspin [40], selling STT-based DDR products for data-centers. Intel [41], and Global Foundries [42] have also began to release STT-MRAM products with a focus on IoT.
MRAMs are based on spintronics, which refers to technologies that use the spin of electrons and its associated magnetic moment as state variables in devices [43]. The basic unit device of MRAM is the Magnetic Tunnel Junction (MTJ).

Single-Barrier Magnetic Tunnel Junctions (SMTJ)

The MTJ, or single-barrier MTJ (SMTJ), is a multilayer nano-pillar structure consisting of a stack of two ferromagnetic (FM) layers separated by a non-magnetic layer as shown in Fig. 2.1 (d). The insulating layer works to magnetically decouple the ferromagnetic layers, and must be thin to allow electrons to tunnel through the barrier when a sufficient voltage is applied. Magnetic anisotropy determines the directional dependence of the magnetic material. If the FM layers are aligned in parallel to the insulating layer the device is an in-plane MTJ (iMTJ), otherwise; the alignment is perpendicular (pMTJ). pMTJs (Fig.2.1 (d)) have a lower switching current and more reliable switching [44].
The operating principles of an SMTJ cell are as follows. One of the FM layers, called the Pinned Layer (PL) has a fixed magnetic orientation. The other FM, called the Free Layer (FL), is able to switch between a parallel (P) and anti–parallel (AP) state with respect to the PL. When the layers are in P configuration the SMTJ shows a low resistance value, i.e., RP; otherwise, if the layers are anti–parallel, the device has a higher resistance, i.e., RAP. The change in resistance is explained by the majority and minority spins of each layer. If both layers are parallel, electrons with majority spin in one FM layer can tunnel easily to the majority states of the other layer, while in the AP case majority and minority spins from one layer tunnel to fill minority and majority states of the other [43]. The key performance indicator is called the Tunnel MagnetoResistance (TMR), defined as

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{2.1}$$

In 1975, the first device with a TMR of 14% was reported using a Fe/Ge/Fe

structure [43]. Current devices use CoFeB ferromagnetic layers separated by a magnesium oxide (MgO) insulating layer. Commonly TMR values are in the 100% to 250% range, like Samsung's [45] integrated STT-MRAM arrays in $28nm$ fully–depleted silicon–on–insulator (FDSOI) processes which can achieve TMR values of 220%. The highest-to-date room temperature TMR is 604% [43].

The magnetic orientation of the free layer can be switched using different mechanisms. The first method is Field Induced Magnetic Switching (FIMS), where a current passing through orthogonal write lines produces an external field that would switch the SMTJ from P to AP and vice-versa. FIMS brought several drawbacks such as half-selectivity problems, high power consumption ($I_{write} \geq 10mA$), and low density [43]. In 2004, Spin Transfer Torque (STT) was demonstrated experimentally for the first time [44]. Writing in STT devices is done by applying a bidirectional current through the junction. According to the direction of the current, flowing electrons are spin-polarized by the pinned layer, and their momentum is transferred to electrons in the free layer. The torque generated by this interaction can change the magnetic orientation of the free layer if it is strong enough, which occurs when a critical current I_{C0} is applied to the SMTJ.

The main challenge for STT–MTJs is the reduction of the critical current to improve switching energy and speed. Additionally, exposition to high voltages for long write pulses significantly degrades endurance [46]. The STT is larger when the magnetic moments are near anti-parallel than near parallel [44], resulting in an asymmetric value for the critical switching current. To reduce the critical switching currents, an additional PL is included in the MTJ stack. This device is introduced hereafter.

Double-Barrier Magnetic Tunnel Junction (DMTJ)

The Double Barrier Magnetic Tunnel Junction (DMTJ) structure increases the switching efficiency of the STT mechanism by introducing a second pinned layer as shown in Fig. 2.2. The three FM layers are separated by two thin oxide layers $oxide_T$ (Top) and $oxide_B$ (Bottom). The bottom layer (PLb) has a magnetic orientation antiparallel to the top layer (PLt) resulting in one

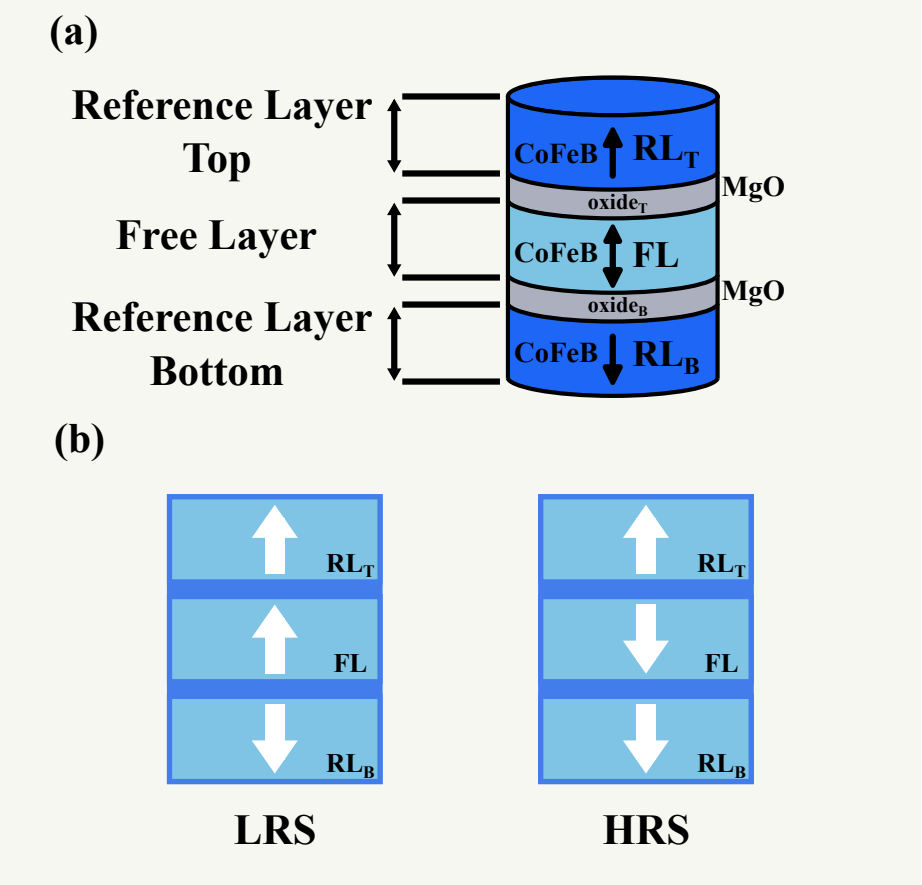

Figure 2.2: Double Barrier Magnetic Tunnel Junction (DMTJ). (a) Device structure. (b) Device states.

junction always being in AP state, reducing the total TMR of the device. In exchange, the critical switching current I_{C0} is reduced up to a factor of 10 [44], and becomes equal for both $P \rightarrow AP$ and $AP \rightarrow P$ transitions.

Finally, STT methods introduce a stochastic nature to DMTJ/SMTJ switching. Initially, when a write current is just applied, the magnetic orientations of all layers (PLt, PLb, FL for DMTJs) are collinear, and the resulting torque is zero. For STT to take effect, a miss alignment caused by thermal fluctuations is required, which introduces a random wait time before switching [43]. Therefore, to ensure a low Write Error Rate (WER), the write current must be applied for a longer time than the ideal device switching time. Additionally, as DMTJs (thus I_{C0}) scale down, using the same current path during the write

and read operations increases the risk of overwriting stored data. For these reasons, alternative switching mechanisms for both SMTJs and DMTJs are being studied. Notable candidates are Spin-Orbit Torque (SOT) and Voltage Controlled Magnetic Anisotropy (VCMA) [8].

2.3 Organization of the Thesis

This thesis studies the use of STT-MRAM devices in designing Non-Volatile CAMs for IMC architectures that feature a high frequency of search and update operations. The rest of this work is organized as follows: Chapter 3 presents the required background to understand the principles of Non-Volatile CAMs (NV-CAMs). Chapter 4 presents the principles and evaluation of a high–performance, reliable STT–MRAM based NV-CAM design. Chapter 5 presents a comparative performance analysis with other STT–MRAM based cells found in the literature. Finally, Chapter 6 summarizes the thesis and presents the research output of this work.

Chapter 3

Background

3.1 Content Addressable Memories

Fig. 3.1 shows the block diagram of the CAM architecture. The memory array consists of $m \times n$ CAM bit cells arranged in m words of length n. Each word is connected to a word-line WL_j and a matchline ML_j. Search-lines SL_i and SLN_i run vertically through each column n. The write operation is controlled by the WLs, and data is loaded through the bit-lines (not shown). For the search operation, the word in the Search data Register is loaded into the search-lines. The outputs on the matchlines are sensed by the Matchline Sense Amplifiers (MLSA) to determine whether the result is a match or mismatch. The number of bits in a CAM word is usually in the range of 36 to 144 bits [5].

Fig. 3.2 shows an overview of the classification of CAMs based on the match-line type, data encoding, match type, and memory type. There are two types of matchline structures in CAMs: NOR and NAND matchlines. NOR match-lines feature a high search speed, at the cost of increased energy consumption. NAND matchlines feature a more energy-efficient search but suffer from low noise margins, and a quadratic increase in delay for every extra cell in the CAM word [5].

CAM cells can be designed to store different types of data. Binary CAMs (BCAMs) consist of arrays of cells made with a single memory device (e.g., one SRAM cell, or one ReRAM), and can store and match against words containing only '1's and '0's. Ternary CAMs (TCAMs), are able to store an additional

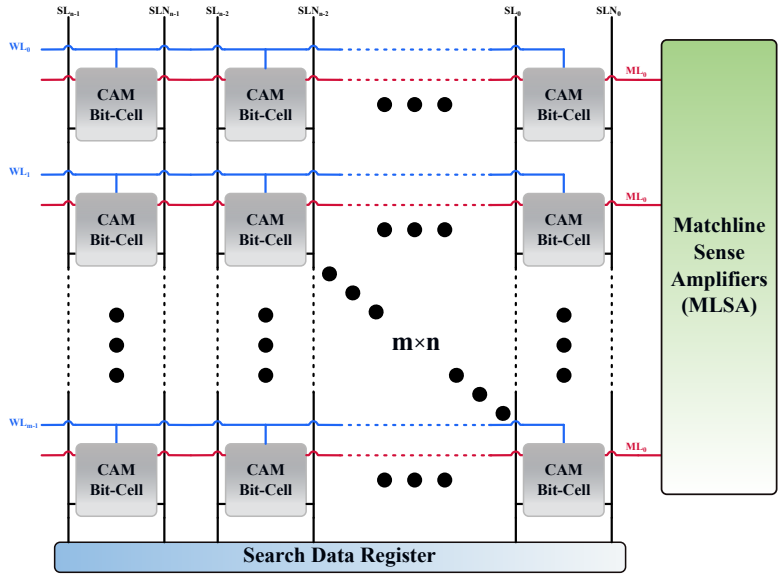

Figure 3.1: Content Addressable Memory (CAM) block diagram.

value, i.e., 'X'. This value acts as a *don't care*, that matches against both a '0' and a '1'. This feature increases data density, and enables searches with partial matches, which are heavily featured in applications like packet forwarding in network routers [5]. TCAM cells require two bits (memory devices) per cell to store the extra state. In cases where a TCAM is needed, but unavailable, BCAMs can be repurposed by using two cells to encode each symbol at the cost of halving the original capacity [47]. Analog CAMs (ACAMs) use the programmable analog characteristics of emergent memory devices to compare an analog search query with analog ranges encoded in the CAM cells [48]. Some ACAMs can be used as memory–dense replacements for digital CAMs by storing narrow ranges as discrete levels [4].

In conventional CAMs, the search operation is designed such that a match occurs only when the search query word and the stored data entries are identical (except for *don't care* bits), otherwise; the operation results in a mismatch. Approximate CAMs allow a certain number of mismatch bits to appear between the search query word, and stored data, leveraging the highly parallel, fast operation of CAMs to enable applications requiring approximate search, like pattern recognition, DNA sequencing, and machine learning amongst others [49].

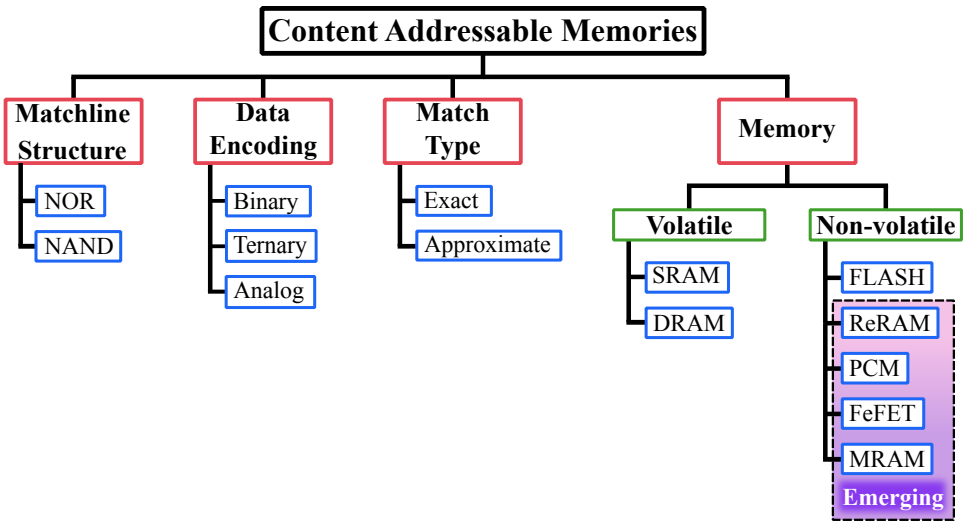

Figure 3.2: Content Addressable Memory taxonomy.

3.1.1 CMOS CAMs

CMOS-based CAMs use volatile SRAM cells for data storage for their fast and reliable search operation. This speed comes at the cost of increased energy consumption, and circuit area. Besides the dynamic energy dissipated by the matchlines and search-lines, the SRAM bit-cells show a high static energy consumption due to their large leakage current [50]. Emerging memory devices are being studied to propose alternative CAM designs featuring low standby power, no leakage, and high memory density [47]. In addition to the non-volatile nature of emergent devices, energy and area-efficient CAM systems enable new potential application spaces which are detailed in Section 3.2.

The conventional CMOS CAM cell uses the 6T-SRAM that holds one of two stable states formed by the feedback loop of two cross–coupled inverters. Nodes Q and Q_B output the stored data, and extra transistors are added to the cell to enable data search. Fig. 3.3 (a) shows the circuit diagram for the 10T-NOR CAM cell, where the bit-lines and access transistors are omitted for clarity. Transistors M_1 and M_3 are driven by the data stored in Q_B, and the search bit loaded to S_L, respectively. The pair forms a discharge path for the matchline that is disabled when either transistor is turned off. Likewise, transistors M_2 and M_4 form a second discharge path controlled by the voltage in Q, and S_{LN}. In case of a match, both discharge paths are disabled since the voltages in Q_B,

S_L and Q, S_{LN} are complementary. For instance, the search '0' operation sets $S_L = 0$ and $S_{LN} = V_{DD}$, and a stored '0' means that $Q_B = V_{DD}$ and $Q = 0$, turning off transistors M_2 and M_3. On the other hand, if the stored value was a '1', $Q = 1$, the discharge path through M_2 and M_4 is enabled. Thus, a mismatch ensures that the matchline is connected to ground through one of the two discharge paths. NOR-type cells are connected in parallel to the matchline to form a CAM word as shown in Fig.3.3 (b).

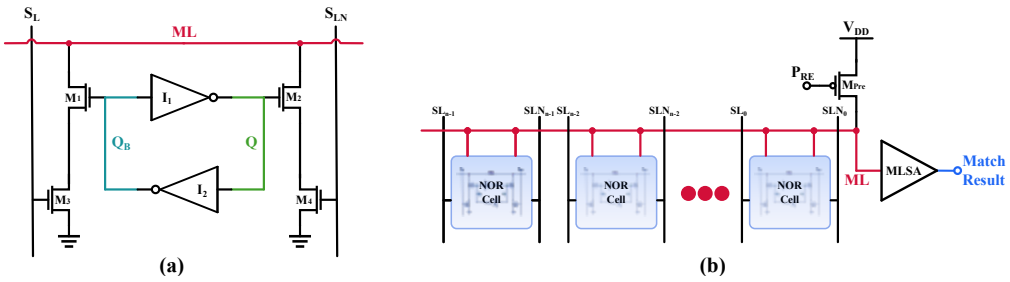

Figure 3.3: (a) 10T-NOR CAM cell. (b) NOR matchline with cells connected in parallel.

The operation of the NOR matchline requires three phases. In the first phase, the search-lines are driven to $S_L = S_{LN} = 0$, to ensure that all discharge paths are disconnected. During the second phase, PRE is driven low, and the matchline is pre–charged to V_{DD} through transistor M_{Pre}. Finally, during the evaluation phase, $PRE = V_{DD}$, and the search-lines are driven according to the search word. In the case of a match, all discharge paths are disabled and the matchline voltage remains high. Conversely, if there is a mismatch, there is at least one active path to ground which discharges the matchline. The sense amplifier senses the matchline, and outputs a value of V_{DD}, or 0 indicating a match or mismatch, respectively.

Fig. 3.4 (a) shows the circuit diagram for the 9T-NAND CAM cell, with the bit-lines and access transistors omitted for clarity. Transistors M_2 and M_3 act as pass transistors connecting S_L and S_{LN}, respectively, to the gate of transistor M_1. According to the data stored in nodes Q and Q_B, the gate of M_1 is going to be driven by S_{LN} if the cell stores a '0', and S_L is the cell stores a '1'. If the search is a match, the voltage at the gate of M_1 will be $V_{DD} - v_{th}$, turning the transistor on, and connecting the segment ML'_i to ML'_{i+1}. For

instance, searching for a '1' ($S_L = V_{DD}$, $S_{LN} = 0$), in a cell storing a '1' ($Q = V_{DD}$), will drive the gate of M_1 high through pass transistor M_2. In the case that the cell was storing a '0', the gate of M_1 receives a 0 form S_{LB} through pass transistor M_4. Thus, a mismatch turns off the transistor M_1 and disconnects the matchline. NAND-type cells are connected in series to form a CAM word as shown in Fig. 3.4 (b).

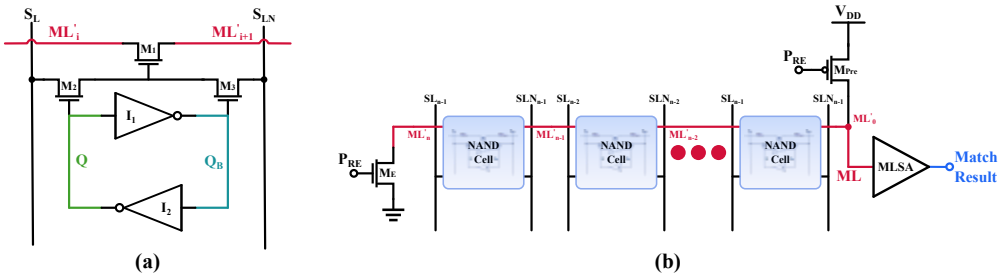

Figure 3.4: (a) 9T-NAND CAM cell. (b) NAND matchline with cells connected in series.

The NAND matchline requires two phases. During the pre–charge phase, the voltage of *eval* is driven low to disconnect the matchline from ground via transistor M_E. At the same time $PRE = 0$, charging the matchline through transistor M_{Pre}. During the evaluation phase, both PRE and *eval* are risen to V_{DD}, and the search-lines are driven according to the search word. In case of a match, a path is created connecting the matchline to ground through all the NAND cells, causing it to discharge. In the case of a mismatch, the path is disconnected by at least one cell, and the matchline voltage stays close to V_{DD}. The MLSA outputs a value of 0 or V_{DD} indicating a match, or mismatch respectively.

3.1.2 Non-Volatile CAMs Based on STT-MRAM Technology

Non-volatile CAMs based on STT-MRAM technology mainly offer compact area footprint, negligible leakage power consumption and scalability. The high switching speed of MRAM devices translates into low-latency write operations. Fig. 3.5 shows the structure of the 2T2MTJ cell presented in [51], featuring

one of the simplest NV-CAM cell structures. The cell stores bit information in the resistance states of the MTJ devices. During search operations, one of the two paths is enabled, and the matchline discharges at a rate that depends on the device resistance. The difference in resistance between HRS and LRS is measured by the TMR, and determines the sensing margin and reliability of the 2T2MTJ cell. This design features a very low area footprint but must operate in a word-parallel, bit-serial, manner to avoid search errors. This results in a long search latency and increased energy consumption [47].

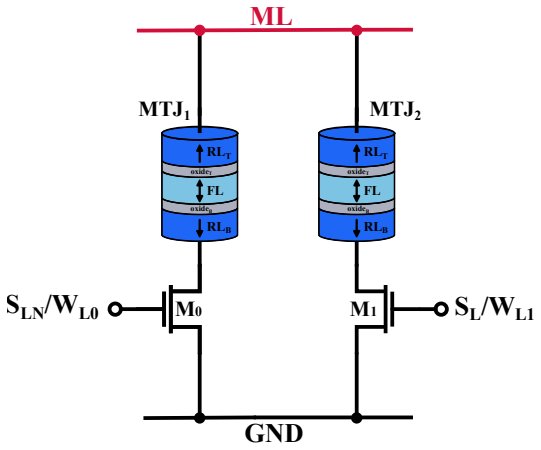

Figure 3.5: Circuit diagram for the 2T2MTJ NV-CAM cell [51].

The low TMR in STT-MTJ devices becomes a significant design challenge. As a result, all STT-MRAM-based NV-CAM cell designs suffer from reliability considerations due to process variations, leading to search errors. The Search Error Rate (SER) is a key parameter in the performance of a NV-CAM/TCAM, limiting word length and possible applications.

To achieve fast, reliable, and energy-efficient search operations, more recent STT-MRAM bit-cell designs include more complex transistor networks. The two main architectures for such networks are discussed below.

Voltage Divider Structures

Fig 3.6 (a) shows the basic structure of voltage-divider cells. Voltage divider solutions feature a moderate number of transistors, and usually no more than two MTJ devices. The sensing logic network is used to amplify the voltage

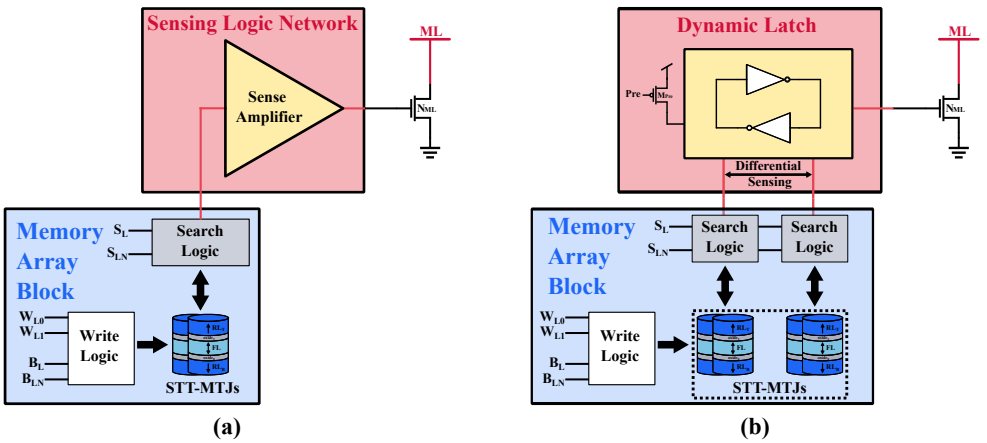

Figure 3.6: Top level diagram for the most common type of STT–MRAM based NV–CAMs explored in literature. (a) Voltage divider structure. (b) Latch-based structure.

difference at the output of the memory array block, and drive the matchline transistor.

Voltage divider cells tend to suffer from higher SER and longer search times leading to more energy consumption. While some designs rely on static sensing logic [52], [53], other voltage-divider based solutions [54], [55], use dynamic-based buffers in the sensing network to provide a faster and more reliable response.

Latch Based Structures

Fig 3.6 (b) shows the basic structure of latch-based type cells. This type of cell uses a greater amount of transistors and MTJs to implement a dynamic, differential sensing scheme, which serves to amplify the small voltage difference produced by the memory array block in order to drive the matchline transistor. Latch-based cells suffer from a higher area footprint, but provide a faster, more reliable search operation [56], [50].

3.2 Non-Voltatile CAMs Application Space

NV-CAMs share the same capabilities as traditional CAMs, which have been studied for a wide variety of applications including parametric curve extraction,

image encoding/decoding, and data compression. Relevant literature for the aforementioned applications is cited in [5]. The most common use for CAMs is packet classification and forwarding in network routers [57]. Routers must forward data packets to the correct output based on addresses that are stored as entries in routing tables. As the sizes of the table and the entries grow, TCAMs become a candidate to handle the demand for ever-growing networking speeds [47].

The introduction of novel devices in CAMs, accompanied by improvements in circuit and architecture design have opened the gates to new, emerging applications. A review of emergent applications like neuromorphic associative memory, text mining, pattern recognition in wearable electronics, and reconfigurable computing, among others, can be found in [47]. Reconfigurable computing systems like Field Programmable Gate Arrays (FPGAs) rely on lookup tables and configurable interconnect frameworks. Large CAMs configured as programmable logic arrays (PLAs) can lower memory requirements when mapping certain functions, while reducing the overhead of the programmable interconnect network [58].

The remainder of this section focuses on Associative Computing Systems (ACS), particularly Associative Processors (AP). An AP is a non-Von Neumman in-memory computing architecture that performs single instructions in parallel across multiple data entries within a CAM memory array [6].

Fig. 3.7 shows the architecture of an associative processor. The main component of the AP is the $m \times n$ cell CAM array that is used to store and process data. The CAM search query is stored in the KEY register, while the MASK register is used to define which columns are "active", meaning that they are affected by the AP write (update) and search operations. Each CAM row is connected to a TAG, forming a Processing Unit (PU). The TAG register is used to mark the rows that match during search operations. The interconnection block is a switching matrix that enables PUs to communicate in parallel with each other [59]. Some AP architectures may also feature a reduction tree connected to the TAGs, which enables the quick accumulation of TAG bits that are useful for vector to scalar transformations [15].

The execution principle of an AP is based on a succession of search and up-

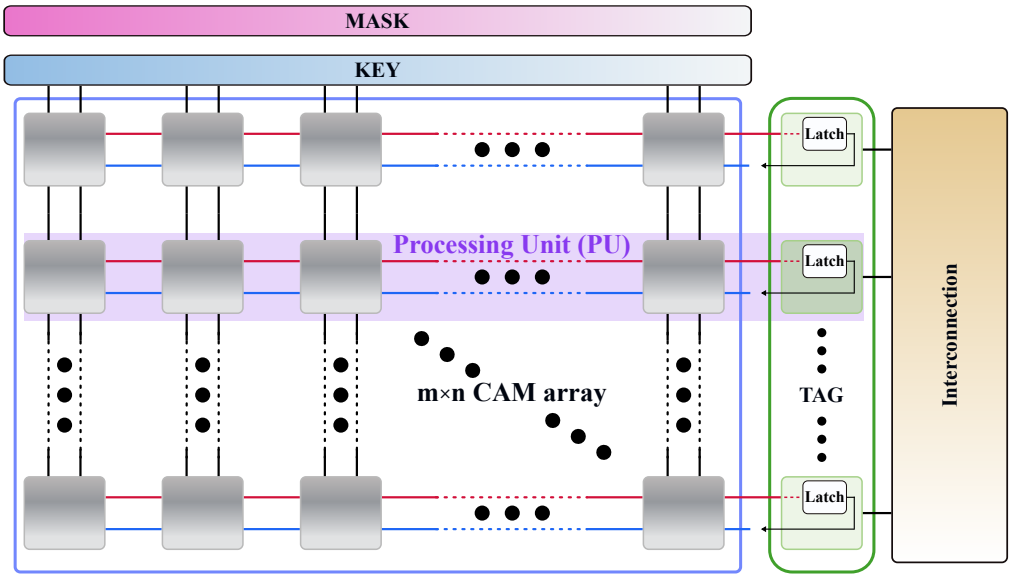

Figure 3.7: Associative Processor (AP) Architecture. Every CAM row is connected to a TAG, forming a Processing Unit.

date phases. During the search phase, the KEY is compared in parallel to every stored entry. During the update phase, data is written into the columns specified in MASK for every row that matched in the search phase. Any single–instruction–multiple–data (SIMD) function f(x), is transformed into a lookup table which acts as a truth table [59]. The AP evaluates the LUT in order by searching for the table input patterns and updating matching words with the corresponding table output. Operations are performed in a bit serial, word parallel manner, for more efficient LUT implementations [15]. The number of cycles is determined by the size of the argument x, regardless of the size of the dataset.

The associative processing execution model is limited by the throughput of single pattern searches in large, complex calculations, and the high write frequency of the search and update operations [6]. To mitigate those issues, novel AP architectures and data encoding methods have been explored in literature. For instance, the "Hyper-AP" design presented in [60] introduces multi-pattern search, and multi-search write computations in order to reduce the number of read and write operations. New circuit structures paired with novel architectures, and the improved performance of emergent devices have

inspired a renewed interest in associative processors [55].

Finally, STT–MRAM-based NV-CAMs have been studied as a suitable candidate for AP designs targeting problem sets that benefit from associative computing hardware. For example, the low power AP developed in [61] was fabricated with a $90nm$ CMOS/MTJ hybrid technology, and has been analyzed for image pattern recognition applications, consuming $600\mu W$ of operating power at a frequency of $20MHz$. Additionally, the "AM^4" AP presented in [3] builds upon the MRAM crossbar array structure presented introduced in [39], and has been analyzed for genome sequencing alignment workloads.

Chapter 4

Non-Volatile Content-Addressable Memory (NV-CAM) Design

This chapter studies the hybrid CMOS/MTJ design and performance evaluation of the proposed 17–transistor 4 (Double–Barrier) MTJ cell. This design builds upon the cell presented in [56]. Two extra transistors are added to enable fast and reliable write operations, which are crucial when targeting applications involving frequent entry updates such as Associative Processors. By adding the DMTJ technology and extra circuitry, the proposed cell achieves good performance while maintaining the reliability of the original design. The design presents standard-sized transistors. The 17T4MTJ cell is designed in TSMC $65nm$ technology using the Cadence Virtuoso software suite. The DMTJ devices are simulated using the Verilog-A compact model described below.

4.0.1 Overview of the MTJ Compact Model

The design of the non-volatile CAM cells uses DMTJs devices simulated using the Verilog-A compact model developed in [62]. The model exploits physics-based analytical formulas to calculate the resistance and statistical switching characteristics for
CoFeB/MgO/CoFeB/MgO/CoFeB perpendicular STT-DMTJs. The simulated switching time distributions are comparable to full micromagnetic and

experimental results [62]. Finally, the model considers Gaussian process variations for the thickness of both $oxide_T$ and $oxde_B$, the thickness of the free layer, cross-sectional area, and TMR.

Table 4.1 reports the main physical device parameters. Detailed calibration of the device is based on the parameters reported in [63], which were chosen to match experimental data for SMTJs. The DMTJ has a diameter of $20nm$, a free layer thickness of $1.2nm$, a top oxide thickness of $850pm$, and a bottom oxide thickness of $400pm$. The critical switching current is $6.182\mu A$, and the resistance for both states at $V_{DC} = 0V$ are $42.8k\Omega$ for the high resistive state, and $18.34k\Omega$ for the low resistive state. This results in a TMR of about 140%.

Table 4.1: DMTJ device parameters

Parameter	**Unit**	**Value**
Diameter (d)	nm	20
FL thickness (t_{FL})	nm	1.2
Top oxide thickness (t_{oxT})	pm	850
Bottom oxide thickness (t_{oxB})	pm	400
Critical current I_{CO}	μA	6.182
HRS (at 0V)	$k\Omega$	42.84
LRS (at 0V)	$k\Omega$	18.34
TMR (at 0V)	%	140%

4.1 17T4MTJ Cell Structure

Fig. 4.1 shows the schematic diagram for the proposed cell. The design consists of 17 transistors and 4 DMTJs (17T4MTJ) and can be divided into several blocks. First is the Memory Array Block (MAB) which is formed by the DMTJs MTJ_{1-4}, and transistors $M_{13}, M_{14}, M_{15}, M_{16}$. Compared to the MAB presented in [56], the block was modified to give each MRAM device its access transistor for faster writing. The MAB stores non-volatile data according to the resistance of each device as shown in Table. 4.2. Although the MAB can be used to store a ternary value 'X', this, and subsequent chapters only consider the cell for binary data search.

Next is the Search Logic Network (SN), consisting of transistors M_4, M_5,

Table 4.2: Memory array block data encoding

	Device State			
Stored Data	MTJ_1	MTJ_2	MTJ_3	MTJ_4
'0'	HRS	LRS	HRS	LRS
'1'	LRS	HRS	HRS	LRS
'X'	LRS	LRS	HRS	HRS

M_6, M_7 which handles the search input, enabling and disabling access to the MAB. Then, the Differential Sense Amplifier (DSA) consisting of two cross-coupled inverters (latch) made up from transistors M_0, M_2 and M_1, M_3, as well as precharge transistors M_{11} and M_{12}. Finally, the Match-Line Sensing Network (MLS) is driven by the output of the latch-based DSA and consists of an inverter M_8, M_9 and the match-line transistor M_{10}.

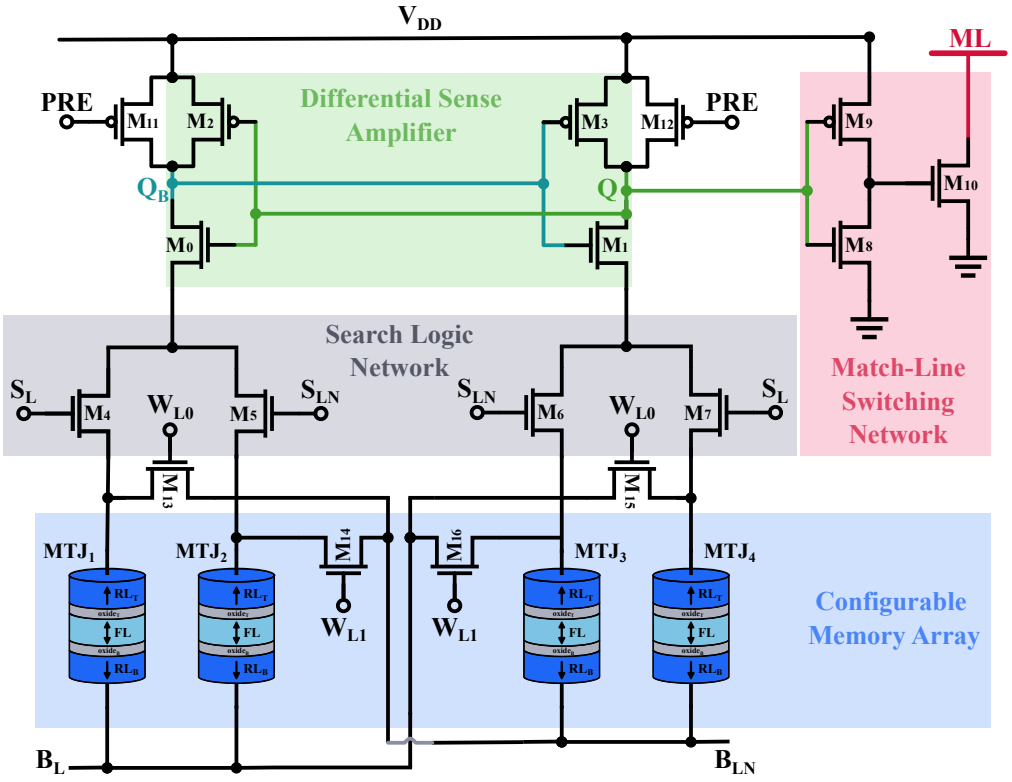

Figure 4.1: Circuit diagram for the proposed 17T4MTJ NV-CAM cell.

4.2 Cell Operation

This section gives a detailed analysis of the write and search cell operations.

4.2.1 Write Operation

During the write operation, the search-lines S_L and S_{LN} are driven to ground ($V_{SL/SLN} = 0V$), turning off the search logic network transistors and disconnecting the sense amplifier from the memory array. The operation involves only the MAB and is divided into two phases. During phase I, the bit-line (B_L, B_{LN}) voltage is set, and transistors M_{13}, M_{15} are enabled by the word-lines, allowing a bidirectional current flow from the bit-lines through MTJ_1 and MTJ_4 as shown in Fig. 4.2 (a). During phase II, the voltage difference between B_L and B_{LN} is reversed and transistors M_{14}, M_{16} are enabled as shown in Fig. 4.2 (b). The current is now able to flow through the two internal DMTJs MTJ_2, MTJ_3.

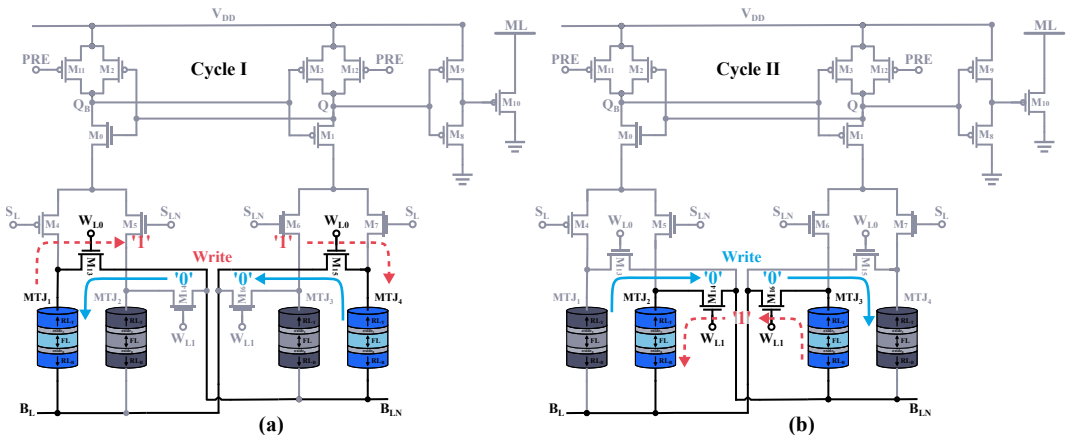

Figure 4.2: Write operation for the 17T4MTJ NV-CAM cell. (a) Phase 1 writes to $MTJ_{1,4}$ (b) Phase 2 writes to $MTJ_{2,3}$.

The write operation is verified by transient simulations of the cell, which involve writing two data values '0' and '1'. The operation was performed out on a single 17T4MTJ cell initially storing a '1', meaning the starting states of the DMTJs are (LRS, HRS, LRS, HRS) for MTJ_{1-4}, respectively. The supply voltage was set as $V_{DD} = 1V$. The resulting waveforms are shown in Fig. 4.3. As expected, each write operation requires two cycles to complete. During the

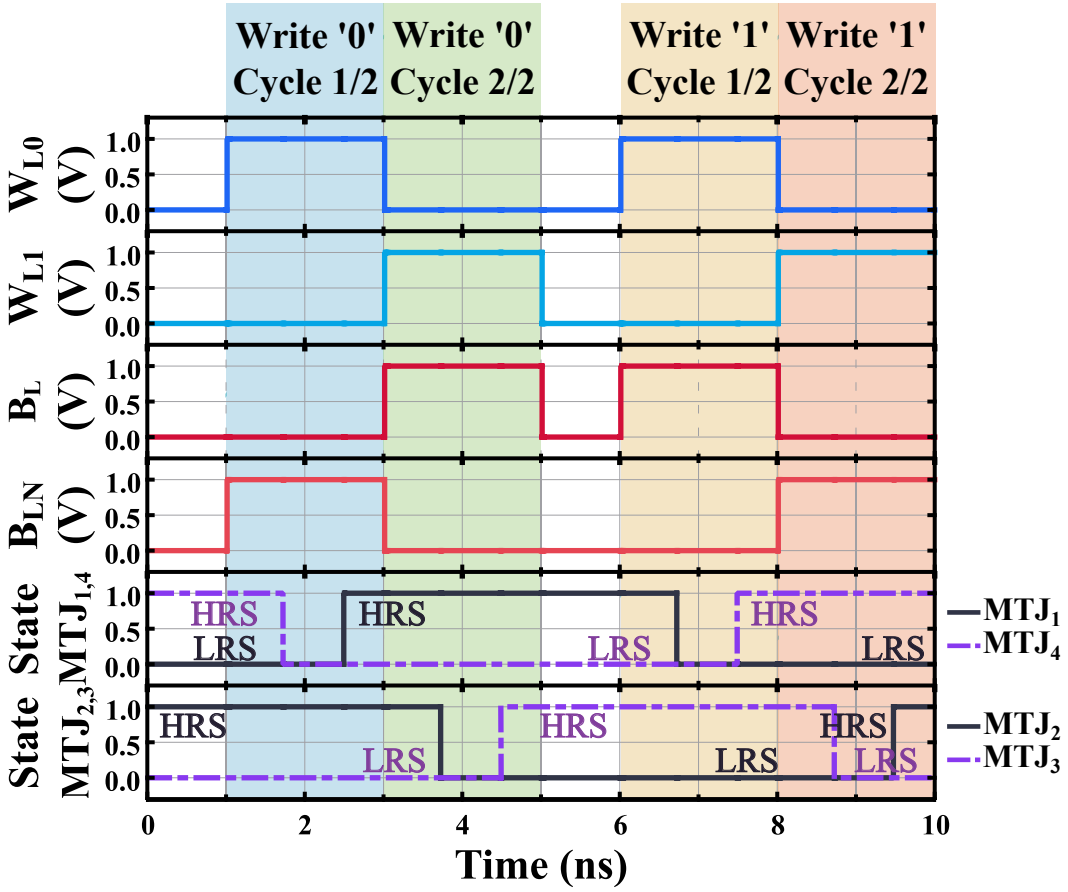

Figure 4.3: Timing diagram for the write operation of the proposed 17T4MTJ NV-CAM cell.

first cycle, corresponding to phase I, W_{L0} is set to V_{DD} while W_{L1} is set to 0, connecting the outermost devices, MTJ_1 and MTJ_4 to the write path. When writing a '0', the bit-lines are set as $B_L = 0$ and $B_{LN} = V_{DD}$, switching MTJ_1 to HRS and MTJ_4 to LRS. To write a '1', the bit-lines are set to the inverse values $B_L = V_{DD}$ and $B_{LN} = 0$, switching MTJ_1 to LRS and MTJ_4 to HRS. During the second cycle, corresponding to phase II, W_{L1} is set to V_{DD} and W_{L0} is set to 0, which connects the innermost devices, MTJ_2 and MTJ_3 to the write path. During this phase, the bit-lines are set to the opposite values of the previous phase. Therefore, for the case of a '0', $B_L = V_{DD}$ and $B_{LN} = 0$, switching MTJ_2 to LRS and MTJ_3 to HRS. Otherwise, for a '1', $B_L = 0$ and $B_{LN} = V_{DD}$, switching MTJ_2 to HRS and MTJ_3 to LRS.

Table. 4.3 summarizes the search-line, word-line, and bit-line input combinations for each write phase, as well as the stored states of each DMTJ. The

cycle time ensures that writes during each phase are carried out with a WER of 10^{-7}.

Table 4.3: Write Operations for the proposed 17T4MTJ NV-CAM cell

		Signals					**States DMTJ$_{1,2,3,4}$***		**Cycle**
Operation		$S_{L/LN}$	B_L	B_{LN}	W_{L0}	W_{L1}	Initial	Final	**Time**
Write '0'	I	0	0	V_{DD}	V_{DD}	0	L,H,L,H	H,H,L,L	$\sim 2ns$
	II	0	V_{DD}	0	0	V_{DD}	H,H,L,L	H,L,H,L	
Write '1'	I	0	V_{DD}	0	V_{DD}	0	H,L,H,L	L,L,H,H	
	II	0	0	V_{DD}	0	V_{DD}	L,L,H,H	L,H,L,H	

* HRS and LRS states are abbreviated as H and L.

4.2.2 Search Operation

During the search operation, the bit-lines $B_L$and B_{LN} are grounded ($V_{BL/BLN}$) to provide a discharge path for the dynamic latch. The operation is divided into two phases and involves all blocks in the circuit. The first phase is the pre–charge phase. As shown in Fig. 4.4 (a), S_L and S_{LN} are set to 0, disconnecting the lower blocks of the circuit. The PRE signal driven low, allowing transistors M_{11} and M_{12} to charge nodes Q and Q_B to V_{DD}, while turning off transistor M_{10} to avoid shorting the matchline to ground. The matchline is pre–charged to V_{DD} by a pass transistor external to the cell.

The second phase is the evaluation phase. During this phase, the PRE signal is driven to V_{DD}, the bit-lines are connected to ground, and the word-lines W_{L0} and W_{L1} are turned off to avoid bypassing the memory array block. The voltages on S_L and S_{LN} are set to enable the correct paths through the search logic network. Fig. 4.4 (b) illustrates the enabled discharge paths for a '0' search, which involve MTJ_2 and MTJ_3. On the other hand, Fig. 4.4 (c) shows the enabled paths for a '1' search, involving MTJ_1 and MTJ_4.

The search operation is verified by transient simulations that involve searching for '0', '1', and 'X' (don't care) values on a circuit containing a single 17T4MTJ bit-cell with a $100fF$ load capacitance connected as a NOR-type matchline (ML). The ML is pre–charged by a pMOS transistor of width $1\mu m$ and length $60nm$. The supply voltage used was $V_{DD} = 1V$. The resulting waveforms are

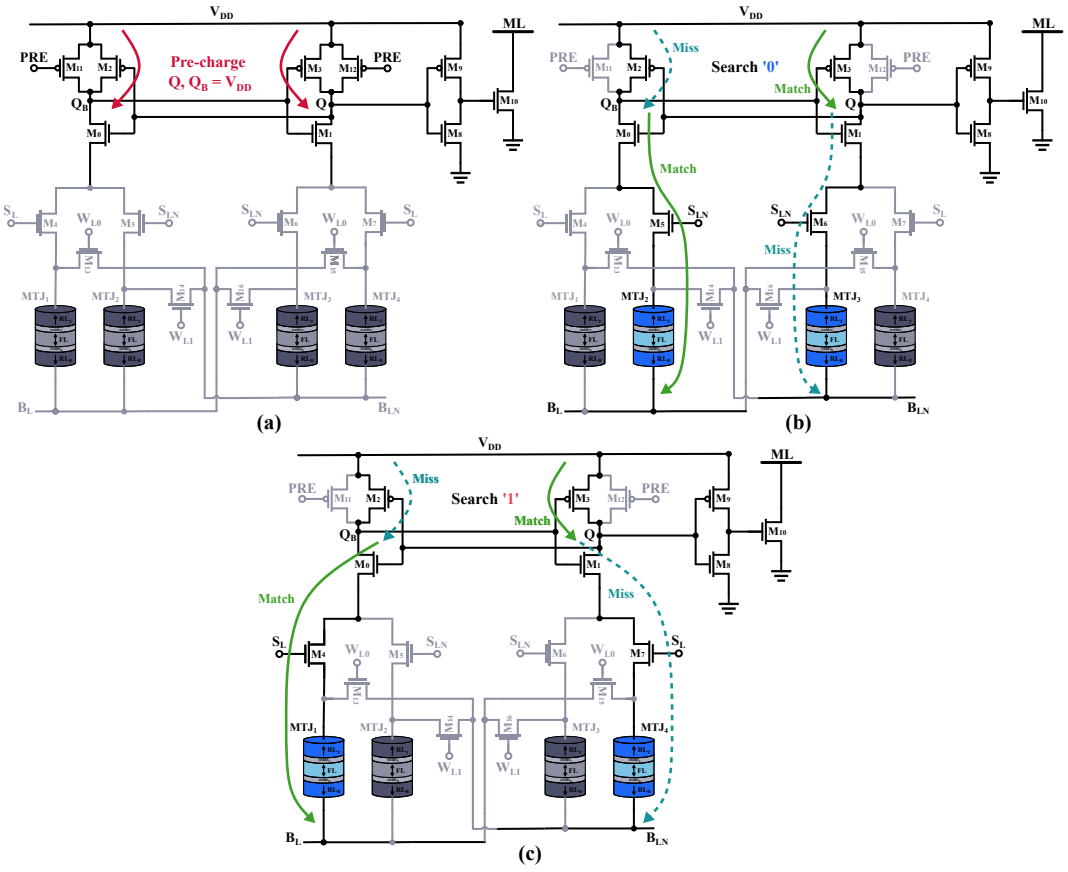

Figure 4.4: Search operation for the 17T4MTJ NV-CAM cell. (a) Pre–charge phase. (b) Evaluation phase for Search '0'. (c) Evaluation phase for Search '1'.

shown in Fig. 4.5.

The search requires two cycles to complete both phases. The search waveforms were simulated for two cases: in Case 1 the cell stores a '0' while in Case 2 the cell stores a '1'. During the pre–charge phase, PRE, S_L and S_{LN} are set to 0, allowing, the ML, and nodes Q and Q_B to be driven to V_{DD}. The evaluation phase by setting the search-line voltages and raising PRE to V_{DD}.

For a search '0' operation $S_L = 0$, $S_{LN} = V_{DD}$, and discharge paths through the innermost DMTJs are enabled. In the case of a stored '0' ($MTJ_2 = LRS$, $MTJ_3 = HRS$), the resistance through the path formed by M_0, M_5 and MTJ_2 is lower than that through M_1, M_6 and MTJ_3, causing the node Q_B to discharge faster than Q. The voltage difference between the nodes is quickly amplified by the positive feedback of the cross–coupled inverters until Q_B reaches 0 and Q returns to V_{DD}. As a result, transistor M_2 on the leftmost

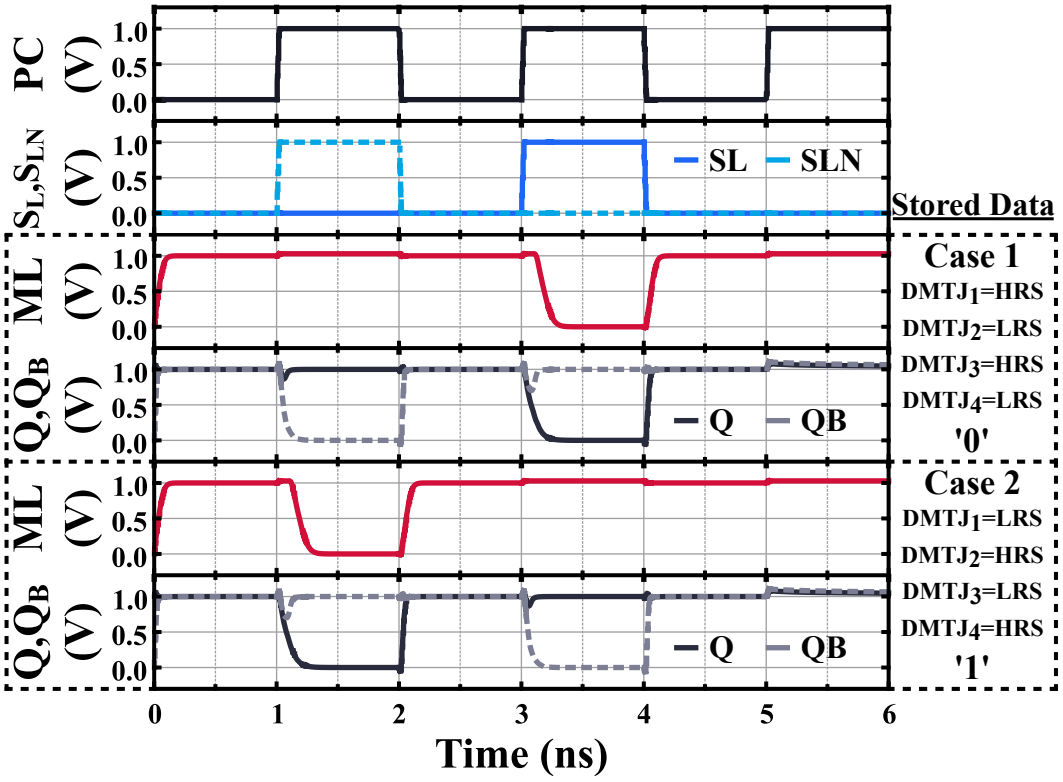

Figure 4.5: Timing diagram for the search operation of the proposed 17T4MTJ NV-CAM cell. Search '0', '1', and 'X' are verified for both possible stored values.

path and transistor M_1 on the rightmost path are turned off, meaning that after a short switching delay, no current flows through the DMTJs from V_{DD} to B_L or B_{LN}. The voltage at the input of transistor M_10 is 0, so the transistor remains off and the matchline does not discharge, indicating a match. In case of a stored '1' ($MTJ_2 = HRS$, $MTJ_3 = LRS$), the path resistances are reversed, and node Q begins to discharge faster than node Q_B. The positive feedback of the latch amplifies this difference and drives Q_B to V_{DD} while Q fully discharges to 0. Transistors M_0 and M_3 are turned off, avoiding direct current paths from V_{DD} to B_L or B_{LN}. The voltage at the input of M_{10} is V_{DD}, creating a discharge path for the ML, indicating a mismatch.

Likewise, for a search '0' operation $S_L = V_{DD}$, and $S_{LN} = 0$, and discharge paths through the outermost DMTJs are enabled. In case of mismatch (stored '0'), $MTJ_1 = HRS$ and $MTJ_4 = LRS$, causing node Q to discharge faster, eventually reaching '0' and driving the input of M_{10} high through the M_8–

M_9 inverter, causing the ML to discharge. In case of a match (stored '1'), $MTJ_1 = LRS$ while $MTJ_4 = HRS$, causing node Q_B to discharge faster, and driving Q to V_{DD}. The input of M_{10} is low, disconnecting the ML path to ground.

Finally, for a search 'X' operation $S_L = 0$, and $S_{LN} = 0$, and no discharge paths are enabled. Both nodes Q and Q_B remain at V_{DD}, and the result is always a match.

Table. 4.4 summarizes the search-line, word-line and bit-line input combinations for each search operation, as well as the matchline response depending on the stored data. The search time is given by ML discharge delay, which depends on the load capacitance and hence on the number of parallel connected cells (word–length).

Table 4.4: Search Operations for the proposed 17T4MTJ NV-CAM cell

	Signals						**Stored Data**		**Matchline**‡
Operation	S_L	S_{LN}	B_L	B_{LN}	W_{L0}	W_{L1}	Value	States*	
Search '0'	0	V_{DD}	0	0	0	0	'0'	H,L,H,L	Match
	0	V_{DD}	0	0	0	0	'1'	L,H,L,H	Mismatch
Search '1'	V_{DD}	0	0	0	0	0	'0'	H,L,H,L	Match
	V_{DD}	0	0	0	0	0	'1'	L,H,L,H	Mismatch
Search 'X'	0	0	0	0	0	0	-†	-	Match

* HRS and LRS states are abbreviated as H and L. Each letter corresponds to $MTJ_{1,2,3,4}$ respectively.

† Search 'X' behaves equally for any stored data.

‡ Matchline evaluation has $< 1ns$ delay.

4.3 Performance Analysis

Fig. 4.6 shows the proposed 17T4MTJ cell layout implemented using transistors in the TSMC $65nm$ technology node. All transistors are standard-size transistors with width $w = 200nm$ and length $l = 60nm$. The cell has a total width of $3.105\mu m$, and a height of $4.31\mu m$, giving a total area of $13.38\mu m^2$. The use of standard-sized transistors allows for a compact cell design, even with the high transistor count. Note that the proposed NV-CAM cell presents

a larger area footprint as compared to other NV-CAM designs. However, this overhead becomes less significant when amortized over a large area available to design the memory macro. For example in 3D integration applications, an entire tier can be dedicated to the NV-CAM.

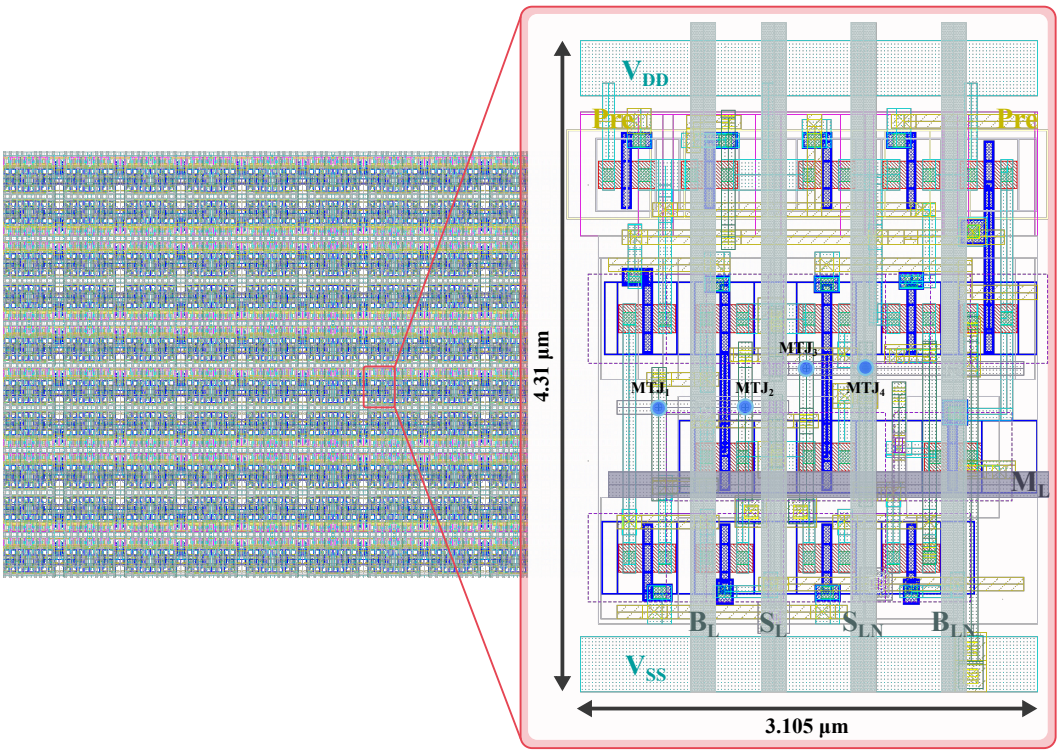

Figure 4.6: Cell layout for the proposed 17T4MTJ NV-CAM cell with a total area footprint of $13.38\mu m^2$.

Integration with non-volatile devices can be realized using a hybrid CMOS/MTJ process where DMTJ devices are fabricated between Metal-3 (M3) and Metal-4 (M4) during the back-end of the CMOS process [55]. Fig. 4.7 shows a 3D hybrid process scheme.

The performance of the 17T4MTJ cell is examined using Monte–Carlo simulations with 1000 runs for every measurement. Results are obtained from the 3σ corners to examine the effects of process variations on DMTJ devices and CMOS transistors. The performance of the NV-CAM cell is tested on different memory word lengths ranging from 8- to 128-cells. Fig. 4.8 shows the CAM word setup, consisting of an array of n-cells connected to a matchline using the NOR topology. The matchline is connected to a transistor M_{Pre} of dimensions $w = 1\mu m$, $l = 60nm$ that is used during the pre–charge phase. The

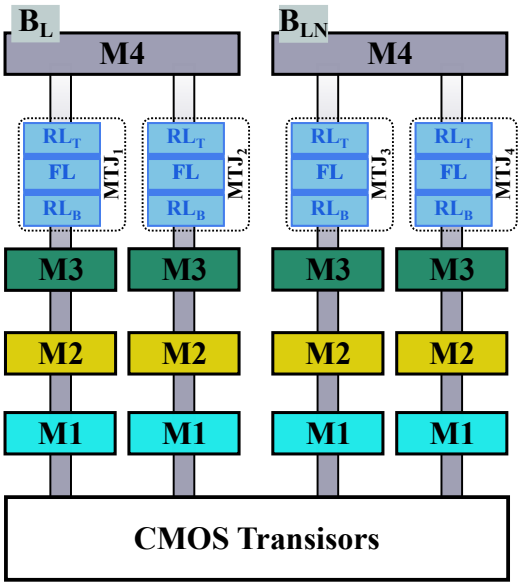

Figure 4.7: Hybrid 3D CMOS/MTJ process. DMTJs are placed between M3 and M4 [55].

sense amplifier consists of an unskewed buffer that drives the word output. Measurements are done for $V_{DD} = 1V$ and $V_{DD} = 1.2V$.

Table. 4.4 shows the search results at the 3σ corner for both values of V_{DD} at every word length. The search latency is defined as the 50% delay between the rise of PRE (end of the pre–charge phase), and the fall of Out, signaling a mismatch. The delay is measured for for the worst-case scenario, where there is only a single bit mismatch between the stored word and the search word. For $V_{DD} = 1V$, Fig. 4.9 (a) shows the search latency (t_search) as a function of word length for the 3σ corner. The average search time is $274ps$, and the latency is kept below $0.5ns$ for every length. Fig. 4.9 (b) shows the probability density function (PDF) for a 64-bit word. Using $V_{DD} = 1.2V$, the average latency is $196ps$, corresponding to a $1.4\times$ improvement in performance. For a 64-bit word in particular, the search at a higher V_{DD} is $1.35\times$ times faster.

The design has a very low SER, with the value rising with word length from 0% up to 0.2% when $V_{DD} = 1V$. The SER does not seem to increase beyond the 16-bit length, suggesting that a greater number of Monte-Carlo simulations are required to properly determine a trend. In the case that an application requires an even lower SER, [56] includes guidelines on improving the error rates by

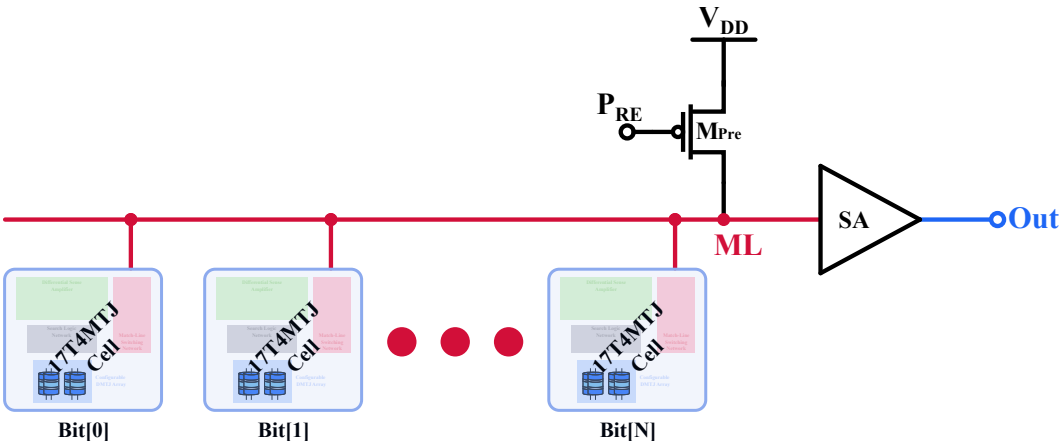

Figure 4.8: 64-bit CAM word using the proposed 17T4MTJ NV-CAM cell. The NOR matchline structure is pre–charged using transistor M_{Pre}. The sense amplifier is implemented by a simple static buffer.

increasing the device TMR, and adjusting the sizes of transistors M_8,M_9 in the ML switching network, as well as the transistors in the search logic network. Increasing the value of V_{DD} has a detrimental effect on the SER, causing it to rise to a maximum of 0.9% for the 128-bit word. The cause for this increase in errors is due inverse relation between the applied device voltage and the TMR, which is captured by the DMTJ compact model. For high voltages, the resistance of the HRS and LRS states can become practically equal. Therefore, increasing V_{DD} improves the response time of the latch, but also reduces the minimum sensing margin between MTJ states which translates to a greater number of errors when process variations are taken into account.

In typical applications, the mismatch case is more energy-expensive and much more common than the match case. However, for the proposed application, each row would be part of a processing unit (PU) which will match at least once for every processed bit, therefore; a significant number of matches are expected during every search. The search energy is reported here as the average between match and mismatch during the evaluation phase. For $V_{DD} = 1V$, the maximum evaluation energy is $263.1fJ$ for the 128-bit word. A 64-bit word consumes 50.96% less energy ($129.05pJ$), as expected.

The average energy consumption during the pre–charge phase is around 71% of the evaluation energy for every word length. In this phase, a significant amount

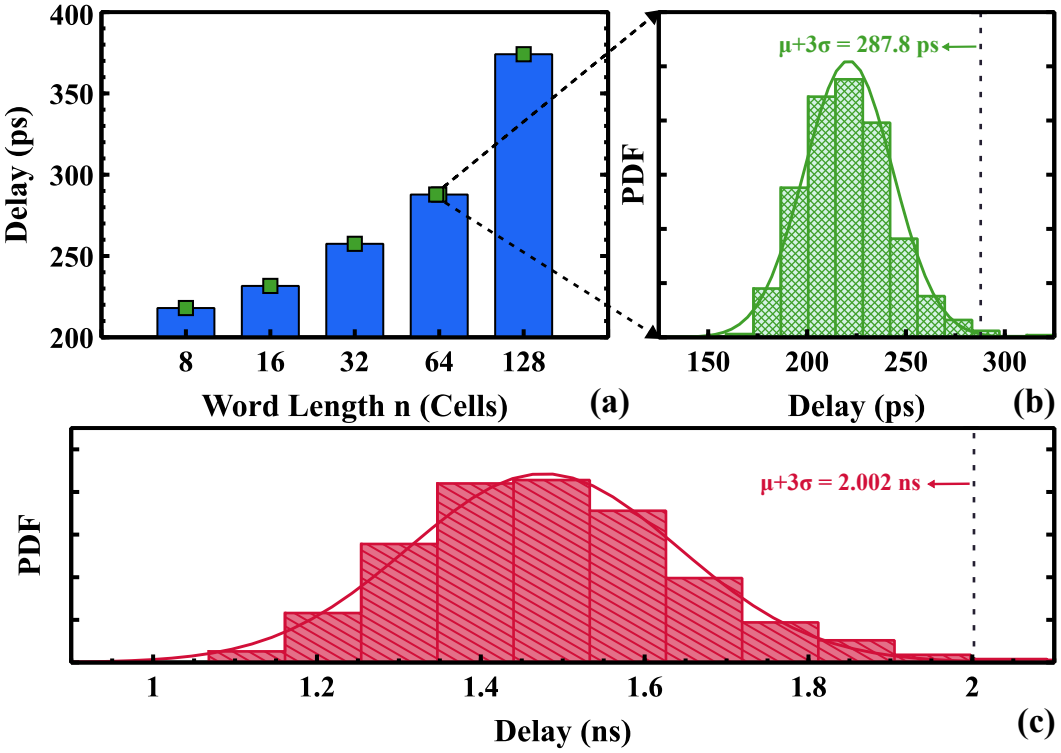

Figure 4.9: Performance evaluation results for the proposed 17T4MTJ NV-CAM cell after 1000 Monte-Carlo runs. (a) Search latency as a function of word length at the 3σ corner. (b) PDF of search delay for a 64-bit word. (c) PDF of the worst-case write latency for a single phase.

of energy is consumed by the dynamic latch. For a 64-bit word, only $13.3pJ$ are spent in charging the ML, while the NOR cell array requires $85.26pJ$. Methods like ML segmentation can be used to reduce the number of pre–charged cells and provide a better energy efficiency for the CAM array, albeit at an increased latency. The average search energy of a 64-bit word considering both pre–charge and evaluation phases is $221.0pJ$.

For V_{DD} = 1.2V, the maximum evaluation energy is $387.45fJ$. The average energy consumption of 64-bit word on both phases is $332pJ$.

Right at the start of the evaluation phase, the nodes Q and Q_B are discharged through the active MTJs in the MAB. In that moment a short, but high transient current flows from V_{DD} to B_L and B_{LN} through the DMTJs. From transient simulations with $V_{DD} = 1.2V$, the current pulse reaches a peak of $3.55\times I_{C0}$. Since the read and write paths on the two terminal device are

shared, there is a risk of overwriting stored data during search. The probability of switching depends not only on the current strength, but also on the length of the pulse. If the pulse is short enough, the switching probability can be made negligible $p_{switch} = 10^{-7}$, corresponding to a WER of $1 - 10^{-7}$. The transient pulse duration was measured in 1000 Monte-Carlo simulations with $V_{DD} = 1.2V$. The average pulse length is $0.125ns$. Meanwhile, the average switching time (WER =0.999999) is $0.221ns$. Pulses with higher currents discharge the internal nodes faster, which leads to shorter transients, while longer pulses produce lower currents. From all the simulations, there were no instances where the pulse length exceeded the switching time, ensuring data reliability during search operations. None of the SER errors were caused by data overwrite.

Table 4.5: Search performance for the proposed 17T4MTJ NV-CAM cell

V_{DD} **(V)**	**Word–Length n**	**Search Time (ps)**	**Eval. Energy (fJ)**	**SER %**
1	8	218.00	19.19	0.0%
	16	231.56	34.79	0.2%
	32	257.52	66.16	0.2%
	64	287.79	129.05	0.2%
	128	374.12	263.15	0.2%
1.2	8	156.40	27.31	0.0%
	16	165.28	50.33	0.3%
	32	182.44	97.14	0.3%
	64	211.97	191.65	0.4%
	128	265.43	387.45	0.9%

Table. 4.3 shows the write results at the 3σ corner for both values of V_{DD}. The single phase write time t_{phase} is defined as the switching delay between the rise of W_0 for phase 1, or W_{L1} for phase 2, and the change of state in the DMTJs. The write path consists of a 1T1MTJ structure, which enables fast writing with standard-sized transistors, and without the need for a high write voltage.

The transition from LRS→HRS is always the slowest since the nMOS access transistor is connected to V_{DD}. For example, during phase 1 of the Write '0' operation, $B_{LN} = V_{DD}$ and transistor M_{13} causes a drop in the voltage going

into MTJ_1, reducing the switching current. Fig. 4.9 (c) shows the PDF for the worst-case write delay in a single phase when $V_{DD} = 1V$. The single phase write delay is $t_{phase} = 2.002ns$, giving a total $t_{write} = 4.004ns$. The write energy is $241pJ$. On the other hand, the write performance can improve when using a higher supply voltage. For $V_{DD} = 1.2V$ the cell is $1.6\times$ faster, with $t_{write} = 2.468ns$. Although the power consumption during write increases, the write energy improves by 3.5% due to the shorter delay.

Table 4.6: Write performance for the proposed 17T4MTJ NV-CAM cell

V_{DD} **(V)**	**Single Phase Write Delay (ns)**	**Total Write Delay (ns)**	**Total Write Energy (fJ)**
1	2.002	4.003	241
1.2	1.234	2.468	230.3

Finally, given the non-volatile property of the DMTJs, the power to the cell can be cut-off when comparisons are not needed, so leakage is eliminated. However, in the case of short periods of inactivity, a full power-down of the CAM may not be desired. In those cases, the cell can be set on stand-by by driving the PRE signal to 0. The reason is the voltage drop between the internal node Q and the B_L in case of a mismatch during the evaluation phase. The node voltage is not exactly $0V$ in stand-by, which increases the leakage of the inverter made by M_8, M_9. Leaving the CAM word in a pre-charge state ensures little leakage on the CAM cell inverters. The stand-by is measured for a 64-bit CAM word left in a pre–charge state for a long time after a series of searches. When $V_{DD} = 1V$ there is an $18.89nW$ consumption per cell, which doubles to $37.94nW$ for $V_{DD} = 1.2V$.

Chapter 5

Alternative NV-CAM Cell Architectures

5.1 Overview of Alternative Cells

This chapter explores various STT-MRAM-based NV-CAM alternatives reported in the literature. For each CAM cell, the schematic and detailed operational principles are presented. followed by a discussion of the design challenges associated with them. The discussion highlights issues like risks of unwanted data manipulation during search or long latency writes.

Finally, the alternative bit-cells are implemented using TSMC $65nm$ technology, and their performance is measured for a 64-bit CAM word. The evaluation focuses on latency for both search and write operations, energy consumption, and reliability. The results are compared to those of the proposed 17T4MTJ NV-CAM cell with an emphasis on the Search Error Rate (SER), Write Error Rate (WER), and write/search delay.

5.2 9T2MTJ

5.2.1 Cell Schematic and Operating Principles

Fig. 5.1 shows the 9-transistor 2 MTJ (9T2MTJ) NV-CAM cell proposed by Matsunaga, Katsumata, Natsui, *et al.* [54]. The cell consists of several blocks. First, the memory array block (MAB) consisting of the devices MTJ_1 and

MTJ_2, as well as two transistors M_0 and M_1. The MAB stores non-volatile data encoded in the resistance of each DMTJ. A stored '0' corresponds to the states $MTJ_1 = LRS$, $MTJ_2 = HRS$, while a stored '1' is encoded by $MTJ_1 = HRS$, $MTJ_2 = HRS$. The array is able to store a ternary value 'X', but this work only considers binary operations on the CAM.

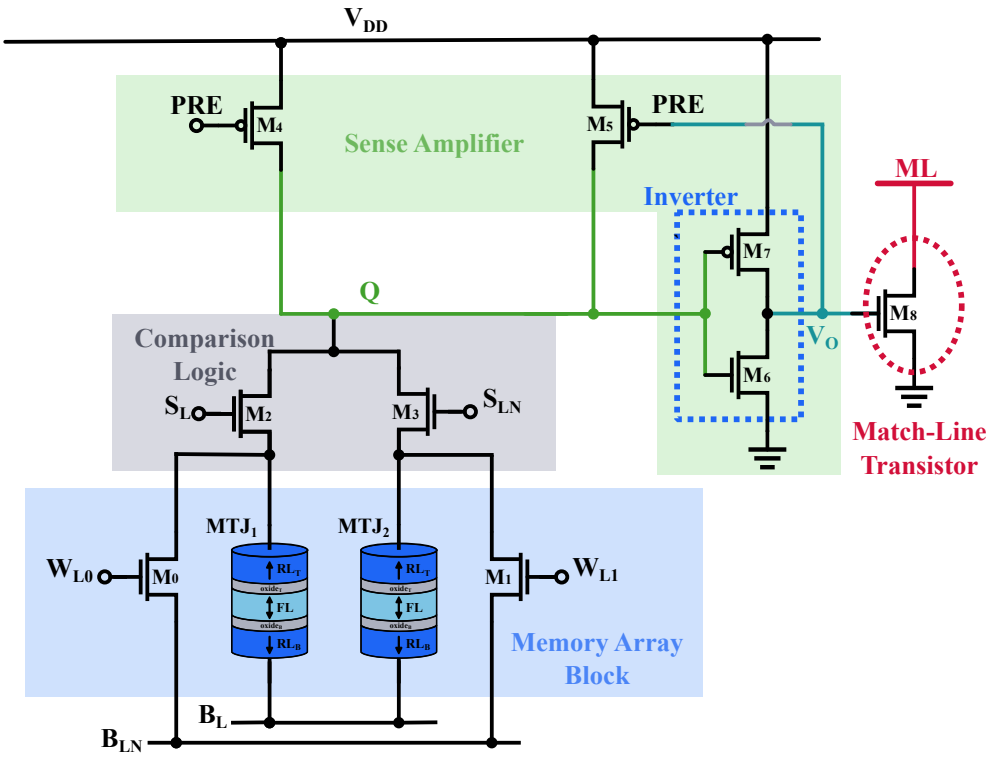

Figure 5.1: Circuit diagram for the 9T2MTJ NV-CAM cell [54].

The next block is the comparison logic (CL) involving transistors M_2, M_3 which enable access to the DMTJs connected below. The final block is the sense amplifier (SA), consisting of a dynamic buffer made up from the pre–charge transistor M_4, the feedback transistor M_5 and the inverter M_6, M_7. The SA amplifies the TMR of the storage devices and drives the matchline transistor M_8 with full swing, allowing a fast matchline discharge.

The write operation requires two phases to set the state of each DMTJ. The signal inputs and states are summarized in Table. 5.1. First, the search-lines S_L and S_{LN} are grounded, disconnecting the MAB from the rest of the circuit. During phase 1, $W_{L0} = V_{DD}$ and $W_{L1} = 0$, turning on M_0 to enable a current path from the bit-lines through MTJ_1. A '0' is written by setting the bit-line

voltages to $B_L = 0$ and $B_{LN} = V_{DD}$, which switches MTJ_1 to LRS. To write a '1', the bit-lines are driven by the opposite polarity, $B_L = V_{DD}$, $B_{LN} = 0$, and $MTJ_1 = HRS$.

Table 5.1: Write Operations for the 9T2MTJ NV-CAM cell [54]

		Signals					**States DMTJ$_{1,2}$***	
Operation		S_L/S_{LN}	B_L	B_{LN}	W_{L0}	W_{L1}	Initial	Final
Write '0'	I	0	0	V_{DD}	V_{DD}	0	H,L	L,L
	II	0	V_{DD}	0	0	V_{DD}	L,L	L,H
Write '1'	I	0	V_{DD}	0	V_{DD}	0	L,H	H,H
	II	0	0	V_{DD}	0	V_{DD}	H,H	H,L

* HRS and LRS states are abbreviated as H and L.

Phase 2 begins by setting $W_{L0} = 0$ and $W_{L1} = V_{DD}$, turning on M_1 and selecting MTJ_2 for writing. To write a '0', the bit-lines are driven to $B_L = V_{DD}$, and $B_{LN} = 0$, switching MTJ_2 to HR. Otherwise, to write a '1' the lines are set to $B_L = 0$, and $B_{LN} = V_{DD}$, and $MTJ_2 = LRS$

The search operation is divided into two phases, pre–charge and evaluation. During pre–charge PRE and S_L/S_{LN} are driven to ground. This disconnects the MAB, and allows the node Q to charge to V_{DD} through the pre–charge transistor M_4. At the same time, the matchline is charged to V_{DD} by an external transistor. The evaluation phase begins when PRE is driven to V_{DD}, the bit-lines are driven to $B_L/B_{LN} = 0$, and S_L/S_{LN} are set according to the desired search bit. Table. 5.2 summarizes the search-line, bit-line, and word-line inputs for each search operation.

Table 5.2: Search Operations for the 9T2MTJ NV-CAM cell [54]

	Signals				**Stored Data**		**Matchline**
Operation	S_L	S_{LN}	B_L/B_{LN}	W_{L0}/W_{L1}	Value	DMTJ$_{1,2}$*	
Search '0'	0	V_{DD}	0	0	'0'	L,H	Match
	0	V_{DD}	0	0	'1'	H,L	Mismatch
Search '1'	V_{DD}	0	0	0	'0'	L,H	Match
	V_{DD}	0	0	0	'1'	H,L	Mismatch
Search 'X'	0	0	0	0	-	-	Match

* HRS and LRS states are abbreviated as H and L.

When searching a '0', $S_L = 0$, $S_{LN} = V_{DD}$, and a path from Q to B_L is

enabled through MTJ_2. Likewise, when searching a '1', $S_L = V_{DD}$, $S_{LN} = 0$, and the path goes through MTJ_1. The node Q is discharged according to the state of the selected DMTJ. If the device is in HRS, the voltage divider structure formed by M_5, M_1/M_2 and $MTJ_{1/2}$ outputs a 'high' voltage V_{QH}, which is inverted by M_6,M_7, and drives V_O to 0. This turns off the matchline transistor, indicating a match. If the device is in LRS, the voltage on node Q reaches a low value V_{QL} that is below the threshold of the inverter (M_6,M_7), driving V_O high. The rise in V_O increases the gate voltage of M_5, driving the node Q closer to 0. This feedback mechanism finally drives V_O to V_{DD}, which turns on the matchline transistor, indicating a mismatch. Finally, for a search 'X' operation, both $S_L = 0$ and $S_{LN} = 0$, so the node Q maintains its charge during the evaluation phase and a match occurs.

5.2.2 Design and Discussion

Table. 5.3 shows the transistor sizes for the 9T2MTJ cell designed under a $65nm$ technology node. The write operation is performed by the memory array block, which provides a 1T1MTJ write path which is the same write path as the 17T4MTJ cell studied in the previous chapter. The configuration ensures a fast, reliable write performance with small access transistors. As such, the write transistors M_0 and M_1 are set to standard size.

Table 5.3: Transistor sizes for the simulated 9T2MTJ NV-CAM cell

Transistor Name	**Width (nm)**	**Length (nm)**
M0	200	60
M1	200	60
M2	120	60
M3	120	60
M4	200	60
M5	200	390
M6	200	60
M7	200	60
M8	200	60

The search operation depends on the comparison logic and sense amplifier blocks. The voltage difference $V_{QH} - V_{QL} = \Delta V_Q$ must be properly sensed

by the inverter, meaning that the inverter threshold must lie between both values. To achieve that, one can skew the inverter, or increase the voltage drop through transistor M_5. The second approach is considered, and for that, the length of M_5 is increased. The dimensions for M_5 are a width of $200nm$ and a length of $390nm$. The inverter transistors M_6 and M_7 use standard size. The short-circuit current during the evaluation phase is an important design parameter. In case of a match, transistor M_5 is turned on creating a direct path from V_{DD} to ground through the selected search transistor and the DMTJ. The current through this path flows for the entirety of the evaluation phase, increasing not only power consumption, but also the risk of dielectric breakdown in the DMTJs. Furthermore, in case of a mismatch, the transient current flowing through the DMTJ in LRS can cause the state to switch if given enough time, overwriting data during search. To mitigate this issue, the search transistors M_2 and M_3 were minimally sized, increasing the resistance through the divider.

Still, most of the mismatch search errors found during the performance evaluation of the cell (Section 5.5) were caused by data overwrite. A possible solution is to increase the resistances of the MTJ devices, at the cost of write performance and access transistor size.

Finally, the pre–charge transistor M_4, and matchline transistor M_8 use standard sizes.

5.3 10T4MTJ

5.3.1 Cell Schematic and Operating Principles

Fig. 5.2 shows the 10-transistor 4 DMTJ (10T4MTJ) NV-CAM cell proposed by Song, Na, Kim, *et al.* [50]. The cell is made up from a memory array block (MAB), the Cross-Coupled transistor Latch (CCL) and the matchline transistor M_9. The memory array block consists of the search-line transistors M_0, M_1, M_2, M_3, each connected to a DMTJ device MTJ_{1-4}; and the write transistor M_4. The MAB stores data encoded in the non-volatile resistive state of the MRAM devices. To store a '0', $MTJ_1 = HRS$, $MTJ_2 = LRS$,

$MTJ_3 = HRS$, and $MTJ_4 = LRS$. To store a '1', $MTJ_1 = LRS$, $MTJ_2 = HRS$, $MTJ_3 = LRS$, and $MTJ_4 = HRS$. The array is also able to store the ternary value 'X', but this work only considers binary operations.

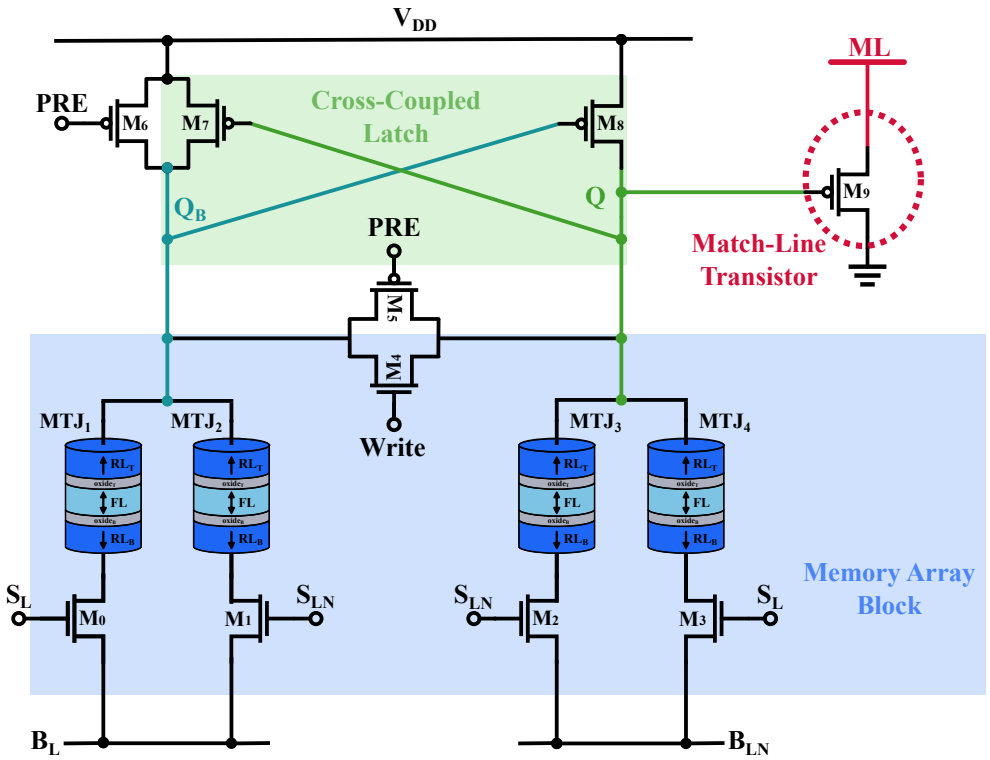

Figure 5.2: Circuit diagram for the 10T4MTJ NV-CAM cell [50].

The cross-coupled latch is made up from pMOS transistors M_7 and M_8 whose gates are connected to the drain of the other, forming the nodes Q and Q_B. Transistors M_5 and M_6 are used to pre–charge the latch. The output of this block drives the matchline pMOS transistor M_9, allowing the matchline to discharge to a 'weak' 0, lowering the ML swing and saving energy at the cost of higher search time.

The write operation is done in two phases to switch the outermost, and innermost DMTJs. The input signals and MTJ states are summarized in Table. 5.4. The $Write$ signal is set to V_{DD} to allow a current path through M_4. During phase 1, $S_L = V_{DD}$ and $S_{LN} = 0$, enabling the outermost DMTJs. The current paths are different for each device. For instance, when writing a '0', the bit-lines are set to $B_L = 0$ and $B_{LN} = V_{write}$, and a conductive path is formed from B_{LN} through MTJ_4, the write transistor, and MTJ_1; ending in

B_L. This current switches MTJ_4 to LRS. The voltage drop through MTJ_4 depends on the difference between V_Q, and V_{DD}. This write scheme requires boosting the search-line voltage to be able to produce a current higher than I_{C0} through all DMTJs transitioning from HRS→LRS. On the other hand, the switching current for MTJ_1 comes from V_{DD}, through the CCL and ends on B_L. This causes the device to switch rapidly to a HRS. When writing a '1', $B_L = V_{write}$, $B_{LN} = 0$, reversing the current paths and writing the states $MTJ_1 = LRS$ and $MTJ_4 = HRS$.

Table 5.4: Write Operations for the 10T4MTJ NV-CAM cell [50]

		Signals					**States DMTJ$_{1,2,3,4}$***	
Operation		S_L	S_{LN}	B_L	B_{LN}	$Write$	Initial	Final
Write '0'	I	V_{write}	0	0	V_{DD}	V_{DD}	L,H,L,H	H,H,L,L
	II	0	V_{write}	V_{DD}	0	V_{DD}	H,H,L,L	H,L,H,L
Write '1'	I	V_{write}	0	V_{DD}	0	V_{DD}	H,L,H,L	L,L,H,H
	II	0	V_{write}	0	V_{DD}	V_{DD}	L,L,H,H	L,H,L,H

* HRS and LRS states are abbreviated as H and L.

During phase 2, $S_L = 0$ and $S_{LN} = V_{DD}$, enabling the innermost DMTJs. To write a '0', the bit-lines are set to $B_L = V_{write}$, and $B_{LN} = 0$, writing the states $MTJ_2 = LRS$, $MTJ_3 = HRS$. Similarly, when writing a '1', the bit-lines are set to $B_L = 0$, and $B_{LN} = V_{write}$, switching MTJ_2 and MTJ_3 to HRS and LRS respectively. Just like during phase 1, a boosted voltage is used for the search-lines, resulting in a power penalty for applications with frequent writing.

The search operation is divided into two phases, pre–charge and evaluation. During pre–charge PRE, S_L and S_{LN} are driven to ground, disconnecting the MAB. The node Q_B is charged through transistor M_6, while transistor M_5 provides a path to charge node Q. At the same time, the matchline is charged to V_{DD} through an external transistor. During the evaluation phase, PRE is driven to V_{DD}, and the bit-lines are set to $B_L = 0$ and $B_{LN} = 0$ to provide a discharge path for the internal nodes Q, Q_B, according to the values set in the search-lines. Table. 5.5 summarizes the search-line, and bit-line inputs for each search operation.

The search '0' operation requires $S_L = 0$ and $S_{LN} = V_{DD}$ to enable a discharge

Table 5.5: Search Operations for the 10T4MTJ NV-CAM cell [50]

	Signals				**Stored Data**		**Matchline**
Operation	S_L	S_{LN}	B_L/B_{LN}	$Write$	Value	$DMTJ_{1,2,3,4}$ *	
Search '0'	0	V_{DD}	0	0	'0'	H,L,H,L	Match
	0	V_{DD}	0	0	'1'	L,H,L,H	Mismatch
Search '1'	V_{DD}	0	0	0	'0'	H,L,H,L	Match
	V_{DD}	0	0	0	'1'	L,H,L,H	Mismatch
Search 'X'	0	0	0	0	-	-	Match

* HRS and LRS states are abbreviated as H and L.

path for the CCL through MTJ_2 and MTJ_3. According to the difference in resistance of the stored devices, the nodes Q, Q_B are going to discharge at different rates, and the CCL is going to amplify the voltage difference, eventually driving node Q to either V_{DD} or 0. If a '0' is stored, $MTJ_2 = LRS$ and $MTJ_3 = HRS$. Then, Q_B is rapidly discharged through MTJ_2, and Q rises to V_{DD}. Transistor M_9 remains off, so the matchline is disconnected and does not discharge, resulting in a match. When a '1' is stored, a mismatch occurs with $MTJ_2 = HRS$ and $MTJ_3 = LRS$. Then, Q discharges rapidly to 0 and turns on M_9, connecting the matchline to ground. The pMOS transistor will only discharge the matchline until it reaches the transistor threshold voltage v_{th}, reducing the matchline swing and saving energy during the next pre–charge.
The search '1' operation sets $S_L = V_{DD}$ and $S_{LN} = 0$ to enable a discharge path for the CCL through MTJ_1 and MTJ_4. If a '0' is stored, $MTJ_1 = HRS$ and $MTJ_4 = LRS$, discharging node Q and causing a mismatch. If a '1' is stored, $MTJ_1 = LRS$ and $MTJ_4 = HRS$, and node Q remains high.
Finally, to search for an 'X', the MAB is disconnected by setting $S_L = 0$ and $S_{LN} = 0$. Therefore, nodes Q, and Q_B remain at V_{DD}, and the matchline transistor is turned off. The result is always a match.
During evaluation, there is always a direct current path from V_{DD} to B_L or B_{LN} through the DMTJ set to HRS, increasing the cell power consumption. The current will continue to flow through the entirety of the evaluation phase. To ensure that the stored data is not destroyed, the device is connected such that writing a HRS requires the same current polarity.

5.3.2 Design and Discussion

Table. 5.6 shows the transistor sizes for the 10T4MTJ cell designed under a $65nm$ technology node. The write operation is performed by the memory array block, and consists of two different write paths. DMTJs that switch from $HRS \rightarrow LRS$ have a 3T2MTJ write path, while those switching from $LRS \rightarrow HRS$ are assisted by the current flowing from V_{DD}, down the cross coupled latch. The 3T2MTJ path requires boosting the search-line voltage to ensure a write current above I_{C0}. A search-line voltage of 1.3V is used. Through iterative simulations of the circuit, the search-line transistors M_{0-3} width was set to $2\mu m$ with a write transistor M_4 of width $1\mu m$. Still, the design has a high write latency, and a big WER was found during the performance evaluation of the cell (Section 5.5). The best solution for this problem is to lower the resistance of the DMTJ devices. Indeed, the cell in [50] was designed with an MTJ model with $R_L = 3k\Omega$ and $R_H = 7.5k\Omega$, which are $\sim 6\times$ smaller than the resistances of the DMTJ model considered in this work.

Table 5.6: Transistor sizes for the simulated 10T4MTJ NV-CAM cell

Transistor Name	**Width (nm)**	**Length (nm)**
M0	2000	60
M1	2000	60
M2	2000	60
M3	2000	60
M4	1500	60
M5	200	60
M6	200	60
M7	200	60
M8	200	60
M9	200	60

The search operation depends on the cross–coupled latch. The performance of the latch was acceptable even when using standard size transistors. Still, some issues with the performance of the cell are aggravated due to the sizing of the search transistors (M_{0-3}). First, the voltage drop through the DMTJs reduces the TMR, which affects the sensing speed of the latch, and causes a greater number of search errors. Second, the short-circuit current during the

evaluation phase increases due to the lowered path resistance. Therefore, the energy consumption of the cell is impacted, and problems like reduced cycle endurance, and the risk of dielectric breakdown are worsened. The 10T4MTJ cell design has the worst search delay and energy consumption of all the desings presented in the performance evaluation of Section 5.5.

5.4 10T2MTJ

5.4.1 Cell Schematic and Operating Principles

Fig. 5.3 shows the 10-transistor 2 DMTJ (10T2MTJ) NV-CAM cell proposed by Garzón, Yavits, Finocchio, *et al.* [55]. The cell is made up from two main blocks, the voltage divider network (VDN) and the matchline switching network (MSN). The VDN contains the memory array consisting of MTJ_1 and MTJ_2, as well as the enable transistors M_0, M_1 and M_2. The stored data is encoded in the resistive states of both DMTJs. A '0' is represented by $MTJ_1 = LRS$ and $MTJ_2 = HRS$. A '1' is represented by $MTJ_1 = HRS$ and $MTJ_2 = LRS$. Finally, the array is able to store a ternary value 'X', but this work only considers the binary case. The sole function of M_2 is to allow writing the ternary 'X', so it may be omitted for a BCAM implementation.

The matchline switching network is made up from the pre–charge transistors M_3 and M_5, the sensing transistor M_4, and the dynamic buffer featuring an inverter formed by M_7, M_8 and the feedback transistor M_6. The MSN amplifies the output of the VDN to either 0 or V_{DD}, providing a full-swing signal that drives the matchline transistor M_9, enabling or disabling a matchline discharge path.

Unlike the cells discussed thus far, the write operation requires only a single phase. The signal inputs and MTJ states are summarized in Table. 5.1. During a write the bit/search-line voltages are set, and the enable signals are asserted $E_{n1} = E_{n2} = V_{DD}$, turning on transistors M_0 and M_1 and enabling a current path through the DMTJs. To write a '0', the bit/search-lines are set as $B_L/S_L = 0$ and $B_{LN}/S_{LN} = V_{DD}$, setting the state of MTJ_1 to LRS, and MTJ_2 to HRS. To write a '1' the lines are driven to $B_L/S_L = V_{DD}$ and

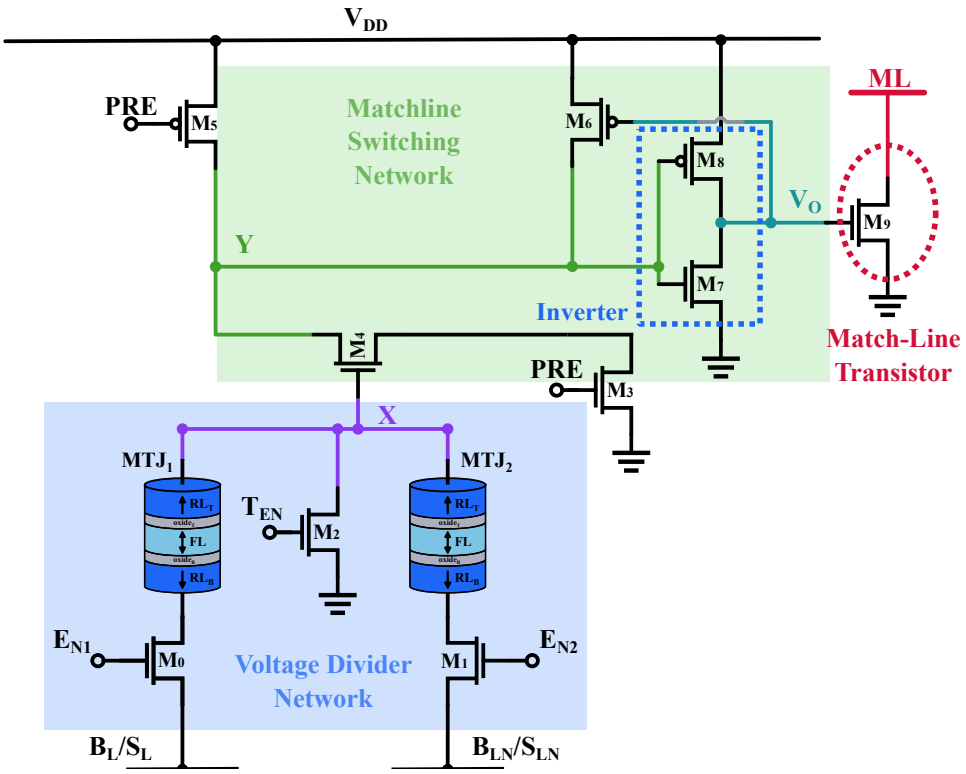

Figure 5.3: Circuit diagram for the 10T2MTJ NV-CAM cell [55].

$B_{LN}/S_{LN} = 0$, and an MTJ_1 is set to HRS while MTJ_2 is set to LRS.

Table 5.7: Write Operations for the 10T2MTJ NV-CAM cell [55]

	Signals					States DMTJ$_{1,2}$*	
Operation	E_{n1}	E_{n2}	T_{en}	B_L/S_L	B_{LN}/S_{LN}	Initial	Final
Write '0'	V_{DD}	V_{DD}	0	V_{DD}	0	H,L	L,H
Write '1'	V_{DD}	V_{DD}	0	0	V_{DD}	L,H	H,L

* HRS and LRS states are abbreviated as H and L.

The search operation is divided into two phases, pre–charge and evaluation. During pre–charge, PRE, E_{n1} and E_{n2} are driven to 0. In the MSN, node Y is pre–charged through transistor M_5. The enable transistors disconnect the DMTJs from the bit/search-lines. This causes the VDN to float and produce an uncertain voltage at the output node X. V_X may be high, turning on the sensing transistor. To avoid shorting V_{DD} to ground during pre–charge, footer transistor M_3 is added. The transistor is turned off when PRE is low to eliminate any short-circuit current. The inverter drives the output voltage V_O to 0, disabling the matchline transistor. The evaluation phase begins by

setting $B_{L/LN}/S_{L/LN}$ according to the desired search value, and raising PRE, E_{n1} and E_{n2} to V_{DD}. The voltage V_X modulates the channel resistance of M_4, changing the level of V_Y on the MSN divider formed by M_6, M_4 and M_3. Table. 5.8 summarizes the enable and bit/search-line inputs for each search operation.

Table 5.8: Search Operations for the 10T2MTJ NV-CAM cell [55]

	Signals				**Stored Data**		**Matchline**
Operation	E_{n1}/E_{n2}	T_{en}	B_L/S_L	B_{LN}/S_{LN}	Value	DMTJ$_{1,2}$*	
Search '0'	V_{DD}	0	0	V_{search}	'0'	L,H	Match
	V_{DD}	0	0	V_{search}	'1'	H,L	Mismatch
Search '1'	V_{DD}	0	V_{search}	0	'0'	L,H	Match
	V_{DD}	0	V_{search}	0	'1'	H,L	Mismatch
Search 'X'	V_{DD}	0	0	0	-	-	Match

* HRS and LRS states are abbreviated as H and L.

To search a '0', the bit/search-lines are set as $B_L/S_L = 0$, $B_{LN}/S_{LN} = V_{search}$, and the voltage divider network outputs a level at node X equals the voltage drop across MTJ_1 and the enable transistor. In case of a stored '0' MTJ_1 is in LRS, resulting in a low voltage level V_{XL}. A low gate voltage in M_4 produces a high channel resistance, and V_Y remains close to V_{DD}. The inverter drives V_O to 0, turning off the matchline transistor and indicating a match. For a stored '1', the state of MTJ_1 is HRS, resulting in a high voltage on X, V_{XH}. Then, the resistance across the channel of M_4 is low, and V_Y is discharged below the threshold of the inverter M_7,M_8. As the voltage V_O begins to rise, the feedback transistor M_6 is gradually turned off, causing V_Y to rapidly discharge towards 0. When V_O reaches V_{DD}, it turns on M_9 and the matchline begins to discharge, indicating a mismatch.

To search a '1', the bit/search-lines are set as $B_L/S_L = V_{search}$, $B_{LN}/S_{LN} = 0$, and the voltage output at node X equals the voltage drop across MTJ_2 and the enable transistor. If a '0' is stored MTJ_2 is in HRS, resulting in V_{XH} driving transistor M_4. V_Y is discharged and the matchline transistor is enabled indicating a mismatch. If a '1' is stored MTJ_2 is in LRS, and M_4 does not pull enough current to discharge V_Y. The matchline transistor remains off and the result is a match.

Finally, to search for 'X', both $B_L/S_L = 0$, and $B_{LN}/S_{LN} = 0$. The output of the VDN is $0V$, and transistor M_4 is completely off. Node Y stays charged at V_{DD}, and the matchline transistor is disconnected, resulting in match.
The VDN uses the same current path for the evaluation phase and the write operation, therefore there is a risk of data overwrite during search. To reduce the probability of unwanted writes, a voltage V_{search} lower than V_{DD} is used.

5.4.2 Design and Discussion

Table. 5.9 shows the transistor sizes for the 10T2MTJ cell designed under a 65nm technology node. The write operation is performed by the voltage divider network, which provides a 2T2MTJ write path, which provides a relatively slow search. To improve performance, the width of the enable transistors M_0 and M_1 were increased to $300nm$.

Table 5.9: Transistor sizes for the simulated 10T2MTJ NV-CAM cell

Transistor Name	**Width (nm)**	**Length (nm)**
M0	300	60
M1	300	60
M2	200	60
M3	1000	60
M4	1000	60
M5	200	60
M6	120	1000
M7	200	120
M8	200	60
M9	200	60

For the search operation, the cell design presents two challenges. First, the VDN shares the same path for writes and searches, requiring a low value for V_{search}. Ideally, V_{search} would be low enough to avoid sending a current higher than I_{C0} through the DMTJs, but the minimum value of V_{search} is also constrained by the required output in node X, namely the level of V_{XH}, and the sensing margin $V_{XH} - V_{XL} = \Delta V_X$. Given the MTJ characteristics and the available technology node, $V_{search} = 0.7V$ was chosen. The maximum search latency to ensure a switching probability of $p_{sw} = 10^{-6}$ (negligible overwrites)

is measured as $t_{ow} = 475ps$.

The second challenge involves the sensing transistor of the matchline switching network. The transistor M_4 amplifies the voltage difference between V_{XH} and V_{XL}, since even a relatively small variation in gate voltage can produce a noticeable change in channel resistance if the values are around the threshold voltage. Nonetheless, for the $65nm$ technology, the transistor threshold voltage is too high, and V_{XH} is unable to drive the sensing transistor M_4 and discharge node Y. To compensate for this issue, the width of M_4 and M_5 is increased to $1\mu m$. The length of the latch transistor M_6 was increased to further account for this problem, and to allow the discharge of node Y to go below the threshold of the inverter. M_6 has a width of $120nm$, and a length of $1\mu m$. All other transistors use the standard size.

Finally, the cell is able to operate in nominal conditions, but during the performance evaluation (Section 5.5) a significant SER was found due to threshold voltage variations rendering the MSN unusable, therefore only nominal results are reported. Additionally, the search latency is slightly higher than to t_{ow}, so data reliability cannot be ensured. The original cell in [55] was designed using a $28nm$ FDSOI technology node, and greater device TMR (187%), which circumvents the aforementioned challenges.

5.5 Performance Comparison

This section presents a comparative performance evaluation of all the NV-CAM cells discussed in this work. To ensure a fair comparison, all designs were implemented using the same TSMC 65nm process design kit (PDK) as well as the same physics–based Verilog–A compact model for the DMTJ devices. The MTJ switching time was simulated to achieve a target WER of 10^{-7}. The CAM cells were arranged as a 64-bit word, and results were measured at the 3σ corner after 1000 Monte-Carlo samples. The cell area for the 9T2MTJ, 10T4MTJ and 10T2MTJ cells was estimated using the scaling equations presented in [64]. Table. 5.10 summarizes the Figures of Merit (FOMs) for each alternative.

For the write operation, both the proposed 17T4MTJ cell and the 9T2MTJ cell use the same 1T1MTJ write path. This configuration provides the low-

Table 5.10: Figures of Merit for the explored NV-CAMs under the same conditions (65nm PDK, 64-bit word CAM, 1000 MC at 3σ)

	9T2MTJ	**10T4MTJ**	**10T2MTJ**	**17T4MTJ***
Technology	65 nm			
WER	10^{-7}	0.04	10^{-7}	10^{-7}
Word Size	64			
V_{DD} **(V)**	1.0	1.0	1.2	1.0
SER	14.60%	5.30%	>60%	0.20%
t_{search} **(ps)**	511.8	2,805.2	490.4‡§	287.8
E_{search} **(fJ)**	418.8	6,140.7	129.1‡	221.0
E_{search} **(fJ/bit)**	6.54	95.95	2.02	3.45
V_{write} **(V)**	1.0	1.3	1.2	1.0
V_{search} **(V)**	1.0	1.0	0.7	1.0
t_{write} **(ns)**	4.00	24.82	12.13	4.00
E_{write} **(fJ/bit)**	120.6	401.5	176.6	241.0
Cell Area†	1.35	1.63	0.84	1

* Proposed cell design.

† Area is shown relative to proposed cell.

‡ Value reported from nominal results.

§ Search time above $t_{ow} = 475ps$.

est write latency, achieving a t_{write} of $4.004ns$, which is 3× faster than the 2T2MTJ write path from the 10T2MTJ cell, and 6× faster than the least performing 10T4MTJ cell. In terms of energy, the 1T1MTJ path is also the most energy efficient per MTJ, with the 9T2MTJ cell consuming $120fJ$ per bit, and the proposed 17T4MTJ cell consuming $241fJ/bit$ to write to four DMTJs. The 17T4MTJ, 9T2MTJ and 10T2MTJ designs present a WER of 10^{-7}. However, the 10T4MTJ cell cannot reach the target WER, even after boosting the search-line voltage to $1.3V$.

The 10T2MTJ cell has a very high SER, resulting in unreliable search FOMs at the 3σ corner. Therefore, nominal values for search delay and energy are presented instead. For the search operation, the proposed 17T4MTJ cell achieves the lowest SER and search latency for a 64-bit CAM word. The 17T4MTJ cell offers a 26× SER improvement compared to the second most reliable design

(10T4MTJ cell). None of the other designs achieved a SER below 1% in their current implementation. This is mainly because the voltage-divider CAM cells present low match/mismatch sensing margins attributed to the TMR of 140%. The search time $t_{search} = 287.8ps$ is 43.8% lower than the 9T2MTJ cell, and $\sim 10\times$ faster than the worst performing 10T4MTJ design. The search delay for the 10T2MTJ cell is longer than t_{ow}, as discussed in the previous section, leading to undesired writes during search.

In terms of energy, the 17T4MTJ cell is the second most energy efficient design, consuming $3.45pJ/bit$, which is 47.24% less than the next best design. Due to the long delay, the wide search-line transistors, and the presence of shortcut currents, energy consumption for the 10T4MTJ design is an order of magnitude higher than the rest of the cells. The 10T2MTJ cell achieves the lowest search energy, using 41.55% less energy than the proposed 17T4MTJ design.

In terms of area, the 10T4MTJ cell is penalized by the need of very big transistors in the write path, while the 9T2MTJ and 10T2MTJ cells require long pMOS transistors in for the dynamic buffer. The cell area is reported relative to the proposed 17T4MTJ design. Despite having the highest transistor count, the 17T4MTJ cell provides a comparable area footprint, being only 15.8% bigger than the 10T2MTJ cell. This is due to the use of standard sized transistors.

Chapter 6

Conclusion

6.1 Conclusion

This thesis presented a STT–MRAM based NV-CAM design built upon the 17T4MTJ cell that considers a 1T1MTJ write path for all four DMTJs in the memory array block. The cell features a dynamic, latch-based, sensing scheme that amplifies the TMR output from the MAB to a full swing voltage driving the matchline transistor. The design was evaluated under 1000 Monte-Carlo simulations at the 3σ corner.

Simulations for a 64-bit CAM word show that the proposed design outperforms other cells previously defined in literature for both search and update operations. For write operations, the 1T1MTJ path provides the best performance, with a write latency of $4ns$, as well as lowest the write energy per MTJ ($\sim 60fJ$) with a total write energy per bit of $241fJ$. For search operations, its reliability is an order of magnitude above the competitors, with a SER of 0.2%. The proposed design also outperforms its competitors in search speed by 43.8%, with a energy per bit of $3.45pJ$, making it the second most energy efficient design. The use of standard sized transistors simplifies the design process and ensures a competitive area footprint, with only a 15.8% overhead compared to the most compact design.

The high–performance and reliability of the proposed 17T4MTJ design enables its use in memory-centric systems featuring a high frequency of search and update operations.

6.2 Research Output

The design and results obtained in this work were used as the basis for the content-addressable memory of a monolithic 3D associative processor (M3D AP). The performance results of the 17T4MTJ NV-CAM design were used during the circuit-level evaluation of M3D AP.

The article titled "Monolithic 3D-Based Non-Volatile Associative Processor For High-Performance Energy-Efficient Computations" [65] was accepted and published in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits.

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