UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio de Posgrados

Design of CMOS based Temperature Sensor

Proyecto de Investigación y Desarrollo

José Benjamín Zambrano Chávez

Marco Lanuzza, PhD
Director de Trabajo de Titulación

Trabajo de titulación de posgrado presentado como requisito
para la obtención del título de Magíster en Nanoelectrónica

Quito, 11/12/2020

UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

COLEGIO DE POSGRADOS

HOJA DE APROBACIÓN DE TRABAJO DE TITULACIÓN

Design of CMOS based Temperature Sensor

José Benjamín Zambrano Chávez

Nombre del Director del Programa:	Omar Aguirre
Título académico:	Doctor of Philosophy
Director del programa de:	Maestría en Nanoelectrónica

Nombre del Decano del colegio Académico:	César Zambrano
Título académico:	Doctor of Philosophy
Decano del Colegio:	Colegio de Ciencias e Ingenierías

Nombre del Decano del Colegio de Posgrados:	Hugo Burgos
Título académico:	Doctor of Philosophy

Quito, diciembre 2020

© DERECHOS DE AUTOR

Nombre del estudiante:	José Benjamín Zambrano Chávez
Código de estudiante:	207577
C.I.:	0926073347
Lugar y fecha:	Quito, 11 de diciembre de 2020.

ACLARACIÓN PARA PUBLICACIÓN

Nota: El presente trabajo, en su totalidad o cualquiera de sus partes, no debe ser considerado como una publicación, incluso a pesar de estar disponible sin restricciones a través de un repositorio institucional. Esta declaración se alinea con las prácticas y recomendaciones presentadas por el Committee on Publication Ethics COPE descritas por Barbour et al. (2017) Discussion document on best practice for issues around theses publishing, disponible en http://bit.ly/COPETheses.

UNPUBLISHED DOCUMENT

Note: The following graduation project is available through Universidad San Francisco de Quito USFQ institutional repository. Nonetheless, this project – in whole or in part – should not be considered a publication. This statement follows the recommendations presented by the Committee on Publication Ethics COPE described by Barbour et al. (2017) Discussion document on best practice for issues around theses publishing available on http://bit.ly/COPETheses.

Contents

List of Figures

List of Tables

Abstract

With the actual rising of IoT technologies the trending in sensors made for this purpose is to mainly have a low power/low energy consumption due to the use of batteries on these kind of portable devices that limits the current capabilities and energy storage while sacrificing the sensor performance thus the seek in more compact, power saving solutions are found in CMOS implementation.

This thesis describes the design of a CMOS based temperature sensor targeting low power consumption with acceptable performance, the whole circuit works at subthreshold region employs a current generator that provides two PTAT currents whose ratio is linear which are then used to feed differential ring oscillators with 2 and 8 stages to ensure high frequency ratio and finally this ratio would be digitized in the form of counting the faster signal pulses over one period of the slower one, thus the circuit does not need an external reference, the circuit without the digital backend was designed and simulated in 180nm commercial library from TSMC working at $0.2V$ of supply voltage with a temperature error of $-6°C/8°C$, an operating temperature range from $0°C$ to $100°C$ and consuming an average power of $2nW$ at room temperature ($25°C$).

I. Introduction

I.I Temperature sensing trends

The usual **approach** to measure temperature in non IoT environments is based on BJT devices along with analog to digital converter being capable of generating complementary-to-absolute temperature (CTAT) and proportional-to-absolute temperature (PTAT) characteristics generally exhibiting good linearity, this means of course low measurement error, but at the cost of high power consumption making them not useful for portable devices and on top of that they does not scale very well with supply reduction severely limiting scalability, hence the need to change the approach to be more energy saving, and this is where CMOS based temperature sensors are more appealing, due to the increasing Internet of things applications the needed of low power consumption sensors also has increased since battery life is now one of the most important features of portable devices and this energy saving feature can be achieved by CMOS based sensors as these can work with very low voltages depending on the design, but also this reduction in supply voltage can impact the measurement error of the sensor which depending on the application can has a different tolerance, hence, favoring less accurate circuits but with lower power consumption expecting it to be ideally in sub-μW territory.

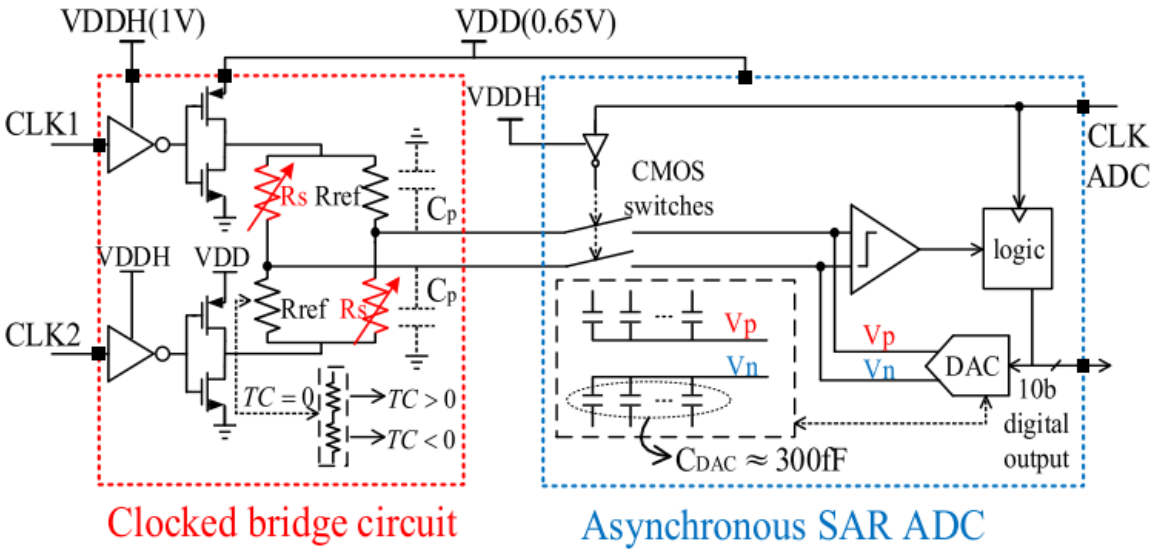

Figure 1.1: Architecture of Resistor based temperature sensor

I.I.I Reviewed sensing methods

I.I.I.1 Resistor based

This approach presented in [7] shows a dynamic architecture which can be adjusted to work at low power consumption ($174pW$) but slow measurement rate ($1S/s$), or higher power consumption ($488.3nW$) with faster measurement rate ($100kS/S$) and no change in resolution. The principle in which is based the translation of temperature into an electric signal is though a resistance that changes its value with temperature.

The architecture is shown in Figure 1.1 including a Wheatstone bridge to do the resistance-voltage conversion and an 10-bit asyncronous ADC to sample and digitalize the bridge output voltage, the temperature resistors resistors are made of nonsilice n-diffusion material whereas the reference use non-silicide p-poly and non-silicide n-poly resistors, something important to point out is the necessity of two different voltage levels, one at $1V$ and another of $0.65V$ this can be translated into the need of a level shifter. Showing a variable power consumption

the advantage of this circuit is the adaptability it has, also features a resolution of $0.61°C$, a inaccuracy of $-1.1°C/1.5°C$, this latter characteristics can change depending on the duty cycle. Another interesting feature of this work is the ability to enter in sleep mode after a conversion is completed, this is because of the nature of dynamic circuits.

I.I.I.2 CMOS based Voltage generators, digitized via capacitive charging [8]

This approach is based on designing two voltage generators, one as a reference, hence, constant with temperature (CWT) and another one proportional to temperature (PTAT), the two generators are depicted in Figure 1.2 having both of them a 3-transistor (3T) design which the authors indicate that are more linear and stable than the 2T approach, the CWT generator include an off-state NMOS used to improve line regulation, a tunable off-state PMOS and the lower transistor is a diode-connected NMOS whereas the PTAT voltage generators consists of two NMOS transistors with the same threshold voltage being the middle transistor (M1,PTAT) tunable and the upper transistor being used as a supply regulator. The sensor also includes a voltage-based capacitive charging-time-to-digital feedback for increased inaccuracy and finally a least significant bit (LSB) feedback algorithm to improve the conversion time.

The concept is to compare the output voltage of the PTAT voltage generator to a ramp voltage generated by charging a capacitor with a mirrored current that comes from the CWT voltage generator measuring its rising time and compare this time with another ramp generated by the same CWT reference but instead charging DAC capacitors by the LSM algorithm which are tunable making the rise time also tunable, the final idea is to match the rising time of both ramps, the solution and circuitry of this approach to measure temperature is complex being this a downside of the sensor, the architecture of this work can be seen in Figure 1.3 showing the general schematic with both voltage ramps generators and digital conversion circuitry in-

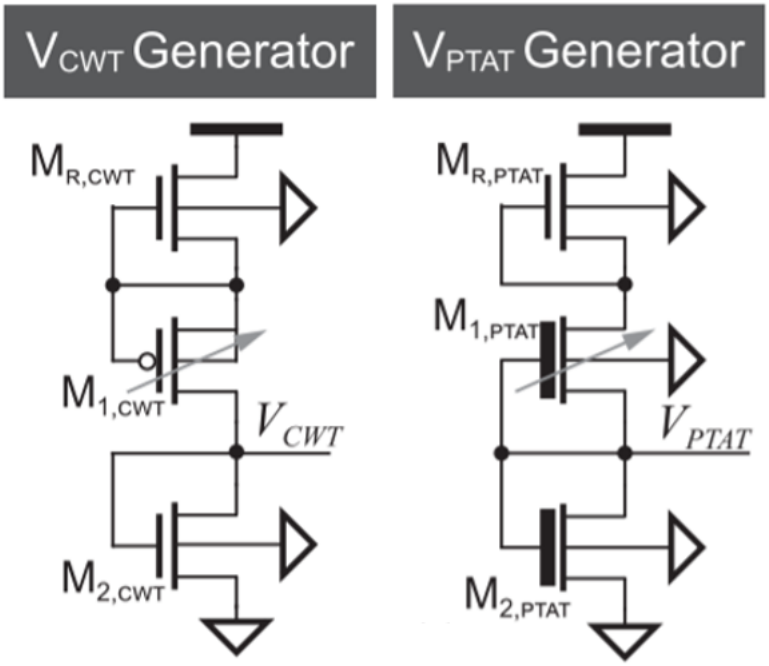

Figure 1.2: CWT and PTAT Voltage Generators

cluding the LSB-First SAR logic feedback. The maximum temperature error of this work is $-1.53°C/1.61°C$ in the range of $0°C - 100°C$, but after two point calibration is reduced to $-0.75°C/0.81°C$ with an average power consumption of $763pW$ at $20°C$ and operating with a supply voltage of $0.5V$, it is also reported that the whole circuit consumes less than $75nW$ in all the temperature range.

I.I.3 CMOS based current generator

This design is described in [1] it proposes to implement a temperature to current transducer first by having a temperature to voltage conversion and then by using a voltage-to-current converter obtain a current which will be used to feed an oscillator to finally be converted digitally by a frequency-to-digital converter implemented with a binary counter to get the corresponding digital code of the measured temperature, the power consumption of this solution will be

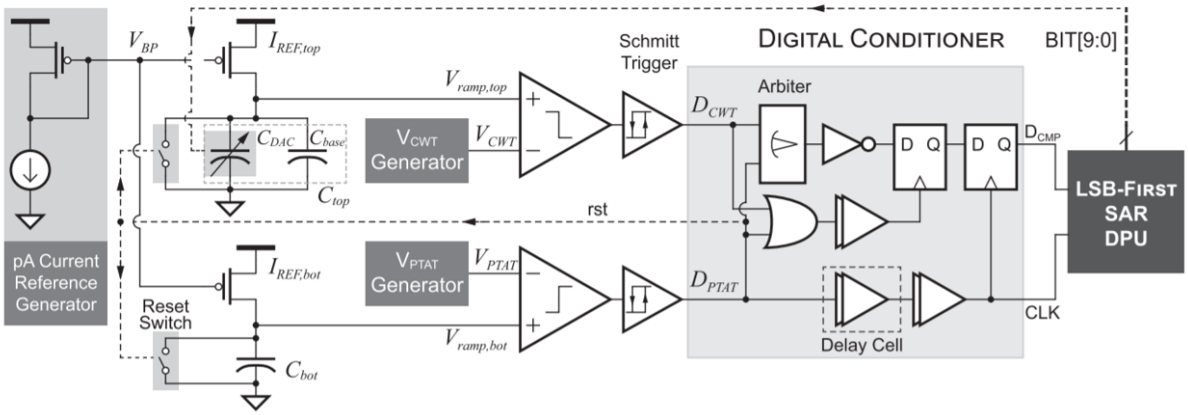

Figure 1.3: Architecture of fully integrated CMOS temperature sensor

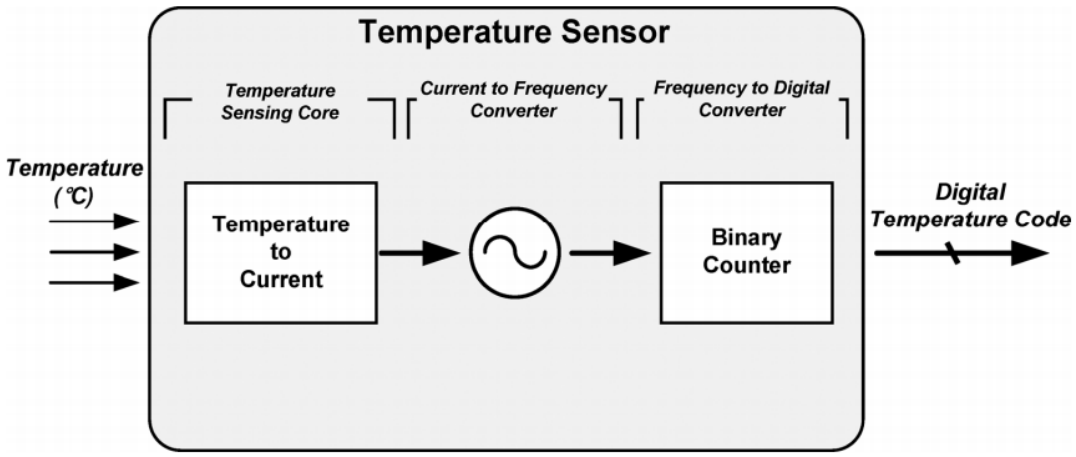

Figure 1.4: Block diagram of proposed sensor in [1]

dominated by the current generated by the first block of the Figure 1.4, depending on this current value the frequency of the oscillator will be determined thus relating directly into power consumption and that is the reason why the generation of the smallest possible current is a very important task of the design.

In Figure 1.5 is presented the sensing element, the output voltage of this element can be modeled by using the subthreshold relation of the MOSFET current taking into consideration second order effects such as DIBL and Body coefficients, applying the equation on both M1 and M2 devices, then, because of the devices connection the current across them is the same

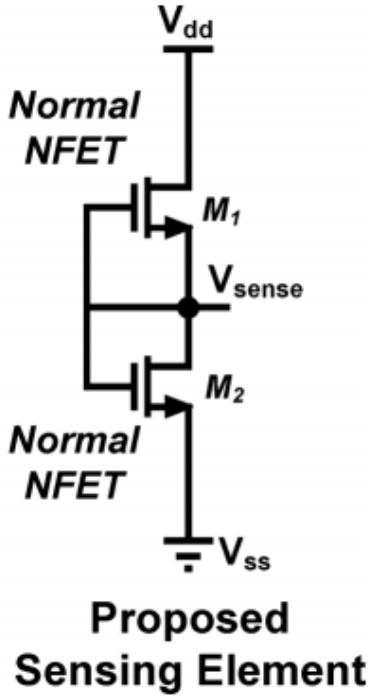

Figure 1.5: Sensing unit used in [1]

therefore the equations can be merged into a single one with the objective of finding a final expression for the output voltage V_{sense} which results as follow:

$$V_{sense} = \frac{m_1 m_2}{m_1 + \gamma_1' m_2} V_T ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1} \right) \tag{1}$$

The full derivation of this formula is detailed in the reference [1]. One important remark of this expression is that the threshold voltage does not appear making it ideally non V_{th} dependent and also mobility can be canceled, with this two parameters out of the equation a low variability feature can be achieved, this output voltage has a PTAT characteristic as can be seen that is proportional to the thermal voltage V_T. This solution final results have as output frequency range from $176kHz$ to $275kHz$, an inaccuracy of $-1.4°C/1.5°C$ with an average power consumption of $71nW$ at room temperature and a resolution of $0.3°C$ and a nominal supply voltage of $1.2V$.

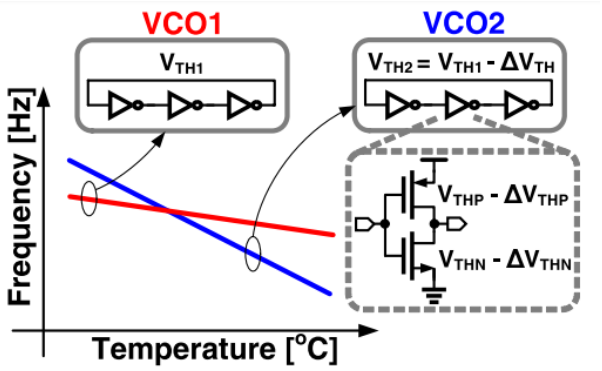

Figure 1.6: Two ring oscillators frequencies versus temperature as described in [2]

I.I.I.4 VCO based

The work proposed in [2] targets processor temperature sensing and is based in self referenced VCOs which frequency changes with temperature and the ratio of these frequencies will give a temperature readout, this approach exploits the fact that the temperature changes the frequencies of the oscillators through mobility or threshold voltage variations, thus changing either mobility, V_{th} or even supply voltage can lead to a change in temperature sensitivity, and was decided to induce threshold voltage changes to arise a temperature sensitivity difference among the VCOs. In Figure 1.6 is shown the behaviour concept of the two VCOs, as explained before the two oscillators have different temperature sensitivities having the devices of VCO2 smaller threshold voltage than those of VCO1 so the frequency of the output voltage of VCO2 will have a higher slope in comparison with the VCO1 due to having more mobility variation with temperature changes. The ratio of these two frequencies (F_{VCO1}/F_{VCO2}) will have a PTAT characteristic and then this ratio has to be digitized to obtain a digital value proportional to temperature. The threshold voltage difference could be classically done by either using two different types of transistors from the library (high threshold voltage and low threshold voltage flavors) and also by applying body biasing, having the two approaches different

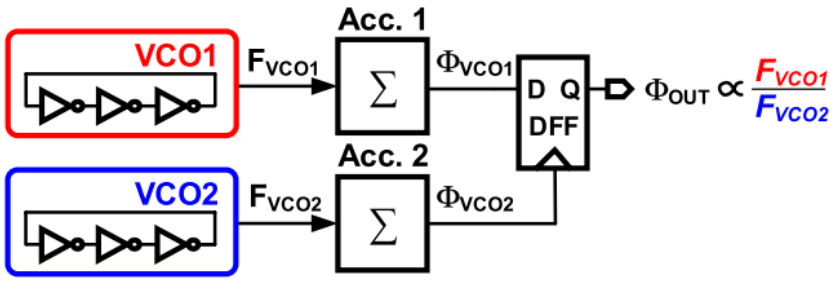

Figure 1.7: Simplified architecture proposed in [2]

downsides, in the case of body biasing there will be the need of using bandgap references and voltage regulators to apply the adequate biasing in the transistors whereas by using different types of devices implies the use of an extra mask in the fabrication process, so to avoid these downsides the authors preferred to exploit the RSCE (Reverse Short Channel Effect) which consists in an increase of the threshold voltage with the reduction in the channel length, this effect is caused by the presence of halo implants within the devices, and because of the selected technology node ($65nm$) this effect is known to be dominant therefore it can be used to create the desired threshold voltage difference using longer channel for transistors of VCO2 and smaller length for transistors of VCO1. The architecture depicted in Figure 1.7 consists of the two above mentioned ring oscillators followed by an accumulator and a latch the concept is that the accumulators give a phase output, when accumulator-2 reaches a threshold N the output of accumulator-1 is latched, in this way the output of the latch is proportional to the ratio of the frequencies in a simple way [2]. This sensor features also a nonlinearity correction circuit based on second-order polynomial correction block, this helps to reduce the inaccuracy from $\pm 2.3°C$ to $\pm 0.9°C$ and with the proposed architecture achieved a resolution of $0.3°C$ in a temperature range of $0°C - 100°C$ after a 2-point calibration, the downside of this work is the power consumption which is $154\mu W$ at $1V$ of supply voltage.

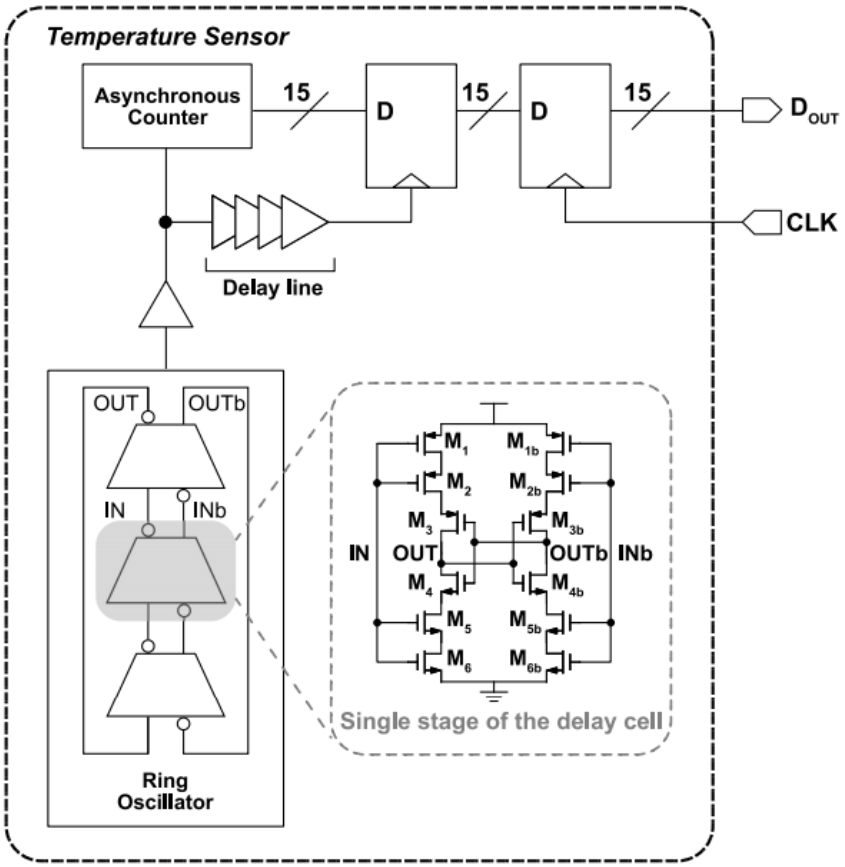

Figure 1.8: Proposed sensor in [3]

I.I.I.5 CMOS leakage current-based ring oscillator

In this brief is presented a CMOS temperature sensor for on-chip thermal monitoring, based on a ring oscillator whose frequency depends on leakage current and a frequency counter to convert this temperature dependent frequency to a digital output [3]. The schematic of the proposed sensor in this work is shown in Figure 1.8, it employs a CMOS ring oscillator, as described before, that uses leakage current to generate temperature dependent frequency due to the subthreshold current temperature dependence, this oscillator is composed of three differential delay stages, the frequency can be as low as $100Hz$ for SS corner at $0°C$ and as high as around $70KHz$ for FF corner at $100°C$ the relation between the logarithm of the frequency and

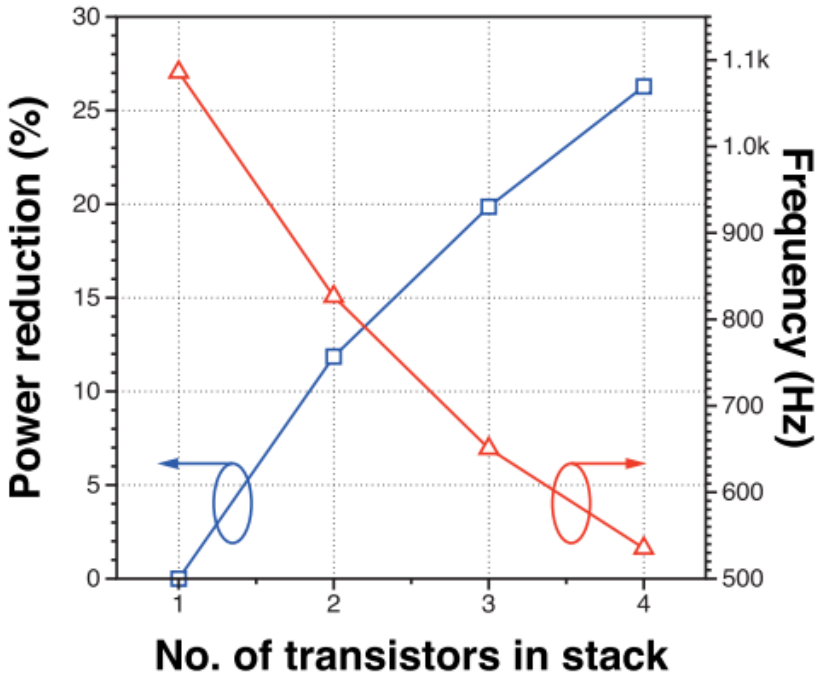

Figure 1.9: Frequency and power reduction as transistor stacking increases [3]

temperature is linear with a minimum R^2 correlation of 0.993, another feature that this circuit has is a good supply sensitivity exhibiting low frequency variability for supply voltage changes from $0.6V$ to $1.2V$ this is due to the subthreshold region operation of the delay cells, and this ability to resist supply voltage changes can be further increased by transistor stacking within the delay cells and also would help to reduce the power consumption but at the cost of conversion time due to the reduction in frequency output, this phenomena is depicted in Figure 1.9. It is used a 15-bit asynchronous counter after the ring oscillator to do the digital output conversion from frequency provided by the ring oscillator, a downside is the needed of a $3Hz$ external reference clock. For the final characteristics of this proposed sensor is obtained a frequency range of $0°C - 100°C$ with an inaccuracy of $-1.64°C/+0.67°C$ after 2-point calibration, a resolution of $0.55°C$, an area used of $0.007mm^2$ and a power consumption of $3.92nW$ at room temperature for $0.9V$ supply voltage.

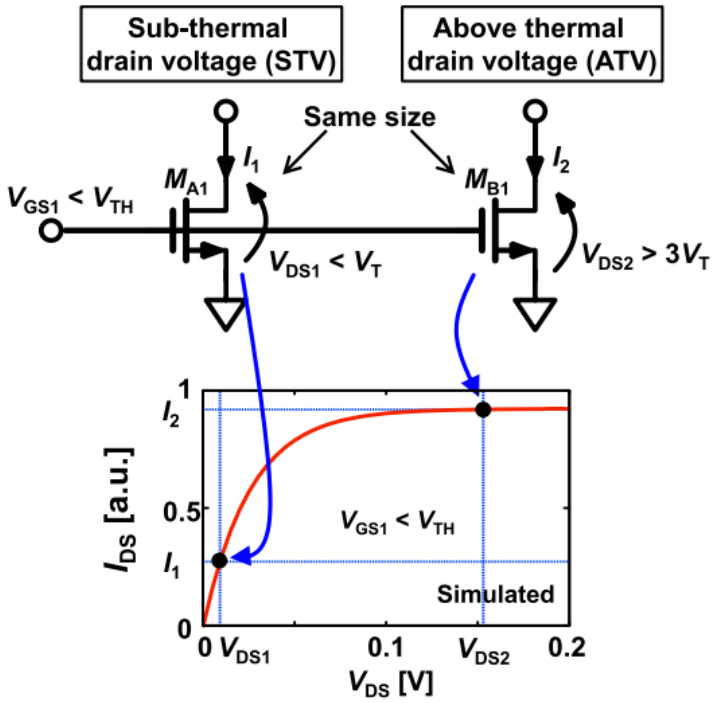

Figure 1.10: Current Generator concept from [4]

I.I.I.6 Different subthreshold currents ratio

The brief on [4] also proposes exploiting the subthreshold current temperature dependence by having a linear current ratio which has a PTAT characteristic and converting this currents to frequency to have an also PTAT frequency ratio and then digitizing this ratio to obtain a temperature measurement.

The principle of operation the current generator presented in Figure 1.10 is to have two nMOSFETS that work in subthreshold region and have different V_{DS} one of them well above the thermal voltage (typically larger than $3V_T$) and the other well below, so their drain current

can have the following model:

$$
\begin{aligned}
I_1 &= K \cdot exp\left(\frac{V_{GS1} - V_{TH}}{nV_T}\right) \cdot \left(1 - exp\left(\frac{-V_{DS1}}{V_T}\right)\right) \\
I_2 &= K \cdot exp\left(\frac{V_{GS1} - V_{TH}}{nV_T}\right) \\
\frac{I_2}{I_1} &= \frac{1}{1 - \left(\frac{-V_{DS1}}{V_T}\right)}
\end{aligned}
\tag{2}
$$

Notice that for I_2 the current expression that includes the drain-source voltage is gone due to the assumption of this voltage being well above the thermal voltage so this term can be discarded. Assuming that V_{DS1} is sufficiently smaller than V_T, I_2/I_1 is approximated as: [4]

$$
\frac{I_2}{I_1} = \frac{V_T}{V_{DS1}} + C \tag{3}
$$

From Eq. 3 can be clearly seen the linear relation between the thermal voltage and the current ratio, in Figure 1.11 is depicted the theoretical (dashed line) of the result in Eq. 2 and the measurements of the real circuit showing that the measurements actually are in agreement with the theoretical analysis in the range of $-20°C$ to $80°C$ with an error of 1% between the theory and the measurements. The nominal supply voltage of this proposed sensor is $0.8V$ with a resolution of $94mK$, with a inaccuracy of $-0.9°C/1.2°C$ and a power consumption of $11nW$.

I.I.I.7 Subthreshold oscillation dependence

This works presented in [5] has physical phenomena exploited: the subthreshold dependence of the current in MOSFET devices, and this is exploited in the form of a differential ring oscillator that works in the subthreshold region to have its frequency proportional to the surrounding temperature, including also a stacked native NMOS device used to achieve a better

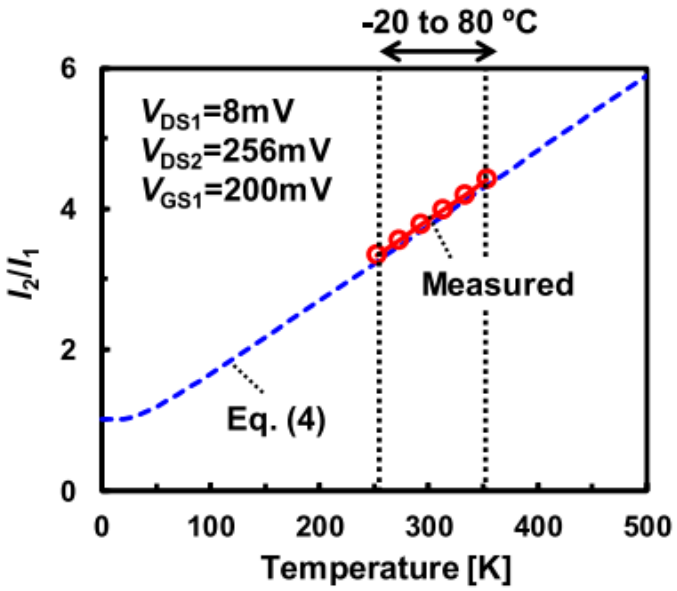

Figure 1.11: Theoretical and measured current ratio done in [4]

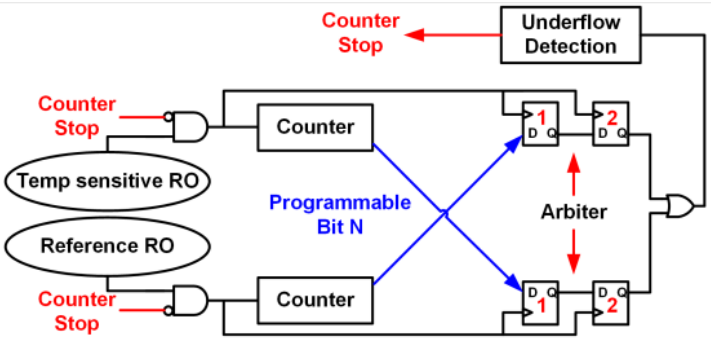

Figure 1.12: Diagram of the proposed sensor in [5]

supply sensitivity and ensure that the oscillator is working in subthreshold region and the most important part which is the delay cell that exhibits good current to frequency linearity giving robustness across process variations, however the circuit needs either a crystal oscillator or a RC oscillator, depending on the oscillator selection the circuit can have different inaccuracy being better with a crystal oscillator due to the more stable output frequency. The full temperature sensor consists of the ring oscillator that translates the temperature into frequency, the reference frequency and the sampling circuits, these are shown in Figure 1.12.

In Figure 1.13 is shown the delay cell used for the ring oscillator an the mathematical deriva-

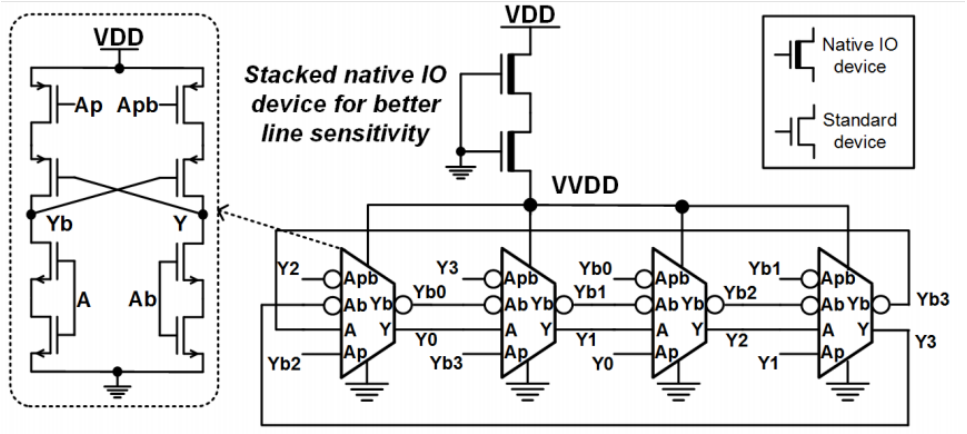

Figure 1.13: Delay cell and working principle of ring oscillator in [5]

tion presented leading to a 2-point calibration method that has to be used in order get the best performance of this circuit.

I.II Temperature dependent Current generation and sensing

From the reviewed literature it is noticed that either a PTAT or CTAT current generation process is usually done for temperature sensors mainly due to the fact that the current in sub-threshold region of MOSFET devices has a temperature dependence and the traditional way to sense this current changes is through an oscillator whose frequency changes with a provided current and finally digitizing this output, being basically a general diagram the one depicted in Figure 1.4.

The work done in [1] shows a sensing element that gives as output a PTAT voltage and with this voltage generate a current, in Figure 1.14 is depicted the basic structure to generate a current from a voltage source, the main issue is that to obtain sub-100nW power levels a very large resistance is required if the input voltage comes from a typical bandgap reference, hence the use of the proposed element shown in Figure 1.5 whose output voltage goes up around $100mV$, but it was not enough to achieve a low power operation, so there were changes to be made within

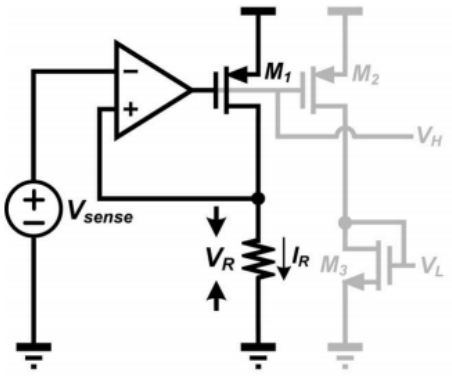

Figure 1.14: conventional scheme for current generation with a voltage source [1]

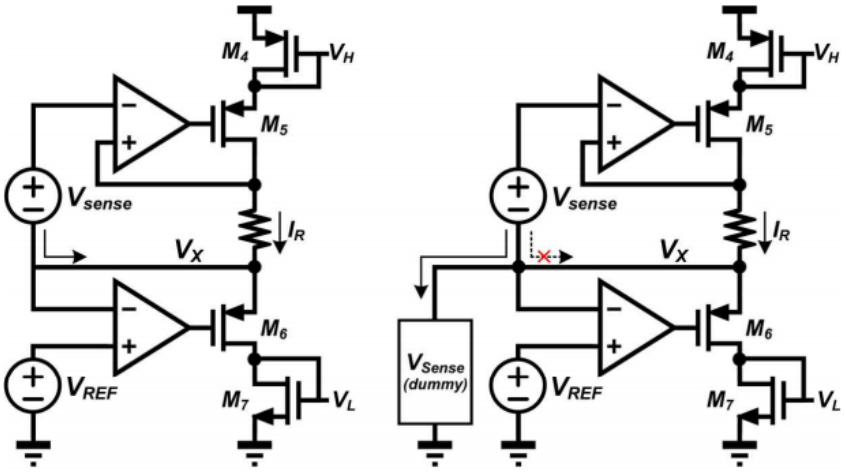

Figure 1.15: Improved versions of voltage-to-current converter [1]

the circuit. The introduction of another feedback loop and a reference generator shown in left circuit of Figure 1.15 and allows to have transistor M7 as a diode connected device being ready to mirror the current through its gate voltage, in contrast with the traditional circuit shown in Figure 1.14 in which the current is mirrored first by M1-M2 to produce V_H and then adding M3 to produce V_L whereas in this circuit the V_L voltage is directly produced in the same branch where current I_R is generated, thus saving power, but another issue arises in this approach, by having the ground of the sensing element V_{sense} connected to node V_x produces a change in the current I_R since the current flowing the sensing element will be added to I_R at node V_x

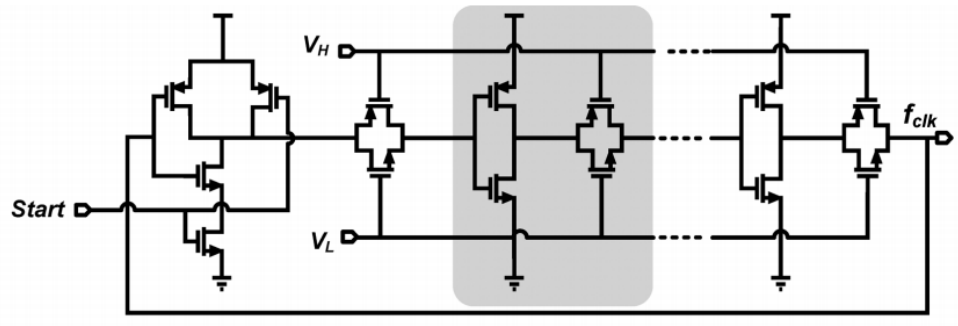

Figure 1.16: Ring oscillator used in [1]

producing a different current for M7 and introducing error at the mirroring, to counter this problem another sensing element is added as shown in the right circuit of Figure 1.15 consuming the same current as the upper sensing element and effectively deviating the current from I_R to ensure better mirroring. These generated voltages are used to feed a voltage-controlled ring oscillator (Figure 1.16) whose delay cell is composed of an inverter followed by a transmission gate that acts as a variable resistance controlled by voltages V_H and V_L [1], in order to the sensor to be self referenced is needed another current generator but this time to obtain a non temperature dependent current by using the exact same structure of the PTAT generator but with a CWT voltage reference, thus another oscillator is also required. The frequencies generated will be digitized by using asynchronous counters one for each oscillator, the counters will work until the reference counter overflows, then the read data is obtained for the PTAT counter, it is worth mentioning that the PTAT counter is designed in such a way that it will never overflows regardless the frequency of the ring oscillator.

Another interesting approach for PTAT current based temperature sensors is the one proposed by [4] which current generator concept was described in subsection I.I.I.6, this work follows the flowchart shown in Figure 1.17 and offers a slightly different digitization process

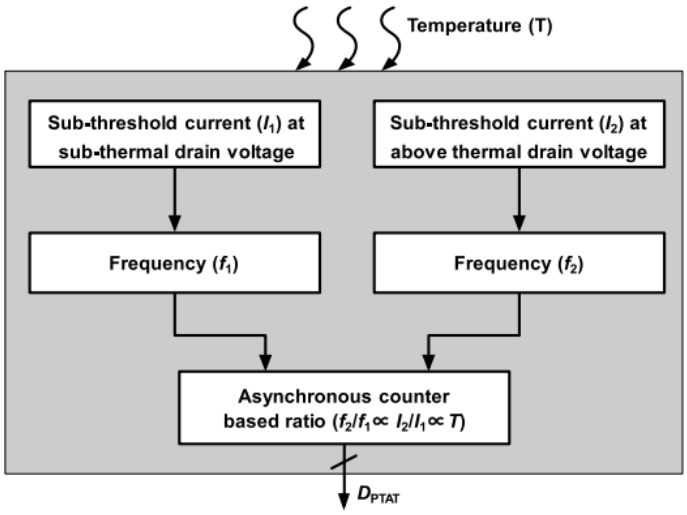

Figure 1.17: Flowchart of proposed temperature to digital converter in [4]

to what was presented in [2].

To ensure an above/below thermal voltage for the MOSFETs V_{ds} (Figure 1.10) it is required a circuit to regulate the voltages, this circuit is shown in Figure 1.18. The circuit uses a voltage reference that will be divided by a series of chain diodes (diode-connected transistors) to have two different voltage levels ($248mV$ and $120mV$) in the case of the ATV MOSFET the V_B voltage is the same as the M_{B2} transistor because they have the exact same current and ideally they are equal transistors so their gate-source voltages must be equal, so the drain-source voltage V_{DS2} of the ATV MOSFET will be $128mV$ that satisfies the condition of being well above the thermal voltage which is $30.43mV$ at $80°C$. On the other hand for the case of the STV MOSFET a transistor stack was needed in order to reduce its drain-source voltage to below thermal voltage levels, after increasing the transistor stack and simulating the issue was solved by a $16T$ stack to ensure a $8mV$ in V_{DS1} satisfying the below of thermal voltage condition for this transistor which in the worst case scenario of $-20°C$ is $21.8mV$.

The block diagram of the architecture proposed in [4] is shown in Figure 1.19, after converting the current to frequency through relaxation oscillators the signals are counted by asyn-

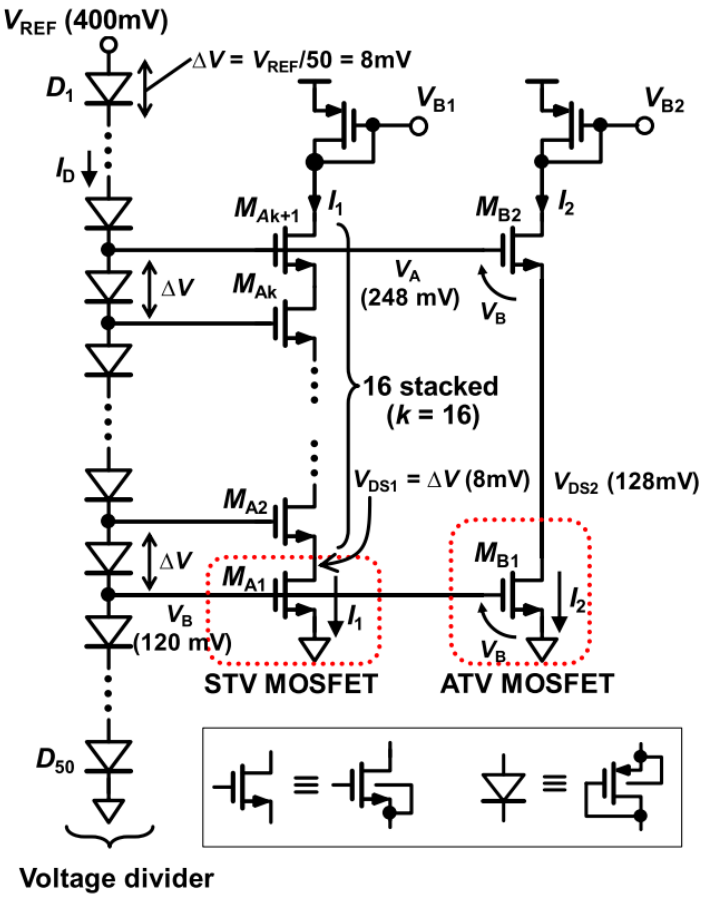

Figure 1.18: Full schematic of current generator used in [4]

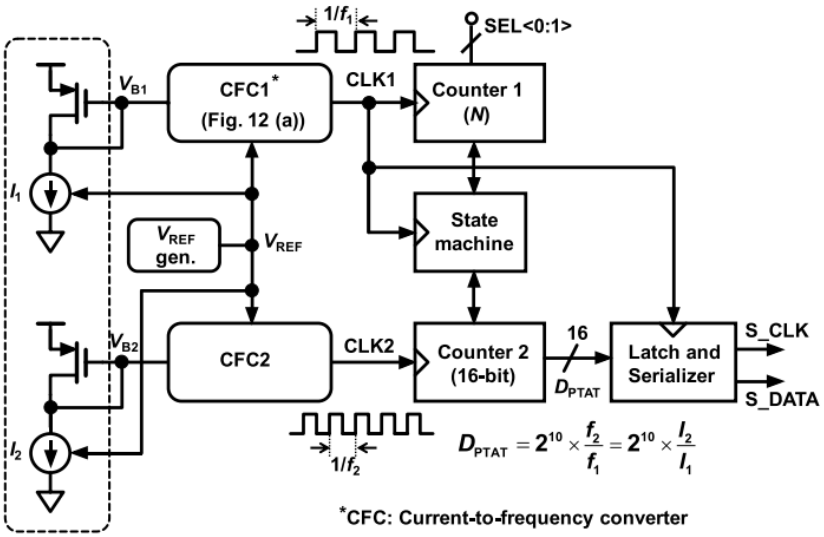

Figure 1.19: Architecture implemented in [4]

chronous counters, the counter in charge of the slower signal will count to a certain number N and then the output of the faster signal counter will be latched and serialized, the appealing feature of this solution is that the Counter 1 (slower signal) has a tunable number of bits, hence, a tunable maximum count number, as the count number is higher the time to reach that number will be also higher taking more time to finish the conversion and this will also mean that the faster signal will be counted more times effectively increasing the conversion time of the temperature measure into digital domain but also with the increased resolution effect due to the more refined counting and by allowing the Counter 1 to be tunable it introduces a trade-off between conversion time and resolution.

I.III Proposed work

For the present work it is highly taken into consideration the proposed solutions in [4] and [1] thus targeting an architecture similar of that of Figure 1.19 which employs a PTAT current generator a current-to-frequency converter and a digitizing block, the sensor is self referenced

so two currents are required being both of them PTAT with diferent sensitivity so their ratio will be also PTAT. For the current-to-frequency converters, directly current-starved ring oscillators are be used, initially the delay cell used on preliminary tests was composed of regular inverters but with added header and footer transistors (similar to the delay cell presented in [9]) acting as mirrored devices for the currents provided by the generator, oscillators were tested with both regular and low threshold voltage devices but among the downsides of this approach was the high number of stages required to recover the oscillator signal voltage swing because otherwise the circuit will have oscillation with very low output swing and in the worst case it will not oscillate at all, and also to actually have low frequency numbers having in mind always power consumption as an important constraint of the design, the circuit oscillation is also heavily dependent on the current provided and it was not so easy to obtain good results in terms of linearity as temperature changed, therefore other options were explored, first to try to reduce the output frequency without increasing in a great manner the number of stages delay elements were introduced in between the oscillator stages although this solution reduces the output frequency it compromised to much the oscillator linearity which in itself was not that good since the beginning. There were also other oscillator architectures with differential cells such the ones presented in [5] and [3] but these solutions offered oscillators whose frequency already was temperature dependent and that feature was not adjusted to what was the work target because the lack of any external control scheme such current or voltage. After reviewing the proposed work in [6] there was an appealing current-starved differential ring oscillator with up to $130KHz$ output frequency which circuit is shown in 1.20 and its delay cell is presented in 1.21.

Although the relative low output frequency presented in the brief the results obtained ini-

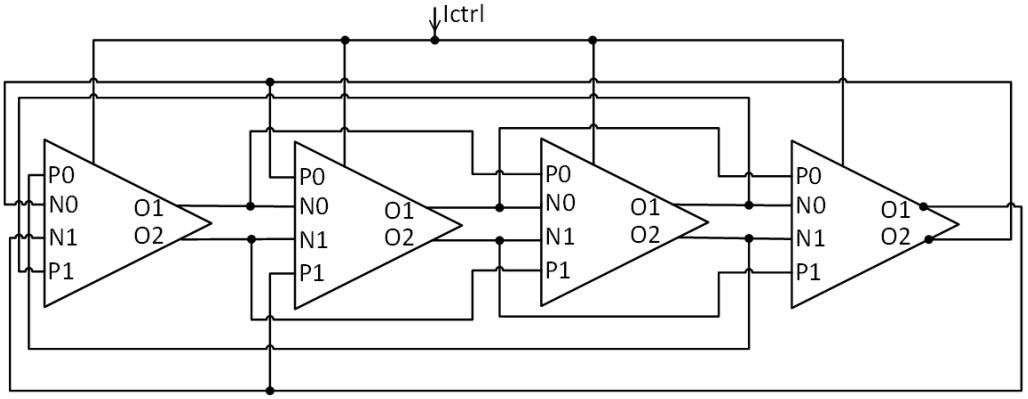

Figure 1.20: Differential Ring Oscillator used on [6]

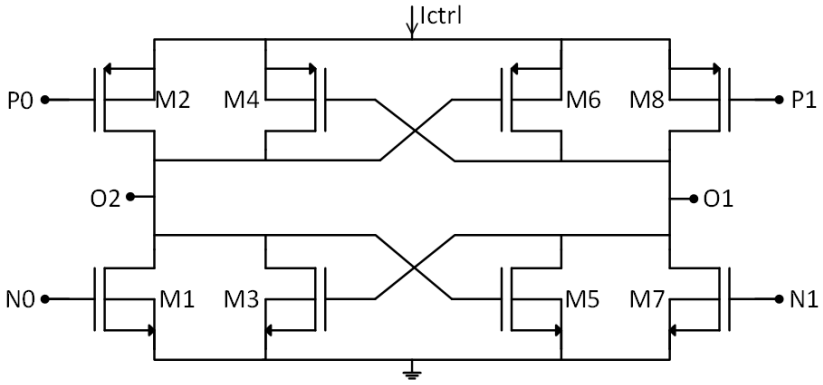

Figure 1.21: Delay Cell used in the differential ring oscillators

tially were not satisfying due to the very high frequency output reaching in some cases MHz territory despite the fact of using the same number of stages. From what was proposed in [10], which is not a sensor related work but its delay cell was modified in [6], and it was useful to have a better insight in what kind of sizing the devices should have to obtain more appealing results thus by having this as a starting point the circuit will be tuned to what was desired.

Finally as digital backend a simple solution was chosen which consists in counting the number of pulses of the high frequency oscillator output that exists in a single pulse of the lower frequency oscillator, this is a simple way to measure the frequency ratio but since it counts directly an integer number of pulses the resolution is severely affected due to the inability of having an opportunity to perceive a fractional frequency ratio, it is also worth mentioning that this backend will not be designed in the present work.

I.IV Linearity Measurement Approach

In order to measure linearity two approaches were used in this work, for the current generators was used the calculation of the Adjusted R-squared which is a number that can go from 0 to 1 meaning the highest value a perfect linearity. The calculation of this coefficient was done on Matlab by using the fitlm function which creates a linear regression model by fitting to a given data set.

In Figure 1.22 is shown the difference in linearity for values of 0.999 and 0.9999, for the former one can be clearly seen that the error is higher at the edges of the independent variable range and this trending will be seen in later simulation graphs, this value of linearity was taken as a threshold for the current generator as this circuit has to be the most linear possible so this

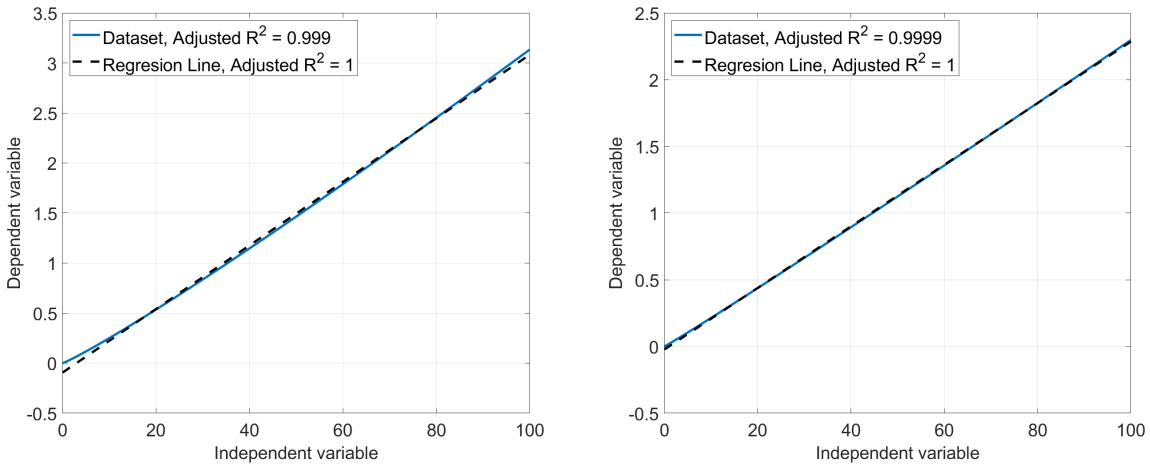

Figure 1.22: Linearity measure examples

strict method was used to ensure high linearity at this part of the circuit.

For the ring oscillator part of the design was used another approach based on the same regression line but measuring error directly not pure linearity and to accomplish this was necessary for every point of the simulation data (the frequency ratio) find the same value on the regression line then make the subtraction of the two x-axis values corresponding to the points in simulation data and regression line, this difference will give the error in temperature at the best scenario the corresponding x-axis (temperature) of the point will be the same of the simulation data meaning the regression line and the simulation data are overlapped which is an ideal behaviour.

To explain better the idea it is worth to take a look at Figure 1.23 which shows a nonlinear data an its corresponding regression line from the datatips shown can be appreciated the difference in the data and the regression line to obtain the same value in the dependent variable in this case is 8.701, for the data the corresponding independent variable is 95.7 (this is the real value of the measure) while on the regression line is 100 meaning a difference of 4.3 so this will be the error when doing this specific measure point.

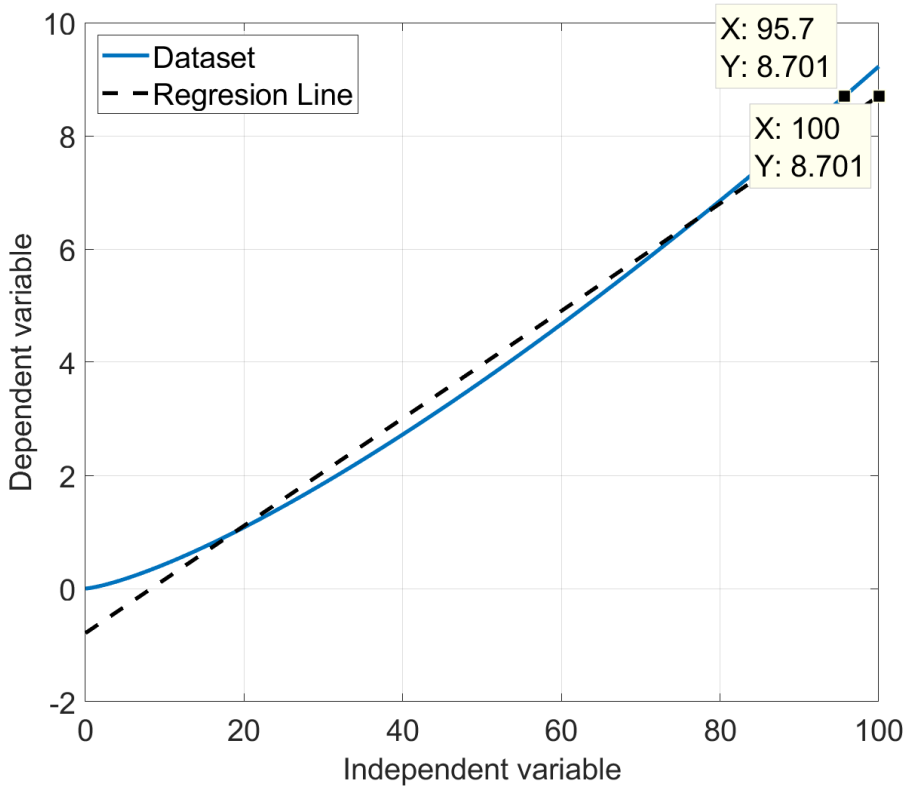

Figure 1.23: Error measurement example

II. Current Generator Circuits

There were two options explored for the PTAT current generation, both of them based on exploiting subthreshold temperature dependence of MOSFET current, this dependence can be apreciated in Eq. (4)

$$I_{ds} = I_0 \left(\frac{W}{L}\right) e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)} \tag{4}$$

Where:

I_{ds} is the drain-source current

I_0 is the intrinsic current

V_{gs} is the gate-source voltage

V_{gs} is the threshold voltage

n is the ideality factor

V_T is the thermal voltage

II.I First Current Generator Circuit

The first proposed circuit is shown in Figure 2.1, the general idea is to have two different PTAT (Proportional To Absolute Temperature) currents, one flowing through M1-M3 and the other through M2-M4, then the goal is that the ratio of the currents has a linear behaviour.
The analysis of this circuit must be done on two parts, the lower and the upper part, we will start first analyzing the lower part shown in Figure 2.2.

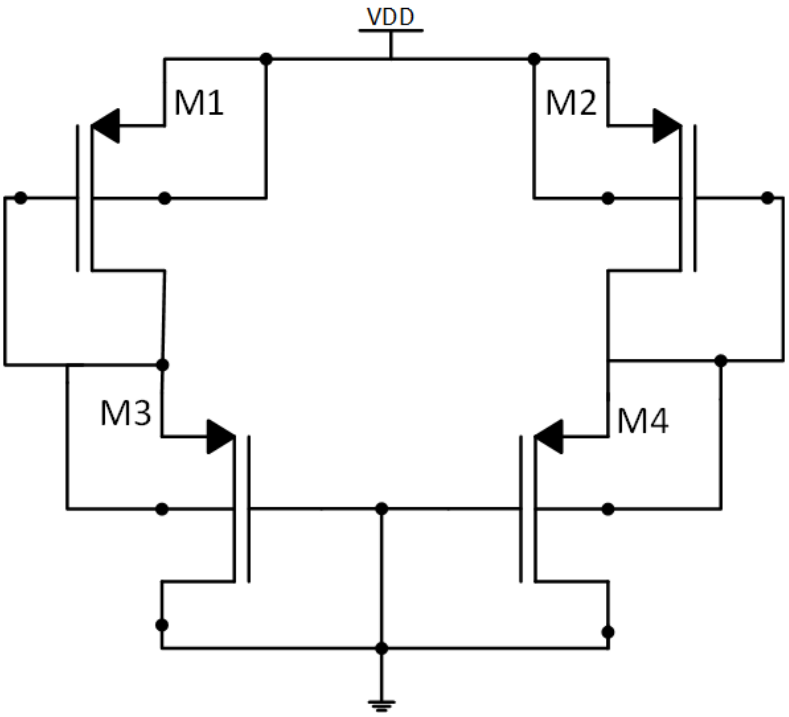

Figure 2.1: Current Generator Initial Idea

First we will assume transistors M3 and M4 are in subthreshold region so the starting point for

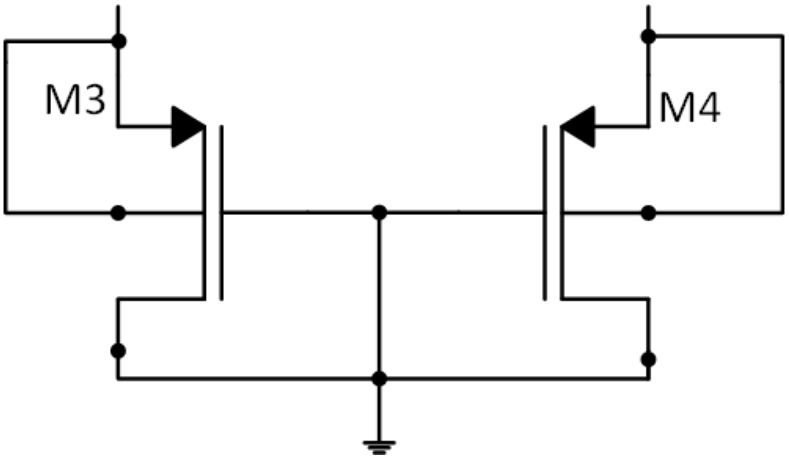

Figure 2.2: Current Generator Lower part

the analysis is the Eq.(5), noticing that the gate of both transistors are grounded this term does

not appear in the equation just the source voltage of the transistors.

$$I_{3,4} = I_0 \left(\frac{W}{L}\right)_{3,4} e^{\left(\frac{V_{s3,4}-V_{th3,4}}{nV_T}\right)} \tag{5}$$

The target is to find an expression for the source voltages of the transistors $V_{s3,4}$.

$$\begin{aligned} \left(\frac{I_{3,4}}{I_0}\right)\left(\frac{L}{W}\right)_{3,4} &= e^{\left(\frac{V_{s3,4}-V_{th3,4}}{nV_T}\right)} \\ nV_T \cdot ln\left(\frac{I_{3,4}}{I_0}\left(\frac{L}{W}\right)_{3,4}\right) &= V_{s3,4} - V_{th3,4} \\ V_{s3,4} &= nV_T \cdot ln\left(\frac{I_{3,4}}{I_0}\left(\frac{L}{W}\right)_{3,4}\right) + V_{th3,4} \end{aligned} \tag{6}$$

Now we can define a differential voltage of both sources of the transistors such that:

$$\begin{aligned} \Delta V_s &= V_{s4} - V_{s3} \\ \Delta V_s &= nV_T \cdot ln\left(\frac{I_4/I_0}{I_3/I_0}\frac{(W/L)_3}{(W/L)_4}\right) + V_{th4} - V_{th3} \end{aligned} \tag{7}$$

And the current for M3 is the same of that for M1, the same can be said for M4 and M2 giving:

$$\begin{aligned} I_3 &= I_1 \\ I_4 &= I_2 \\ \Delta V_s &= nV_T \cdot ln\left(\frac{I_2}{I_1}\frac{(W/l)_3}{(W/l)_4}\right) + V_{th4} - V_{th3} \end{aligned} \tag{8}$$

With this expression ends the analysis of the lower part, now moving onto the upper part analysis, which is shown in Figure 2.3, this derivation is pretty much similar of that from the lower part.

The starting point will be the subthreshold relation for M1 and M2 shown in Eq. (9).

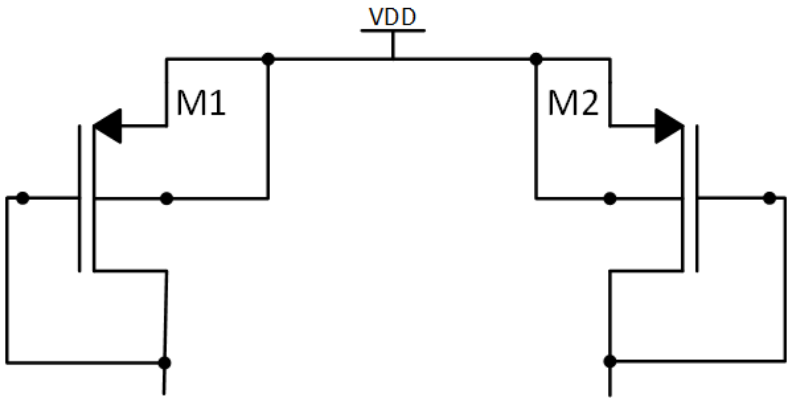

Figure 2.3: Current Generator Lower part

$$I_{1,2} = I_0 \left(\frac{W}{L}\right)_{1,2} e^{\left(\frac{V_{sg1,2}-V_{th1,2}}{nV_T}\right)} \tag{9}$$

By doing a similar analysis from that of the lower part we can obtain an expression for the gate-source voltages of M1 and M2:

$$V_{sg1,2} = nV_T \cdot ln\left(\frac{I_{1,2}}{I_0}\left(\frac{L}{W}\right)_{1,2}\right) + V_{th1,2} \tag{10}$$

Now will be defined the differential voltage for the same nodes, this is the drain of M1 and the source of M3, and the drain of M2 and the source of M4, let's call the difference of this nodes as ΔV_s.

$$\begin{aligned} \Delta V_s &= V_{dd} - V_{sg2} - (V_{dd} - V_{sg1}) \\ \Delta V_s &= V_{sg1} - V_{sg2} \end{aligned} \tag{11}$$

Applying this latter relation in Eq. (10) we obtain:

$$\Delta V_s = nV_T \cdot ln\left(\frac{I_1}{I_2}\frac{(W/L)_2}{(W/L)_1}\right) + V_{th1} - V_{th2} \tag{12}$$

The next step is to combine the final expression in Eq. (8) with the last expression obtained and also calling the difference of the threshold voltages of M1 and M2 $DeltaV_{th1,2}$.

$$\Delta V_{th1,2} = V_{th1} - V_{th2}$$

$$nV_T \cdot ln\left(\frac{I_2}{I_1}\frac{(W/L)_3}{(W/L)_4}\right) + V_{th4} - V_{th3} = nV_T \cdot ln\left(\frac{I_1}{I_2}\frac{(W/L)_2}{(W/L)_1}\right) + \Delta V_{th1,2} \tag{13}$$

If transistors M3 and M4 are exactly the same it can be said that their respective threshold voltages are equal, also for their aspect ratio.

$$\begin{aligned} V_{th3} &= V_{th4} \\ \left(\frac{W}{L}\right)_3 &= \left(\frac{W}{L}\right)_4 \end{aligned} \tag{14}$$

So the Eq. (13) turns into:

$$nV_T \cdot ln\left(\frac{\frac{I_2}{I_1}}{\frac{I_1}{I_2}\frac{(W/L)_2}{(W/L)_1}}\right) = \Delta V_{th1,2} \tag{15}$$

As specified before the target of the current generator circuit is to have a linear currents ratio so it is needed to find an expression for the currents ratio:

$$ln\left(\frac{I_2\sqrt{(W/L)_1}}{I_1\sqrt{(W/L)_2}}\right)^2 = \frac{\Delta V_{th1,2}}{nV_T}$$

$$\frac{I_2\sqrt{(W/L)_1}}{I_1\sqrt{(W/L)_2}} = e^{\frac{\Delta V_{th1,2}}{2nV_T}} \tag{16}$$

$$\frac{I_2}{I_1} = \sqrt{\frac{(W/L)_2}{(W/L)_1}}e^{\frac{\Delta V_{th1,2}}{2nV_T}}$$

Defining R as:

$$R = \frac{(W/L)_2}{(W/L)_1} \tag{17}$$

The final expression can be obtained just by replacing Eq (17) into the later expression of Eq. (16).

$$\frac{I_2}{I_1} = \sqrt{R}\cdot e^{\frac{q\Delta V_{th1,2}}{2nK_BT}} \tag{18}$$

In Eq. (18) it can be easily assumed that the relation is not linear but exponential with temperature which is, of course, correct, but the relation can be linear with the right value of $\Delta V_{th1,2}$ which is around $100mV$ as shown in Figure 2.4.

In order to obtain this threshold difference it was necessary to introduce a change into the initial circuit idea, this consists in replace M1 with a 5 transistor stack to further enhance the threshold voltage difference, this proves that linearity was indeed better and in addition it was improved by introducing a feedback at the cost of reduced Current Ratio. In Figure 2.5 is shown this idea, the transistors at the left branch will give a smaller current due to the stack and also

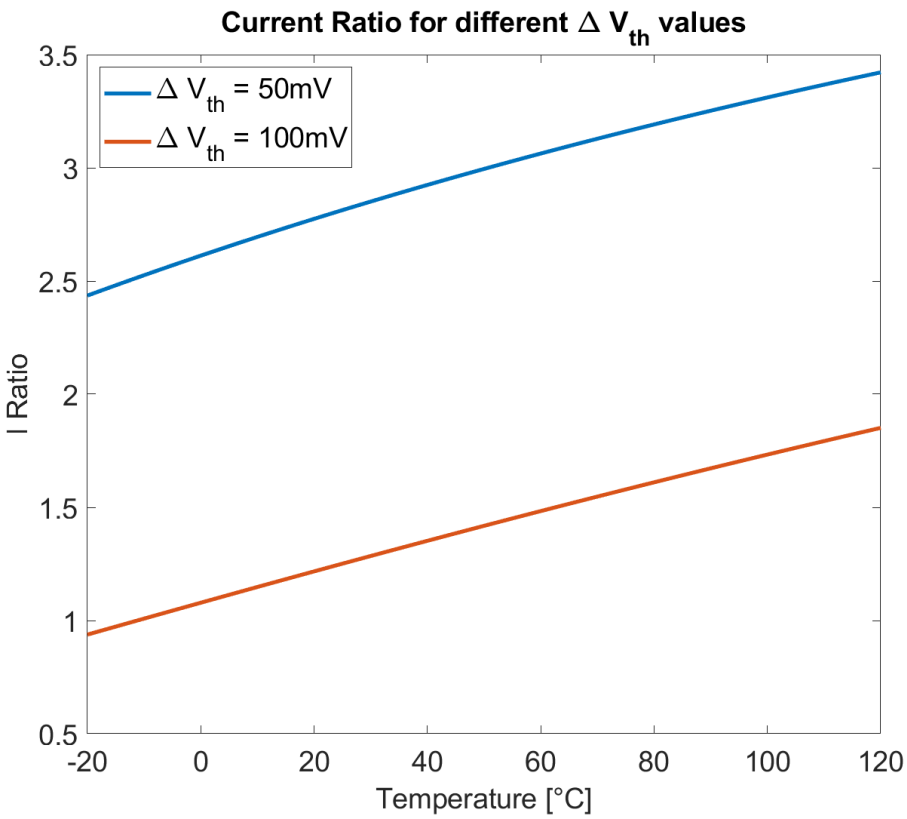

Figure 2.4: Current Ratio Linearity simulation in Matlab

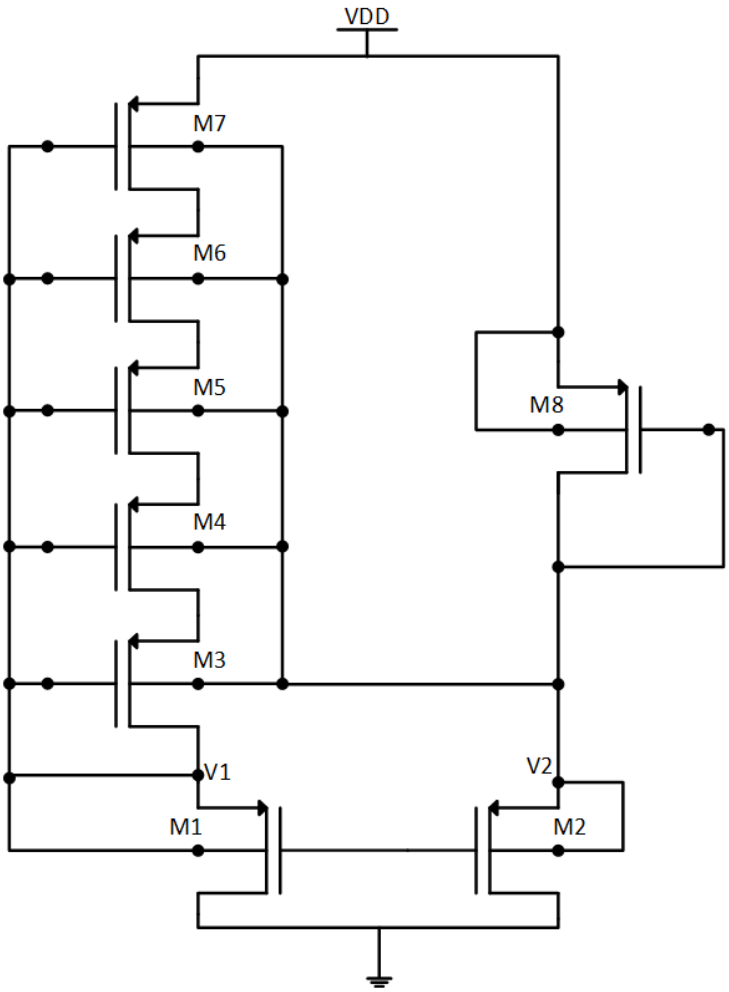

Figure 2.5: Current Generator final circuit

	W [μm]	L [μm]
M1,2	2	1
M3-7	2	2
M8	80	1

Table 2.1: Sizing for circuit presented in Figure 2.5

will have a higher threshold voltage. The current on the right side will be of course higher.

II.II Simulation Results

On left side of Figure 2.6 can be appreciated the current behaviour of the circuit, both of them are exponential as expected, obeying the subthreshold current equation as explained in Section II.I and exhibiting a highly linear ratio going from about 4.7 up to 9 in the -20 to $120°C$, the main advantage of the circuit is the linearity for the given $V_{dd} = 0.5V$ but the ratio itself is low, this means that the ratio must be greatly enhanced by the ring oscillator while maintaining good linearity in order to have more temperature resolution and less measurement error.

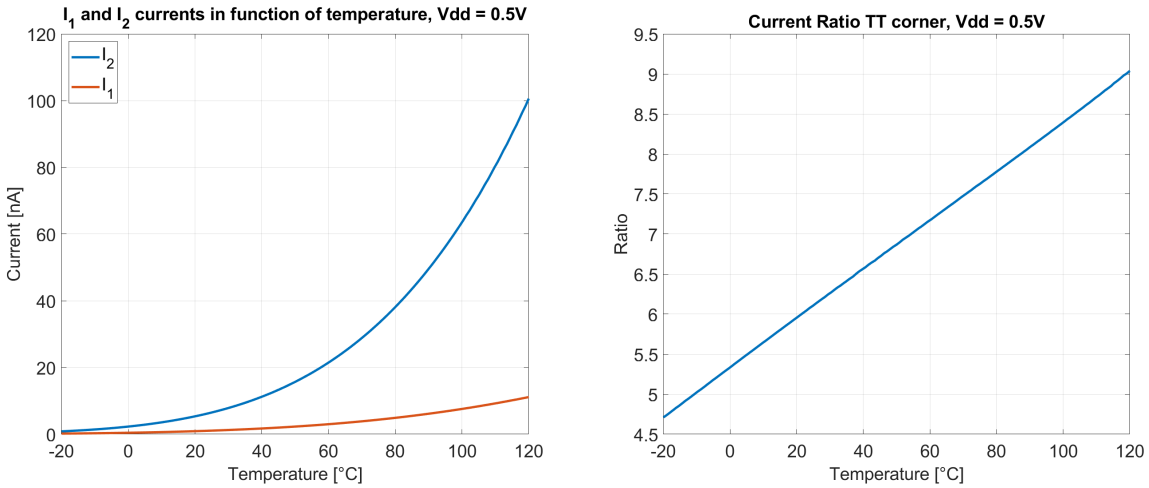

Figure 2.6: First Current Generator Operation

Now it is necessary to do process variation testing to see the circuit's robustness, results are shown in Figure 2.7 and can be seen that for all corners the results exhibit a very high linearity,

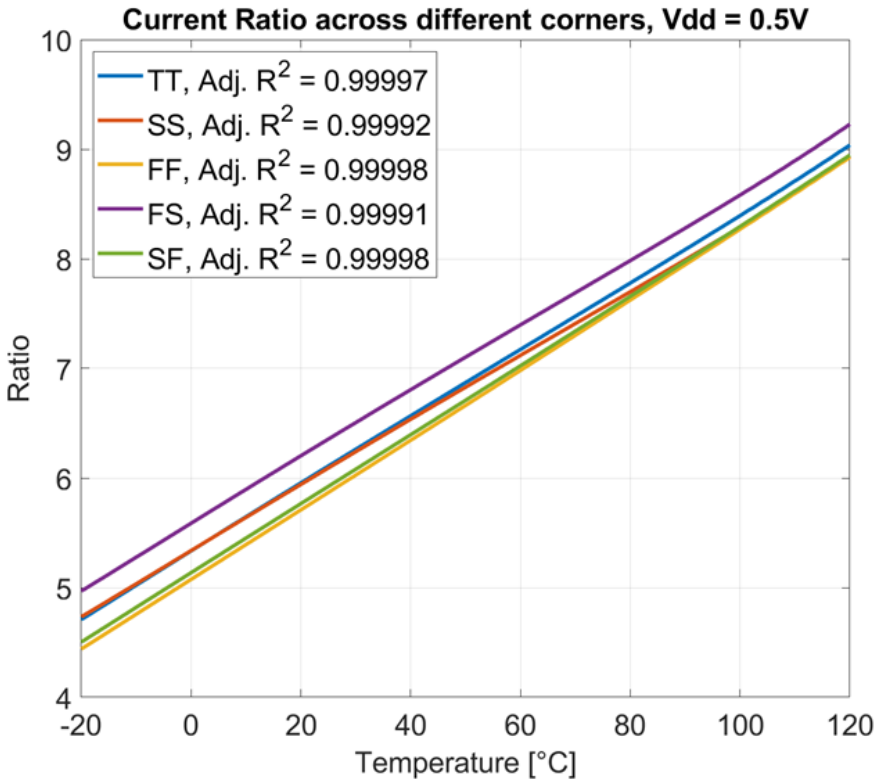

Figure 2.7: Current Ratio across all corners

the only downside is that with different corners the ratio has different slope meaning the need to use two-point calibration on each chip.

For mismatch testing 3000 runs per each corner were done to ensure we have a realistic result, which can be seen in Figure 2.8, in this case the circuit also proves to be robust in terms of mismatch changes exhibiting high linearity across all corners and showing that the worst corner is the SS one, but even in this worst case, linearity is still high enough.

The circuit had to be tested with supply voltage changes to see a usable range, results shown in Figure 2.9 indicate that the circuit can work quite good from $0.4V$ up to $0.8V$ in which voltage on the FF corner we obtain the worst case in terms of linearity, but it is still good enough to ensure a not so high error measurement.

Taking from Figure 2.9 the best, average and worst case scenarios for linearity across all

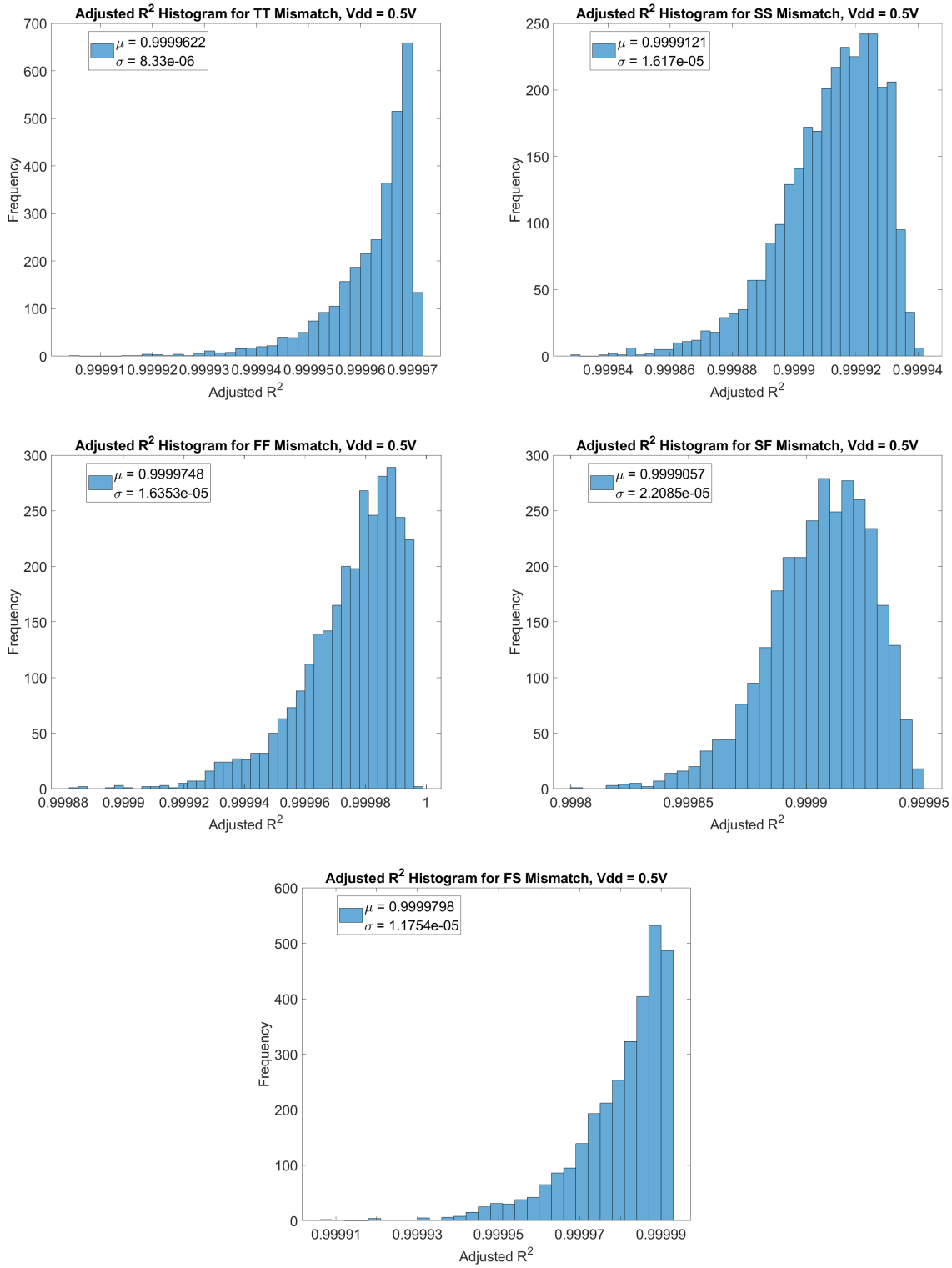

Figure 2.8: Mismatch simulations for $Vdd = 0.5V$ across all corners.

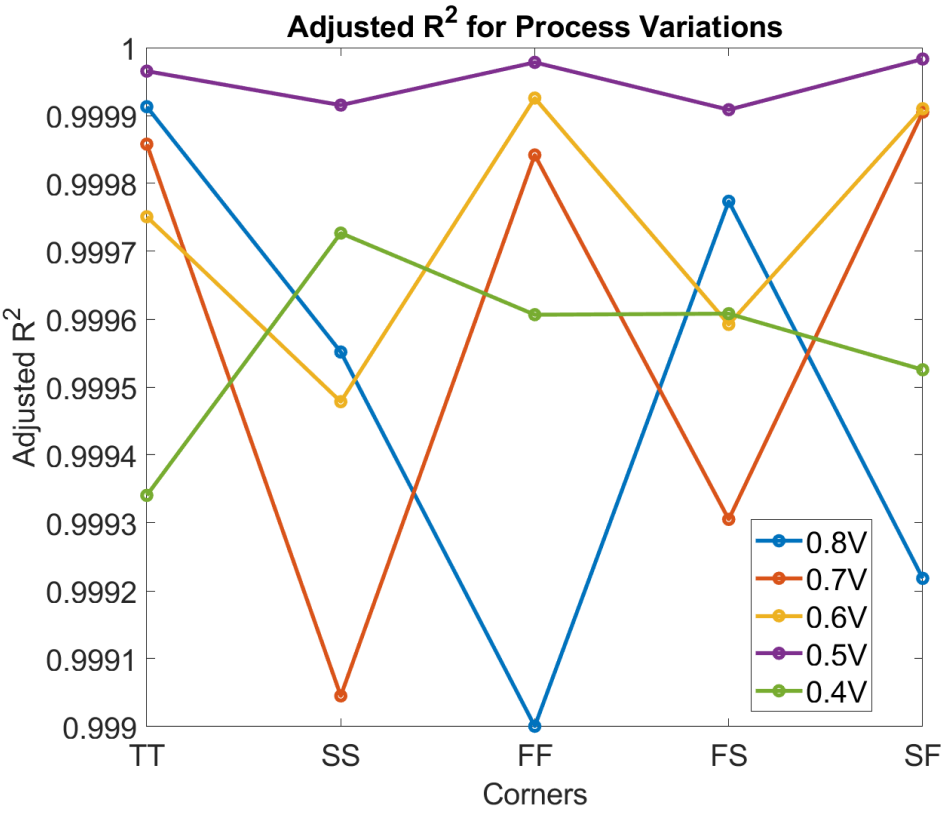

Figure 2.9: Adjusted R^2 value for different supply voltages across all corners

voltages were performed mismatch simulations for these three cases, the best case was SF corner for $0.5V$ supply voltage and this result is already shown in Figure 2.8, the worst case is FF corner with $V_{dd} = 0.8V$ and was taken FF corner for $V_{dd} = 0.4V$ as average result.

In Figure 2.10 can be appreciated that even on the worse case scenario the linearity is still good enough and also the deviation in percentage is 0.0132% which is very low meaning the low variability of the results when mismatch is taken into account.

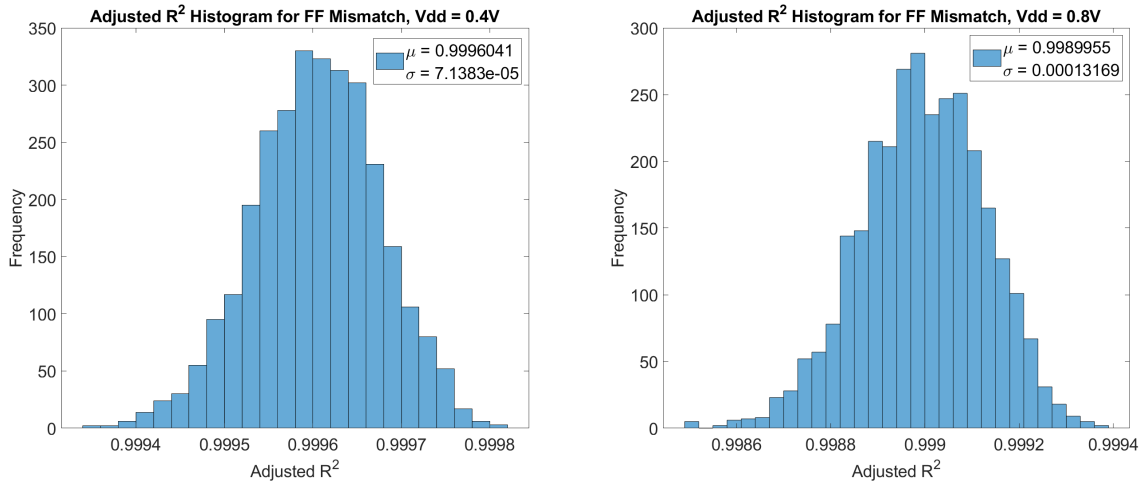

Figure 2.10: Average and worst case scenario mismatch simulation

II.III Second Current Generator Circuit

Initial idea for the second current generator is shown in Figure 2.11, from a qualitative point of view, when the temperature increases I_M also increases, while V_x decreases. The resistance $R2$ decreases slower then the resistance $R1$ and the ratio between the currents through first and second stack increases linearly with the temperature.

In Figure 2.12 is shown the circuit used for analysis purposes to explain the mathematical derivation of the transducer, first by taking the equations for subthreshold conduction of the transistors as follows:

$$
\begin{aligned}
I &= I_0 e^{\frac{-V_{th0}}{nV_t}} \\
I_{11} &= I_{0,11} e^{\frac{V_x - V_{th0,11}}{n_{11}V_t}} \left(1 - e^{\frac{V_1 - V_x}{V_t}}\right) \\
I_1 &= I_{0,12} e^{\frac{V_1 - V_{th0,12} + \lambda_D(V_1)}{n_1 V_t}} \left(1 - e^{-\frac{V_1}{V_t}}\right) \\
I_{21} &= I_{0,21} e^{\frac{V_x - V_{th0,21}}{n_{21}V_t}} \left(1 - e^{\frac{V_2 - V_x}{V_t}}\right) \\
I_2 &= I_{0,22} e^{\frac{V_2 - V_{th0,22} + \lambda_D(V_2)}{n_1 V_t}} \left(1 - e^{-\frac{V_2}{V_t}}\right)
\end{aligned}
\tag{19}
$$

And by dividing equations related to I_1 and I_2 currents an expression can be found:

$$
\frac{I_1}{I_2} = e^{\frac{(1+\lambda_D)(V_1 - V_2)}{n_1 V_t}} \frac{\left(1 - e^{\frac{-V_1}{V_t}}\right)}{\left(1 - e^{\frac{-V_2}{V_t}}\right)} \tag{20}
$$

And this result can be approximated to:

$$
\frac{I_1}{I_2}(T) \approx \frac{n_{11}W_{11}L_{21}}{n_{21}W_{21}L_{11}} \frac{n_{11}V_{th0,21}(T) - n_{21}V_{th0,11}(T)}{n_{11}n_{21}V_t(T)} \tag{21}
$$

In equation (21) is shown the final result of the analysis for this current generator, the ratio of the currents depends on the sizes of the devices, the threshold voltage difference between the two transistors M_{11} and M_{21} and of course on the temperature.

The final schematic is shown in Figure 2.13, the idea is the same as before the different points in this one is that there are not only PMOS but also NMOS transistors, also the added transistor $M0$ used to reduce the supply sensitivity and therefore exhibit low current changes with different supply voltages, in this figure are also taken into account the mirroring stage of the circuit, it is important to notice the stacked mirroring transistors are meant to make $I1'$ and $I2'$ closer to $I1$ and $I2$ respectively.

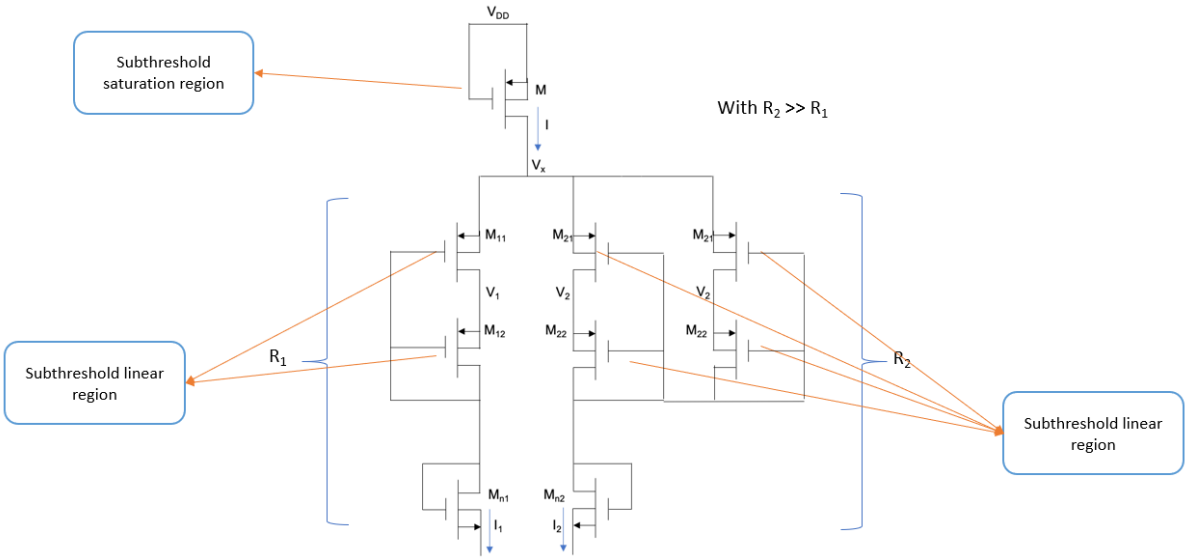

Figure 2.11: Proposed solution for second current generator

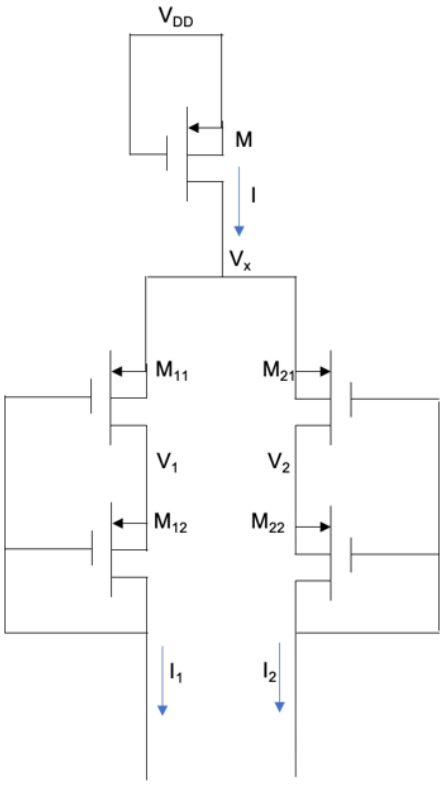

Figure 2.12: Circuit used for analysis

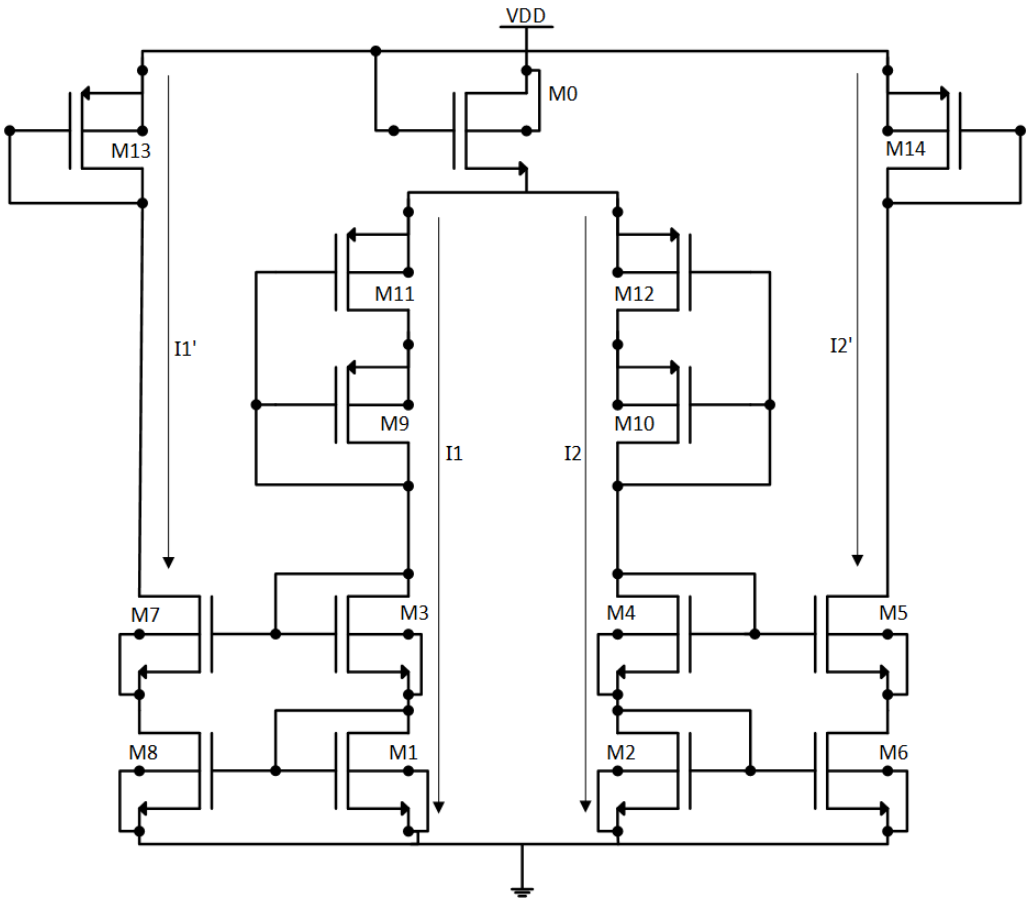

Figure 2.13: Current Generator Second Circuit including mirroring transistors

	W [μm]	L [μm]
M1-4	15	1.5
M5-8	0.22	10
M9,11	15	0.25
M10	15	0.25
M12	0.22	10
M13	15	0.5
M14	15	10
M0	15	3.5

Table 2.2: Sizing of second current generator

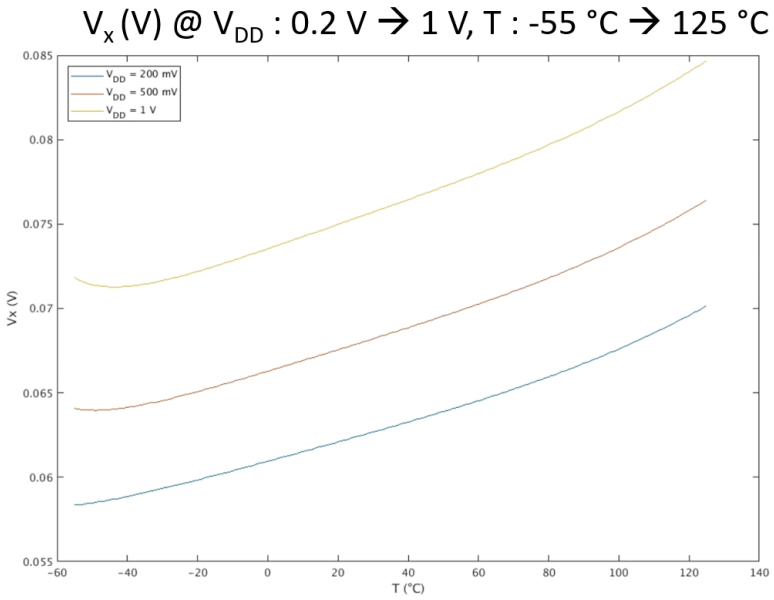

Figure 2.14: V_x node supply sensitivity

II.IV Simulation Results

The most appealing characteristic of this circuit is the low supply sensitivity it posses as depicted in Figures 2.14 and 2.15 showing that the circuit outputs have low variability when changing the supply voltage across a temperature range of $-55°C$ to $125°C$ being the higher temperature the least stable but on an acceptable margin.

Finally in Figure 2.16 can be seen the behaviour of the circuit on a wide temperature range and also for supply voltage variation exhibiting low supply sensitivity since the ratio of the currents do not change in a great measure between $0.2V$ and $1V$, another important remark is the high output range in the ratio being of about 70 which is much higher that the first proposed generator that was of about 5, this can help to achieve a high output range from the ring oscillator stage and this will translate into temperature resolution of the sensor.

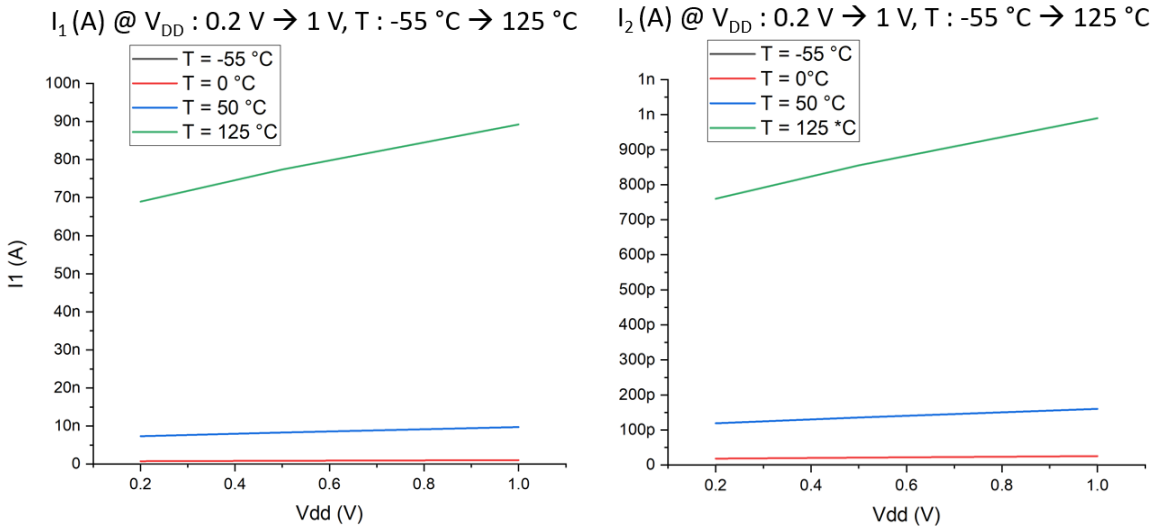

Figure 2.15: Currents I_1 and I_2 supply sensitivity

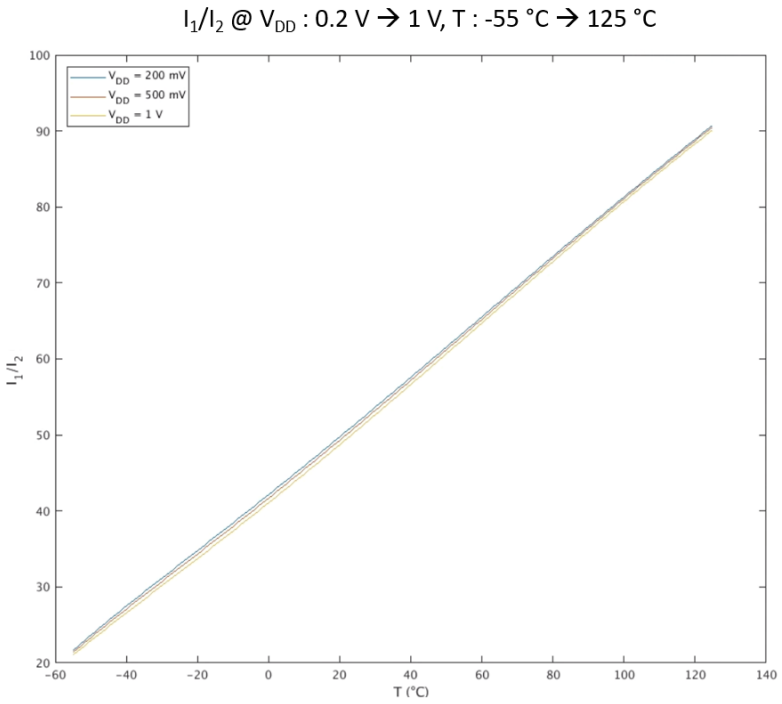

Figure 2.16: Current ratio of second current generator

III. Ring oscillators and Design testing

The ring oscillator tuning was the most difficult part of the sensor as this circuit has to oscillate with a linear proportion to the input current and moreover it has to be linear across a temperature range. The oscillators used are from the architecture described in I.III, for the higher frequency oscillator were used two stages and for the lower frequency oscillator eight stages the circuits used are shown in Figure 3.1.

III.I First Current Generator

One setup was done with the first current generator, at most the output ratio range was 20 from 0 to $100°C$ and that of course will mean a very low temperature resolution (about $5°C$) but on the other hand it has a high linearity at least on four corners, only the SF corner exhibits low linearity and also almost no ratio range as seen in Figure 3.2, this setup was particularly challenging to optimize since the current generator is very sensitive to power supply changes, not affecting linearity in great measure as shown in Section II.II, but changing the current levels accordingly to the supplied voltage, this impacted the behaviour of the oscillator making it difficult to work at low voltages as the circuit needs to be re-sized per each supply voltage to obtain better results. To sum up, the lack of frequency ratio range and the linearity issues addressed on SF corner make this approach not useful.

III.II Second Current Generator

After changing the current generator by the second approach discussed in section II.III and maintaining the sizing of the ring oscillator to see the behaviour, a better output range was

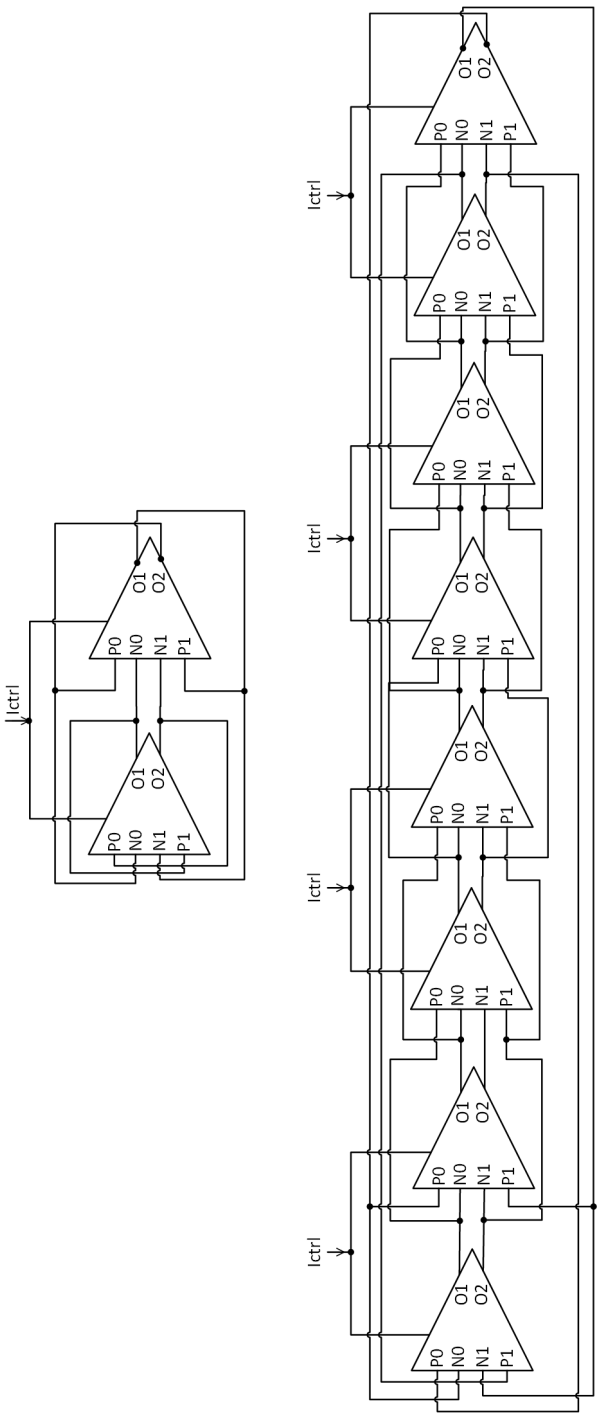

Figure 3.1: Differential ring oscillators used for current to frequency conversion

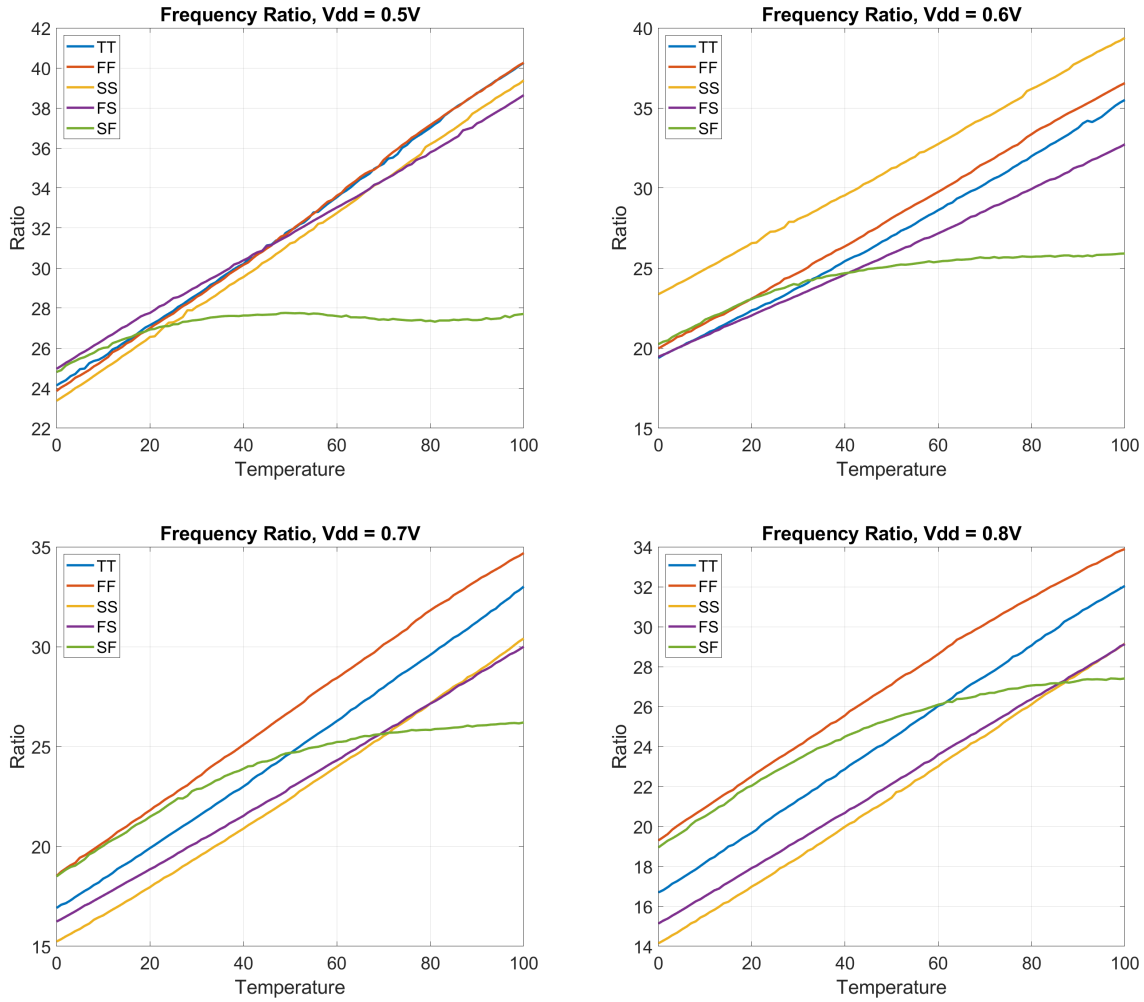

Figure 3.2: Frequency Ratio using first current generator

obtained but with low linearity, hence, the measurement error was high in most instances so it was needed to change all the sizing of the circuit and also the target supply voltage was changed since the second current generator approach has better supply sensitivity allowing the voltage to go as down as $0.2V$ to lower the power consumption, but the circuit as it was at that stage of the develop it was not capable of oscillating at such low voltage, so it had to be resized from scratch.

In Tables 3.1 and 3.2 is shown the sizing used for each delay cell, devices must had been either very large or very small to ensure a noticeable difference in the output frequencies, the

	W [μm]	L [μm]
M1,7	0.24	19.8
M2,8	5.4	19.8
M3,5	2.4	19.8
M4,6	3.6	16.5

Table 3.1: Delay cell sizing for eight stage ring oscillator

	W [μm]	L [μm]
M1,7	2.4	1
M2,8	9	1
M3,5	0.24	1
M4,6	9	1.5

Table 3.2: Delay cell sizing for two stage ring oscillator

approach to size the oscillator was to test each one individually to measure mainly the frequency range because the trade off while sizing was always between linearity and output range, as expected, while increasing the output range the linearity was more and more affected, this is the main reason of restricting the temperature range from $-20°C - 120°C$ to $0°C - 100°C$, always at the edges of the range the error was at its highest points but it was particular that for the SF corner the results were more linear, after noticing that the most linear results are from corner SF this means slow NMOS devices and faster PMOS devices the circuit was tuned by following this concept, just strengthen PMOS transistors and weaking NMOS transistors to obtain a better linearity especially for TT corner, this was done by multiplying all the oscillator's transistors by constants to increase/decrease the aspect ratio of all NMOS/PMOS transistors at the same proportion, As expected this reduced the output range and hence the resolution but this was countered by adjusting accordingly the length of the transistors to increase the frequency of the faster oscillator and produce the opposite effect on the slower one, also this sizing was done targeting $0.2V$ supply voltage to reduce power consumption, this final result is shown on Figure 3.3.

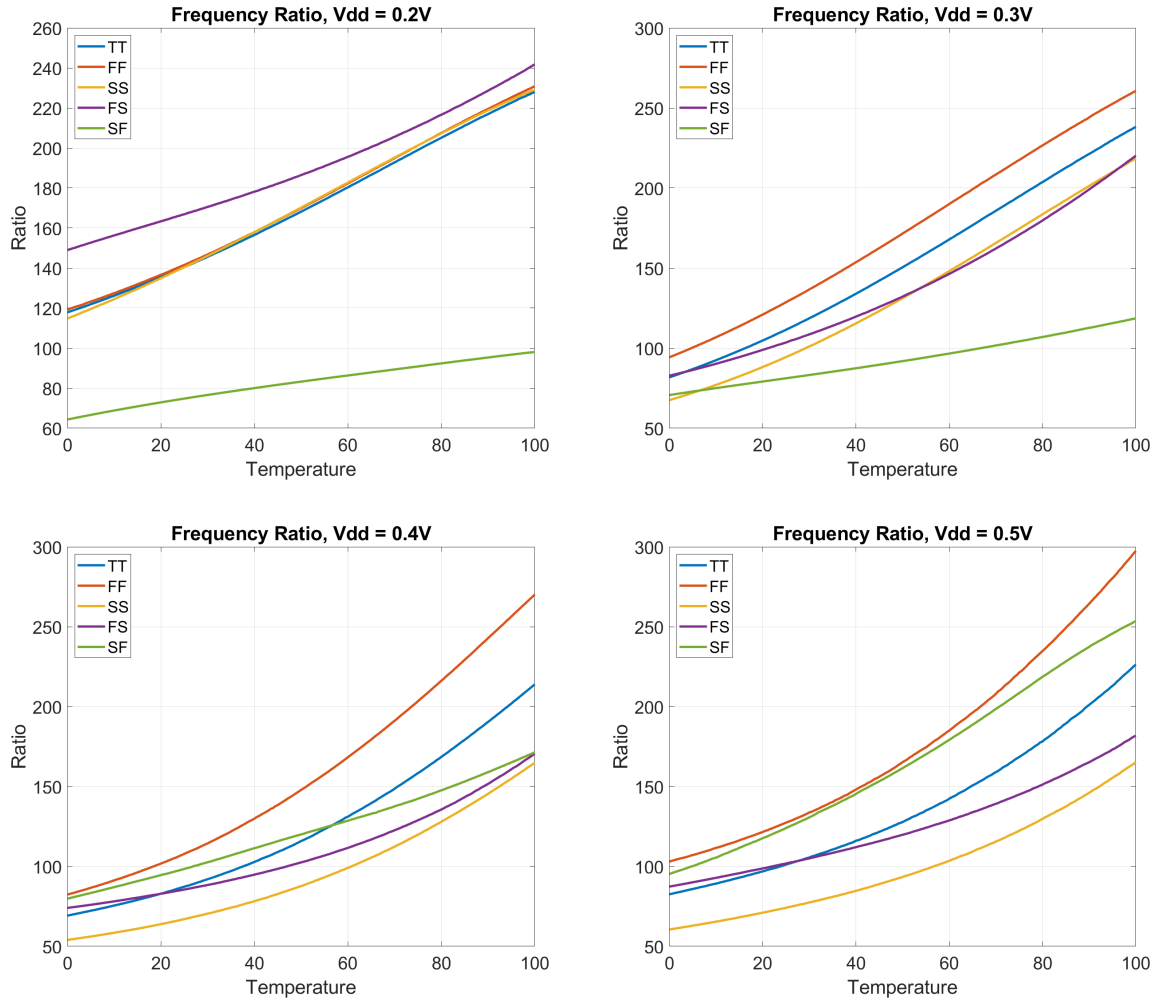

Figure 3.3: Oscillator output results

For the low frequency ring oscillator the main characteristic is the high value of the transistor length to ensure a low frequency behaviour, this combined with the higher number of stages (8) made the circuit oscillate with frequencies as low as $5.3Hz$ on the SS corner and as high as $562Hz$ for the FF corner in which the better results in terms of linearity (hence error) are obtained and for the higher frequency oscillator (2 stages) the lowest frequency was of $612Hz$ and the highest was $130KHz$ on FF corner all these values correspond to a supply voltage of $0.2V$ and of course they will increase with supply voltage.

In Figure 3.4 it is shown the difference between the actual simulation for the frequency

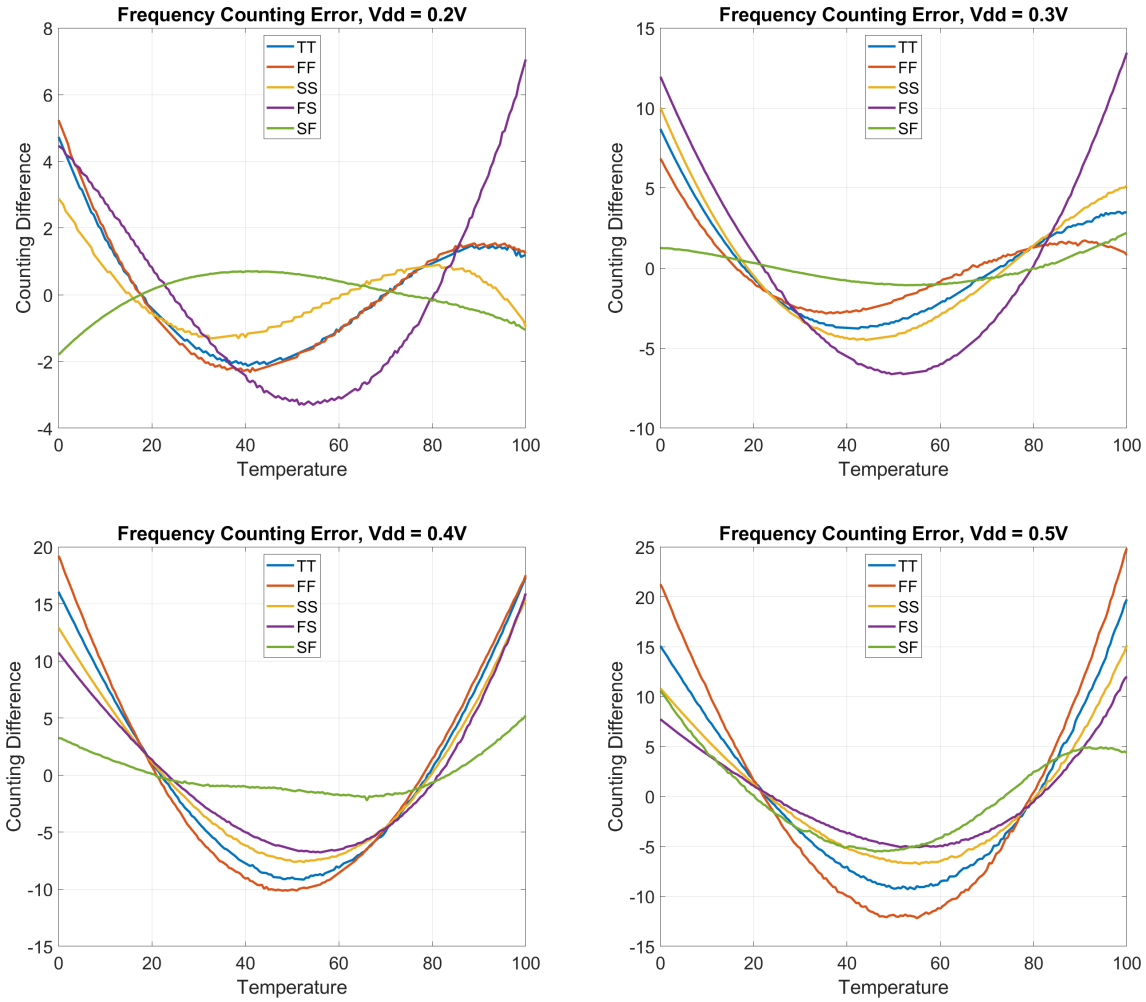

Figure 3.4: Frequency Counting difference between measurements and regression line

ratio and a calculated regression line this will give an insight of the measurement linearity, an error of 0 will mean that the simulation curve and the regression line are overlapped being this a perfect value for the counting this can help to find the calibration points to have a better match between the calibration curve and the actual regression line, from the $0.2V$ graph can be seen that at around $20°C$ and $70°C$ the counting difference is 0 so these values will be the temperatures to obtain the calibration points. The lowest values for the difference in frequency counting were found for $0.2V$ supply voltage, these are the most linear results being SF corner the most accurate across all corners but of course with less output range as discussed before,

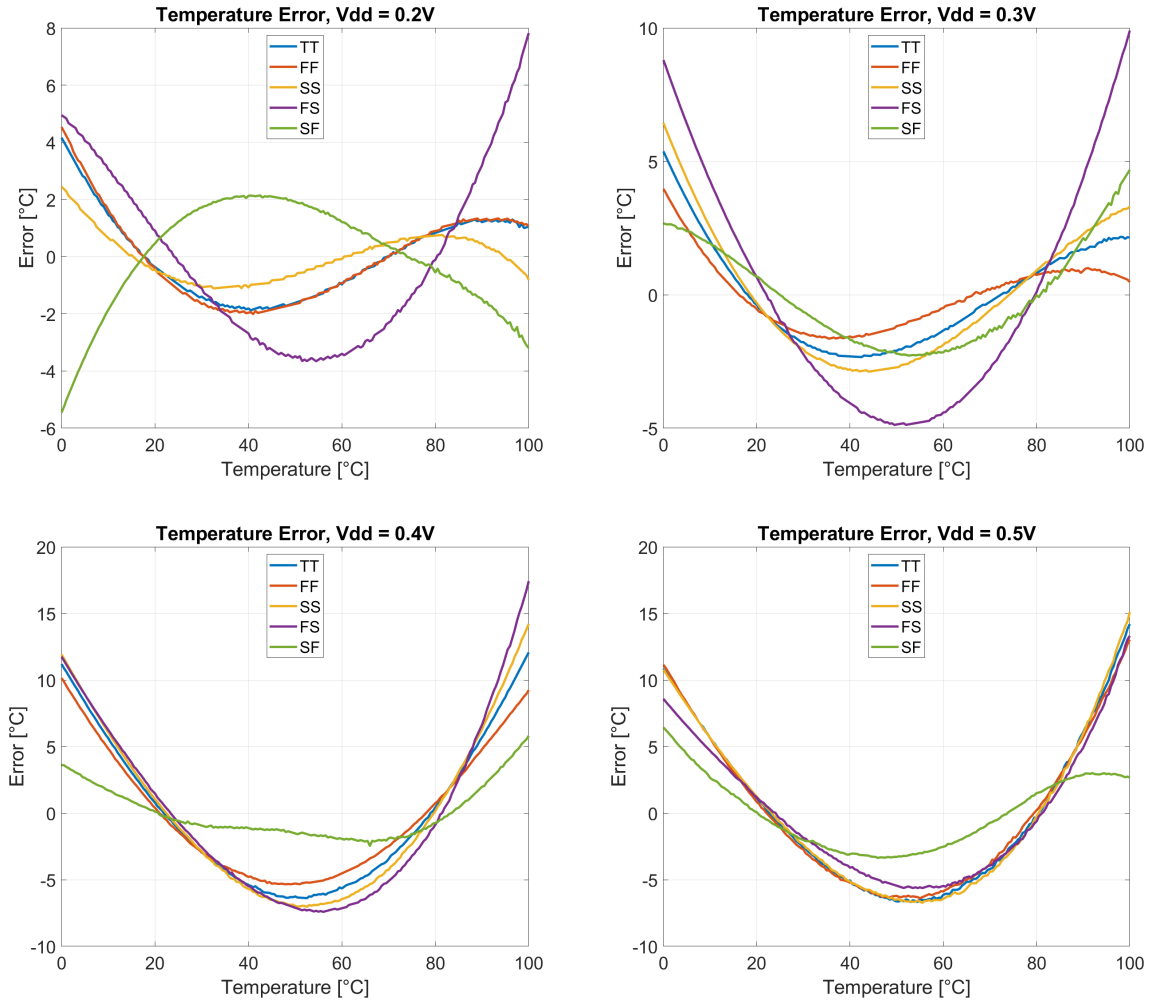

Figure 3.5: Temperature Error for Vdd variations across corners

as the supply voltage increases so do the non-linearity of the response being the maximum error in counting of 25 for $V_{dd} = 0.5V$ on FF corner. In order to find the error in temperature was necessary to interpolate the simulation values on the regression line and then subtract the corresponding temperatures. In Figure 3.5 is shown the temperature error across all corners from $0.2V$ to $0.5V$ supply voltage, results show that for $0.2V$ the error is lower as expected as the circuit was better tuned for this specific voltage giving a maximum error of $8°C$ for $100°C$ of actual temperature, as supply voltage increases so do the error, having a maximum error of $17°C$ for $0.4V$ supply and $100°C$ of actual temperature. The same error analysis for the first

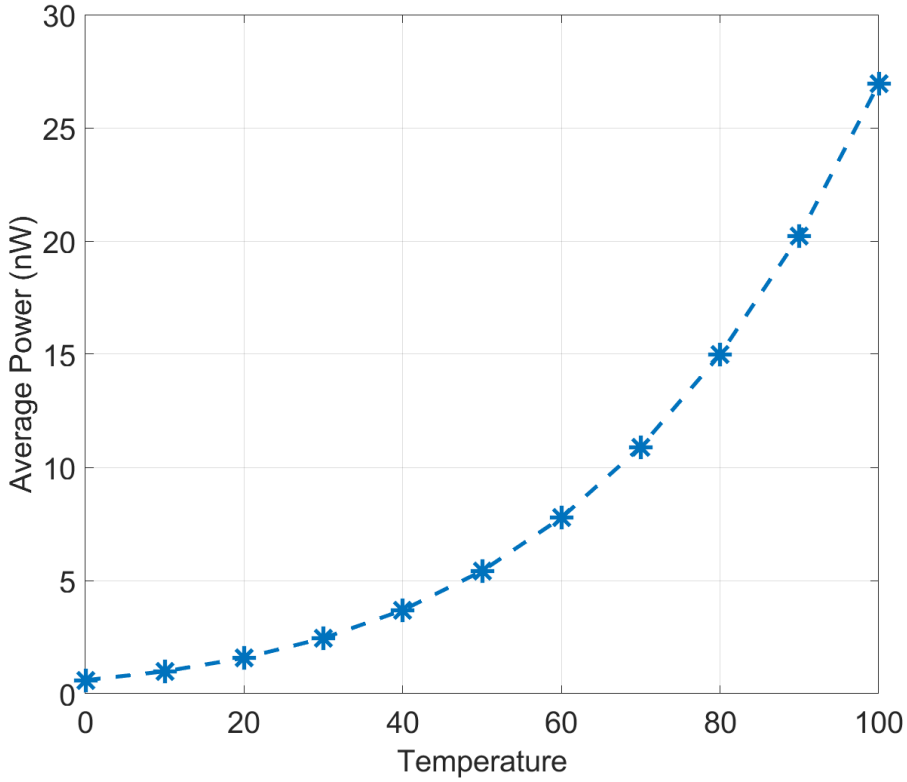

Figure 3.6: Average Power consumption over temperature range at $V_{dd} = 0.2V$

results shown on Figure 3.2 would give for sure less error theoretically but since that approach lacks totally of temperature resolution the actual error when measuring would be even higher, remembering that the resolution of that circuit is about $5°C$ it is highly probable to have this value of error. Finally after seeing the behaviour of the circuit across supply voltage variations can be said it is better to work at $0.2V$ only to ensure less error in the measurements as an increase in the supply voltage leads to a very large error incursion. In Figure 3.6 is presented the power consumption of the designed circuit, it is calculated as the average power for each temperature, being the lowest power consumption $600pW$ at $0°C$, the highest $27nW$ at $100°C$ and obtaining as nominal power consumption the value of $2nW$ at $25°C$.

IV. Conclusion

The aim of this work was to present a low power consumption with acceptable performance sensor, the highlights of the sensor is the ability to work at low supply voltage ($0.2V$) and have a power consumption of $2nW$ at $25°C$ and even at the highest temperature the power is still sub-100nW with $27nW$ at $100°C$ which is very respectable but it does not take into account the digital backend as this was not designed, therefore the total power consumption of the circuit is still not defined as it is unknown the power overhead generated by the digital backend. Due to the simple target of measuring the frequency ratio the sensor exhibits a relative low temperature resolution of $1°C$ and a high inaccuracy depending the corner which according to the application can be good enough, specially if the application enters IoT territory where the main constraint is power consumption due to the limited capabilities of current drawn from a battery so the current consumption of any sensor implemented within an IoT device should be as low as possible. As future work there is still many aspects that can be improved in the design such as the inclusion of better supply sensitivity in the first designed current generator explained in Section II.I, an increase in the number of stages in the high frequency ring oscillator to reduce its frequency output for lower power consumption and better signal output swing since with an increase of stages there can be a better recover of the signal made by the delay cells, depending on the results also can be implemented a linearity correction algorithm as shown in [2], have another approach in the digitizing process to improve resolution and give the faster oscillator opportunity to reduce the output frequency, reduce the frequency ratio and with fine tuning of the oscillators achieve better linearity for improved measure error, another possibility to reduce the power consumption even further is to turn off the oscillators when the sensor is idle. Finally after improving the

	[1]	[2]	[3]	[4]
Type	CMOS	CMOS	CMOS	CMOS
Technology	180nm	65nm	180nm	180nm
Supply Voltage (V)	1.2	0.85-1.05	0.6-1.2	0.8
Area (mm^2)	0.09	0.0082	0.007	0.074
T range (C)	0-100	0-100	0-100	-20 - 80
Inaccuracy (C)	-1.4/1.5	+-0.9 @1V	-1.64/0.67	-0.9/1.2
Calibration	2-point	2-point	2-point	2-point
Resolution (C)	0.3	0.3	0.55	94m
Power (W)	71n @ $25C$	154μ @ 1V	3.92nW @ $25C$	11n @ $25C$

Table 4.1: Comparison between reviewed temperature sensors

	[5]	[7]	[8]	**This work**
Type	CMOS	Resistive	CMOS	CMOS
Technology	180nm	65nm	65nm	180nm
Voltage (V)	1.2	1	0.5	0.2
Area (mm^2)	0.008865	0.11	0.63	-
T range (C)	-20 - 100 (External Oscillator) -20 - 80 (RC Oscillator)	0-100	0-100	0-100
Inaccuracy (C)	-0.22/0.19 (XO) -0.76/0.76 (RC)	-1.1/1.5	-1.53/1.61	-6/8
Calibration	2-point	1-point	2/3 point	2-point
Resolution (C)	90m	0.61	0.3	1
Power (W)	75n (XO) 570n(RC)	488.3n	763p	2n @ $25C$

Table 4.2: Comparison between reviewed temperature sensors (cont'd)

performance of the sensor in the best way rest to do layout design to do a comparison in terms of area with other works reviewed in the literature.

References

[1] S. Jeong, Z. Foo, Y. Lee, J. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nw cmos temperature sensor for low power wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[2] T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A vco based highly digital temperature sensor with 0.034 °c/mv supply sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2651–2663, 2016.

[3] C. Ku and T. Liu, "A voltage-scalable low-power all-digital temperature sensor for on-chip thermal monitoring," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1658–1662, 2019.

[4] T. Someya, A. K. M. M. Islam, T. Sakurai, and M. Takamiya, "An 11-nw cmos temperature-to-digital converter utilizing sub-threshold current at sub-thermal drain voltage," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 613–622, 2019.

[5] K. Yang, Q. Dong, W. Jung, Y. Zhang, M. Choi, D. Blaauw, and D. Sylvester, "9.2 a 0.6nj −0.22/+0.19°c inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 160–161, 2017.

[6] M. Jalalifar and G.-S. Byun, "A wide range cmos temperature sensor with process variation compensation for on-chip monitoring," in *IEEE Sensors Journal*, 2016.

[7] H. Xin *et al.*, "A 174 pw–488.3 nw 1 s/s–100 ks/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability," *IEEE Solid-State Circuits Letters*, 2018.

[8] H. Wang and P. P. Mercier, "A 763 pw 230 pj/conversion fully integrated cmos temperature-to-digital converter with +0.81 °c/−0.75 °c inaccuracy," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 2281–2290, 2019.

[9] S. Park, C. Min, and S. Cho, "A 95nw ring oscillator-based temperature sensor for rfid tags in 0.13µm cmos," in *2009 IEEE International Symposium on Circuits and Systems*, pp. 1153–1156, 2009.

[10] Y. A. Eken and J. P. Uyemura, "A 5.9-ghz voltage-controlled ring oscillator in 0.18-/spl mu/m cmos," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 230–233, 2004.