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Towards a non invasive glucose sensor using near infrared spectroscopy: preliminary results

.

Martín José Calero Mantilla

Ingeniería Electrónica

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RESUMEN

Este artículo presenta los resultados preliminares de un sensor de glucosa no invasivo que utiliza espectroscopia de infrarrojo cercano con el objetivo de medir la glucosa analizando la absorción de luz de la glucosa en dos longitudes de onda específicas. Se diseñó un circuito de adquisición de datos, que incluye el estado de control del LED, el amplificador de transimpedancia y los circuitos de filtrado, así como un algoritmo de estimación mediante regresión de mínimos cuadrados parciales (PLS). Los datos se adquirieron a través de tres etapas diferentes, cada una con condiciones distintas. El sistema se calibró con 60 datos de cada longitud de onda y se probó con 12 datos de cada longitud de onda. Los resultados se evaluaron con el error cuadrático medio (RMSE) y el análisis del error de rejilla de Clarke.

Palabras clave: Diabetes, sensor de glucosa, no invasivo, prototipo, estimación.

ABSTRACT

This paper presents the preliminary results of a non invasive glucose sensor using near infrared spectroscopy with the aim of glucose measurement analyzing the glucose light absorption at two specific wavelengths. A data acquisition circuit, which include LED control state, transimpedance amplifier and filtering circuits were design, as well as an estimation algorithm using Partial Least Square (PLS) regression. The data was acquired through three different stages, each one with different conditions. The system was calibrated with 60 data from each wavelength and tested with 12 data from each wavelength. The results were evaluated with the Root Mean Square Error (RMSE) and the Clarke's grid error analysis.

Key words—Diabetes, glucose sensor, non invasive, prototype, estimation.

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INTRODUCTION

In the last years, the amount of people diagnosed with diabetes has increased in unbelievable numbers. According to the World Health Organization, from 1980 to 2014 the quantity of people with diabetes increased from 108 millions to 422 millions [1]. This disease is not only a world wide public health challenge, but also a national challenge. In fact, according to the Pan-American Health Organization, in Ecuador there is a prevalence of 1.7% of diabetes in adults from 10 to 59 years old [2].

Diabetes is a disease which does not recognize between age, gender, race, and it is caused by an immunologic effect where the body identifies the insulin produced by the pancreas as an external agent and attacks it. There are three types of diabetes: Type 1 Diabetes Mellitus (T1D), Type 2 Diabetes Mellitus (T2D), and Gestational Diabetes Mellitus (GD) [3]. One similarity between all of these types of diabetes are the cost of the disease. The minimal cost for treating this illness in Ecuador, which includes clinical examinations, medical consultations, supplies and medications is $224,36 per month or $2692,32 per year [4]. In this analysis, the supplies and medications that are considered are the cheapest ones, but nowadays the best way to control and avoid future complications is the use of new technologies that are even much more expensive.

After insulin, the most important supply for diabetes treatment is the instrument for measuring the blood sugar or glucose called glucometer. The most widely used glucometer is the Accu-Chek Performa Nano, where a test strip and a drop of blood is used to determine the amount of glucose after few seconds [5]. Other instruments for glucose measurement are the Continuous Glucose Monitoring (CGM) which are sensors that capture information about the behaviour of glucose through interstitial tissue. One of the most popular CGM is the Free Style Libre, a glucose sensor from Abbot which main difference with glucometers is that

these instruments give information in terms of glucose tendency [6]. All these instruments are invasive or minimal invasive, however they causes pain to patients.

The focus of this study is centered around a non invasive way for measuring glucose level, and compare our method with the other instruments for glucose measurement such as the Accu-Chek Performa Nano and the Free Style Libre. Moreover, the aim of this research is to analyze the glucose light absorption at specifics wavelengths using the Lambert-Beer law, make a partial least square regression to calibrate a glucose measurement estimation model.

This work is organized in the following manner: in the section of development is the methodology to obtain the photoplesthysmogram (PPG) signal, process it and calibrate the model. In this section, the experimentation and results are presented for a variety of scenarios with respect to glucose measurement under different amount of carbohydrates ingested. The overall findings and future steps are presented in the conclusion section.

DEVELOPMENT

METHODOLOGY

In this section, the Lambert-Beer law is explained through their equations. Then, the two wavelengths are defined for obtaining the peak light absorption of glucose. Moreover, each part of the circuit to obtain the PPG signal together with the design equations are explained. The signal processing, which includes a peak and valley detection algorithm and absorbance calculation are also presented. Finally, the calibration model and glucose estimation is detailed.

Lambert-Beer Law

Before explaining the Lambert-Beer law, it is important to understand the behaviour of light when it has interaction with glucose and human tissue. As it can be seen in Fig. 1, there are two main elements: the NIR diode and a photodiode. The intensity of reflected light is the aspect to be analyzed. In Fig. 1 a), there is a little light absorbance, which means a less glucose concentration due to the light intensity received by the photodiode is low. In the other hand, in Fig. 1 b), when there is more glucose in blood, the light intensity is higher because there is more reflected light so that the absorbance is also higher [7][8][9][10].

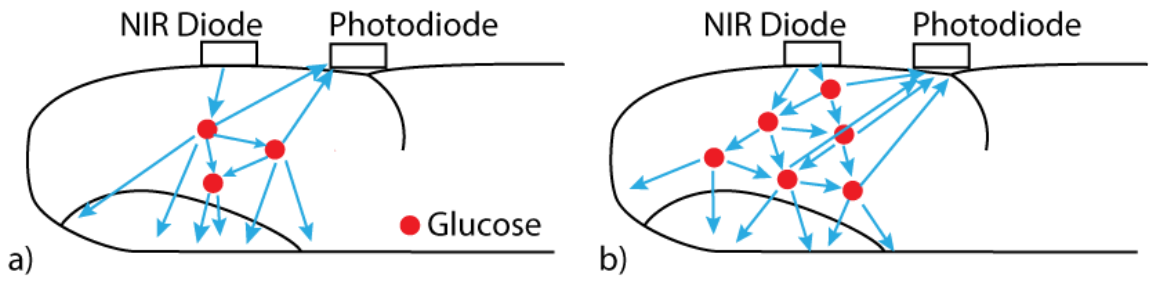

Figure 1 Behavior of light across human tissue. Principle of reflection [8].

The Lambert-Beer law is the method used to estimate the glucose value through the information gather by the light absorbance of tissue. This law states that the absorbance of light through any type of solution is proportional to the concentration of the solution and the length path travelled by the ray [7][8][9][11]. Equation (1) describes the Lambert-Beer law where I is the light intensity at an specific wavelength, I_o the incident light intensity, ε is the molar extinction coefficient, C is the molar concentration and L is the path length [7][8][9]. Equation (1) is modified with the aim to obtain the absorbance of light. The new equation can be seen at equation (2) where A is the absorbance, I_o is the intensity of incident light and I is the intensity of light at a specific wavelength [8][9][12].

$$I = I_o e^{-\epsilon CL} \quad (1)$$

$$A = \log_{10}\left(\frac{I}{I_o}\right) \quad (2)$$

At this point, the basic concept of the Lambert-Beer law is used for glucose estimation, now we will move on to the determination of peak light glucose absorption wavelength.

Wavelength of peak light glucose absorption

First of all, it was decided to use LEDs because they are cheaper and easier to obtain than laser lights. It is important to highlight that at different wavelengths, elements have different peak absorption of light [7][11][8][9][12][13][14][15][16][17], for this reason it was decided to choose a wavelength where glucose has a peak light absorption and other where glucose has a lower peak light absorption. According to [17], to have two absorbance at different wavelengths can lead to obtain a better estimation model based on multivariate analysis. For this reason, the wavelength of 940nm that produces a considerable peak light absorption was chosen. Moreover, a wavelength of 860nm was also selected due to it

produces a lower peak light absorption for glucose. The elements purchased were the VSLY5850 of Vishay as the 940nm LED and the VSMB3940X01 of Vishay as the 860nm LED.

Other important element to be selected is the photodiode which must match with the same wavelength of the peak light absorption of glucose in order to have the best performance. According to suggestions of [7][11][8][9][12][13][14][15][16][17] the QSB34GR of Fairchild Semiconductor was selected because it has a peak light absorption at 940nm which is the peak light absorption of glucose and it also has a natural light filter for noise suppression. With the two important elements for the light absorption peak of glucose, the design of each part of the circuit to obtain the PPG signal can be explained.

Obtainning the PPG signal

To get the PPG signal, first it is necessary to understand how this signal works. The sensor for obtaining a PPG signal works similar to a pulse oximeter, where the light absorption depend on the heart beat due to the expansion and contraction of blood vessels in the finger after each heart-beat [8][14]. A PPG signal is composed by two parts: a pulsatile component that comes from the change of blood volume of heart-beat and non pulsatile component that has low frequency components that comes from different factors such as respiration, vasomotor activity and thermoregulation [8][9][14][16].

Based on this change in blood volume, the PPG signals sensor detects variations in the intensity of transmitted or reflected light of the tissue. When light penetrates into the human tissue, its intensity fluctuates through the cardiac cycle. Therefore, the photodiode generates a current that is directly proportional to variation of light intensity [8][9][14][15][16]. Fig. 2 shows the behaviour of the PPG signal.

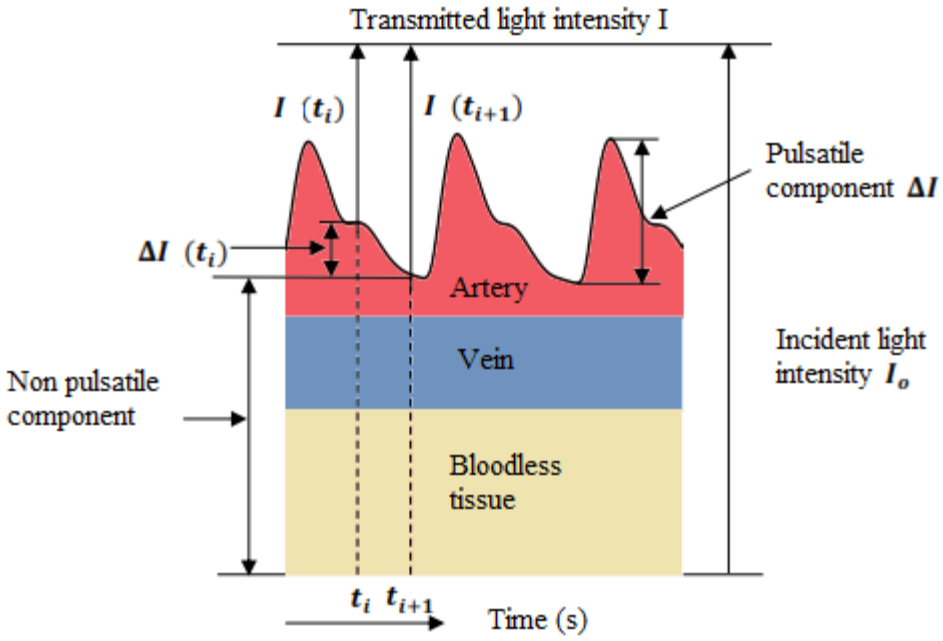

Figure 2 PPG signal per parts [8][17].

After understanding the operation of PPG signals and their parts, it is possible to move on to each part of the acquisition circuit.

Transmitter and receptor configuration

To have a better glucose estimation, the light that is transmitted should be able to reach into the deepest human body layer. To achieve the subcutaneous tissue and use the method of reflection, it is necessary to establish a distance between the emitter and the receiver because of the path length is equal to half of the distance between the two devices [7][8][9]. So that a distance of 4mm was selected with the aim that the penetration be 2mm in the finger tissue.

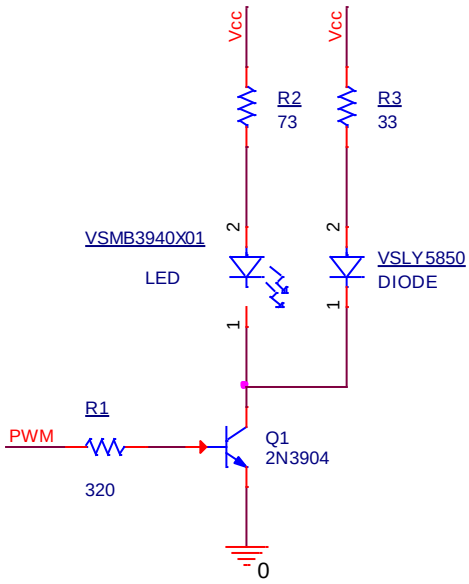

Figure 3 Control circuit of ON/OFF state of LEDs.

The design of the circuit was based on [7][11][8][9][10][12][13][14][15][16][18] and [19]. Fig. 3 presents the ON/OFF LEDs control circuit. As can be seen, a Bipolar junction transistor (BJT) controls the state of the LED using a Pulse width modulation (PWM) signal with a frrquency of 1Hz generated by an Arduino UNO. Equation (3) presents the design of BJT input resistance.

$$R_1 = \frac{Vcc - V_{BE}}{I} = \frac{5V - 0.65V}{10mA} = 380\ \Omega \qquad (3)$$

For the design of the resistance that connects Vcc with the anode of the LED, it is important to take into account the necessary voltage that needs the LED to emit the light at the correct wavelength. For the 940nm wavelength, it is necessary a voltage of 1.55V, and for the 860nm a voltage of 1.35V is needed. Moreover, according to the data sheet [20][21], the forward current is 50mA for the 940nm LED and for the 860nm the current is 100mA, so that the resistance value for each led is (4).

$$R_2 = \frac{Vcc - V_{LED940nm}}{I_{act}} = \frac{5V - 1.35V}{50mA} = 73\ \Omega$$
$$R_3 = \frac{Vcc - V_{LED860nm}}{I_{act}} = \frac{5V - 1.65V}{100mA} = 33\ \Omega \qquad (4)$$

The 2n3904 was the BTJ selected together with a resistance of 330 Ω for the base. Moreover, for the 940nm LED, one resistance of 10 Ω in series with other two of 33Ω was used for the 840nm LED only one resistance of 33 Ω. As the emitter and receiver needs to be at a distance of 4mm, a superficial contact PCB was made to get the best results.

Transimpedance amplifier

The photodiode produces a current which is proportional to the light intensity change, so that, to measure that change it is necessary to transform current into voltage, this operation does the transimpedance amplifier. Fig. 4 shows the circuit of transimpedance amplifier, the configuration of the transimpedance amplifier used is the zero-bias mode, where the anode of the photodiode is connected to ground and the cathode to the negative entrance of the amplifier . With this configuration the OPAMP keeps the voltage across the diode zero and the resistance creates a voltage at the output of the amplifier [8][9]. The capacitor is used for stability and filtering as a low pass filter [9][20].

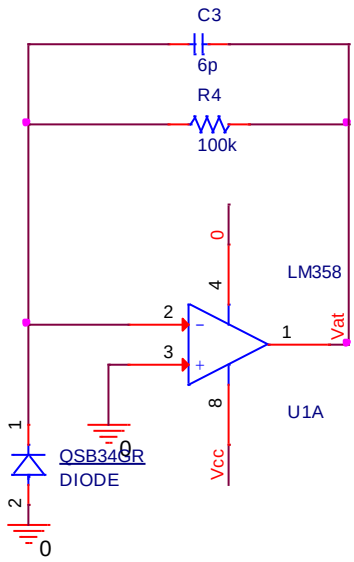

Figure 4 Transimpedance amplifier circuit.

To design the resistance and capacitor of the transimpedance amplifier, the equation of [9] was used. An important fact to take into account is the amplifier bandwidth gain. The capacitor can make unstable the output of the amplifier due to the fact that if the intersection of cut off frequencies of zero and polo is outside the bandwidth gain, the output will oscillate [9][20]. With this in mind, a LM358 device which has a bandwidth of 1 MHz was used, knowing that the capacitance of the photodiode is 25pF and as was recommended in [9], the chosen resistance is 100k Ω. Equation (5) was used to completely design the transimpedance amplifier.

$$C_3 = \frac{1}{4\pi R_4 GBW}\left[1 + \sqrt{1 + 8\pi R_4 C_{pd} GBW}\right] = 7.15\ pF \qquad (5)$$

A commercial ceramic capacitor of 6 pF was used. After the transimpedance amplifier, it is necessary to filter the signal to eliminate noise and only keep the frequency band where PPG signals are.

Filters

A filter stage is needed in order to eliminate information of unwanted frequencies and to remove noise. PPG signals work in frequencies between 1Hz and 10Hz, for this reason, it is necessary to use a band pass filter to keep this frequency band. At the output of the transimpedance amplifier, an active band pass filter that is made up by a high pass filter, followed by a voltage follower configuration together with a low pass filter are fitted. The low pass filter and the high pass filter are referenced to a voltage of 2.5V instead of ground because this way the PPG signal will not have negative values.

The design of both low pass and high pass filters was based on equation (6). It was decided that the value of the capacitor for the high pass filter is 10 μF and for the low pass filter a capacitor of 100 nF. The cut off frequency for the high pass filter was of 10Hz and for the low pass filter was of 0.86Hz. Equation (7) presents the resistance values for both filters.

A voltage divider configuration was used to obtain half of the input voltage, this new voltage works as a new voltage reference. Then a voltage follower is also implemented so that the voltage divider does not affect the behavior of the band pass filter. [8][9]. The LM358 device is also used for the voltage follower configuration. The entire circuit with the respective values of elements can be seen at Fig. 5. After the filtering of the signal it is necessary to digitize it.

$$f_c = \frac{1}{2\pi RC} \tag{6}$$

$$R_5 = \frac{1}{2\pi 10\mu F 0.86Hz} = 18.5k\ \Omega$$
$$R_6 = \frac{1}{2\pi 100nF 10Hz} = 159k\ \Omega \tag{7}$$

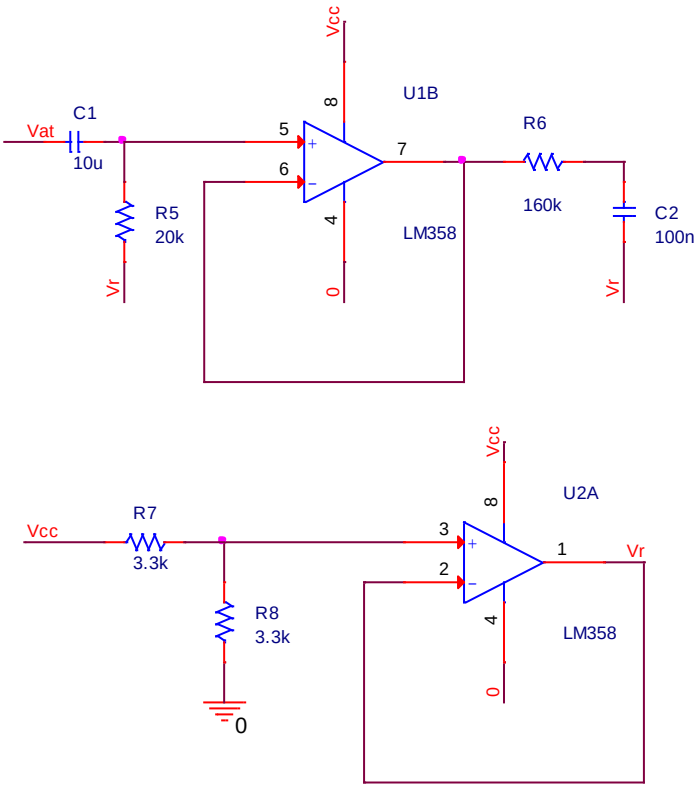

Figure 5 Filters and voltage divider circuits.

Microprocessor and external analog to digital converter

Two different Arduino boards were used in this project. One of them manage the ON/OFF control of the LEDs and the other obtains the digitization of the analog PPG signal. To have a better signal resolution, an external analog to digital converter ADS1115[21], which has a 16 bit resolution, is used in stead of Arduino analog channel that only has 10 bit resolution. In order to communicate the external analog to digital converter with Arduino MEGA board, the connection SDA and SCL was used.

Signal processing

MATLAB is used to process the signal. First of all, the ADS1115 takes samples with a frequency of 475 Hz, and with a MATLAB code, the digital value is printed with a frequency of 100 Hz and save it in a matrix. Then, the signal is analyzed with a peaks and valleys detection algorithm. Finally, the light absorbance is calculated based on the Lambert-Beer law.

Peak and valley detection algorithm

The peak and valley detection algorithm is straight forward. First, the peaks of the signal are found as maximum values. In order to get the valleys, the signal is inverted and the peaks are also found so that, this new peaks are actually the valleys of the original signal. After that, a code to determine if the peaks and valleys found are correct was made. In this code, the maximum peak and valley values are found and a difference between those values are calculated, then it is multiplied by a threshold. If this new value is higher than threshold, the peak and valley position is saved. This process is performed for all peak and valley values.

Light absorbance

The light absorbance is obtained based on Equation (2) where I_o is the difference between the peak and valley and I is the value of the valley. Then an average of the detected peaks and valleys is calculated in order to calibrate the model and to obtain an error between each calculated absorbance with the average.

Model calibration and glucose estimation

With the absorbance data collected, it is necessary to make a model that estimate the glucose value. As suggested in [17], the model of partial least squares (PLS) regression was selected due to the fact that the method finds a linear regression with a projection of the predicted variables and the observed variables in a new space [17]. In addition, the PLS regression model lets does a multivariate model where the information of absorbance at two different wavelengths are the inputs allowing that the estimation model will be more accurate. The MATLAB plsregress function gives betaPLS coefficients which are basically the scores of the linear regression model. These values are desired because they can be used to estimate the value of glucose only with the information of absorbance.

In order to calibrate the model, the 80% to 85% of data collected is used to obtain the scores of the linear regression model. The rest 15% to 20% of data is used to test how well the model works for estimate the glucose value.

Finally to be sure that the glucose estimation is clinically correct, 2 measurements are going to be used. One is the root mean square error (RMSE) which gives the information about for how much the estimation model is not accurate from the real glucose value. Equation (8), where $\widetilde{A}_i$ is the value estimation, A_i is the real value and n is the number of samples, describes how to calculate the RMSE.

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n}(\widetilde{A_i} - A_i)^2}{n}} \quad (8)$$

The second one is the Clarke's grid error analysis which have 5 different zones and relates the glucose estimation value and the real glucose value. This grid establishes that if the estimation value is in the zone A or B, it is clinically acceptable and it could pass all the clinical tries [7][11][8][9][10][12][13][14][15][16][17][18][19]. To obtain the results of the Clarke's grid error analysis the code found in [22] was used.

EXPERIMENTATION AND RESULTS

This section talks about how the data for calibrating and estimating glucose was acquired, besides reports on the obtained results and errors between the estimated glucose value of the non invasive sensor and the blood glucose obtained by the glucometer Accu-Chek Performanano and the sensor FreeStyle Libre of Abbot.

Test bench design

Data were collected from only one person. There were 3 stages of data collection:

- 1st stage: For two straight hours, the data was collected every 5 minutes with the Free Style Sensor, the Accu-Chek Performanano and the non invasive sensor. For this stage the person was fasting and after the first 15 minutes or 4 data collected, the subject ingested 25g of carbohydrates and does not have an insulin injection to obtain the change of glucose through time.
- 2nd stage: For two straight hours, the data was collected every 5 minutes with the Free Style Sensor, the Accu-Chek Performanano and the non invasive sensor. For this stage the person was fasting and after the first 15 minutes, or 4 data collected, the

subject ingested 25g of carbohydrates and had a dose of insulin injected to obtain the change of glucose through time and under insulin effect.

- 3rd stage: Information was collected randomly through two days until 24 absorbance values were acquired.

At the end of data collection, 72 data for each wavelength had been acquired, where 60 data of each wavelength where used to calibrate the PLS regression model and the other 12 to test how good the estimation model is. The results obtained can be seen in the next section.

PPG signal and peak and valley detection algorithm

Fig. 6 presents the PPG signal obtained with the peaks and valleys detected by the algorithm. In table I the average absorbance of different samples can be seen, as well as the error between the peaks and valleys of that sample with the average of those peaks and valleys to confirm that the data collected is correct.

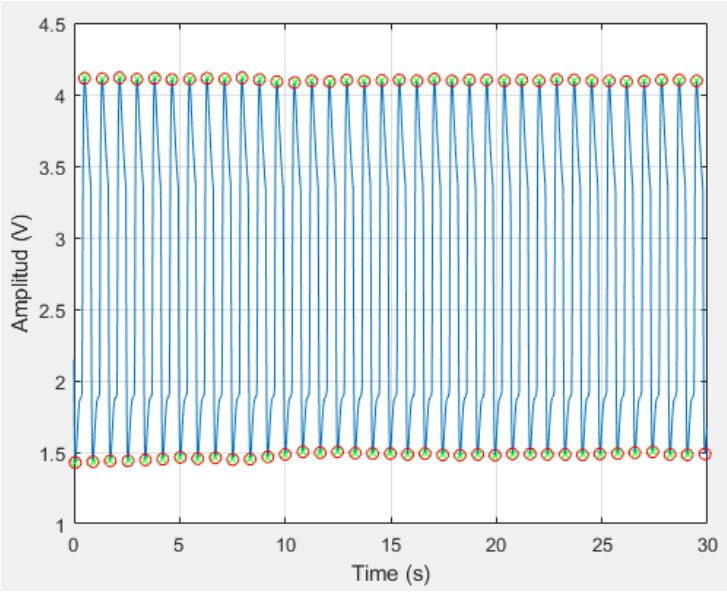

Figure 6 PPG Signal obtained at 940nm wavelength.

Table 1 Absorbance of different data and error between peaks and valleys of the sample.

Sample	Reference (mg/dl) Blood —— CGM	Average Absorbance 860nm —— 940nm	Error (%) 860nm —— 940nm
1	69 —— 64	0.1438 —— 0.4113	2.7321 —— 1.0954
2	154 —— 157	0.2742 —— 0.4952	3.9578 —— 2.7510
3	107 —— 78	0.2111 —— 0.4190	3.1030 —— 2.3066
4	259 —— 264	0.4033 —— 0.6781	3.7185 —— 4.0161

Non invasive sensor glucose estimation and RMSE

After calibrating the model with the 60 data from each wavelength, the rest 12 data was used to test how well the model can estimate the glucose value. Table II shows the value of the 12 glucose measurement made with the blood test on the Accu-Chek Performa Nano, with the FreeStyle Libre and with the non invasive glucose sensor. In this table the RMSE between the blood glucose, the non invasive sensor and the FreeStyle Libre sensor are also presented. Looking at these results, it is clearly seen that data from the non invasive sensor has a RMSE lower than the FreeStyle Libre sensor data. In fact, the method of this project is approximately 11 mg/dl more accurate than the FreeStyle Libre sensor.

Table 2 Glucose measurement in blood, the FreeStyle Libre sensor, the non invasive sensor and the RMSE.

Blood glucose (mg/dl)	FreeStyle glucose (mg/dl)	Non invasive sensor glucose (mg/dl)
61	60	72.03
135	128	148.54
184	204	189.89
219	259	214.48
154	157	165.94
104	101	145.35
143	130	152.05
107	78	126.07
146	75	155.06
123	103	133.77
174	173	180.41
259	264	253.33

RMSE between blood glucose and FreeStyle glucose (mg/dl)	RMSE between blood glucose and Non invasive sensor glucose (mg/dl)
26.6849	15.9802

Finally, Fig. 7 shows the Clarke's error grid where the estimated results of the non invasive glucose sensor and the FreeStyle Libre sensor together with the real blood results are plotted. The Clarke's grid diagram shows that for the non invasive sensor 11 (91.67 %)of the 12 testing data is in zone A and 1 (8.33 %) of data is in zone B. In comparison, for the FreeStyle Libre sensor the Clarke's grid graph shows that 10 (88.33 %) of the 12 testing data is in zone A and 2 (16.67 %) of data is in zone B. With these results, it is evident that thenon invasive sensor presents more accurate measurements than the FreeStyle Sensor. It should be noted that any information of the non invasive sensor is in zone C, D or E which indicates that even though the data is not big enough to have a good deep analysis, it has promising results and clinically acceptable.

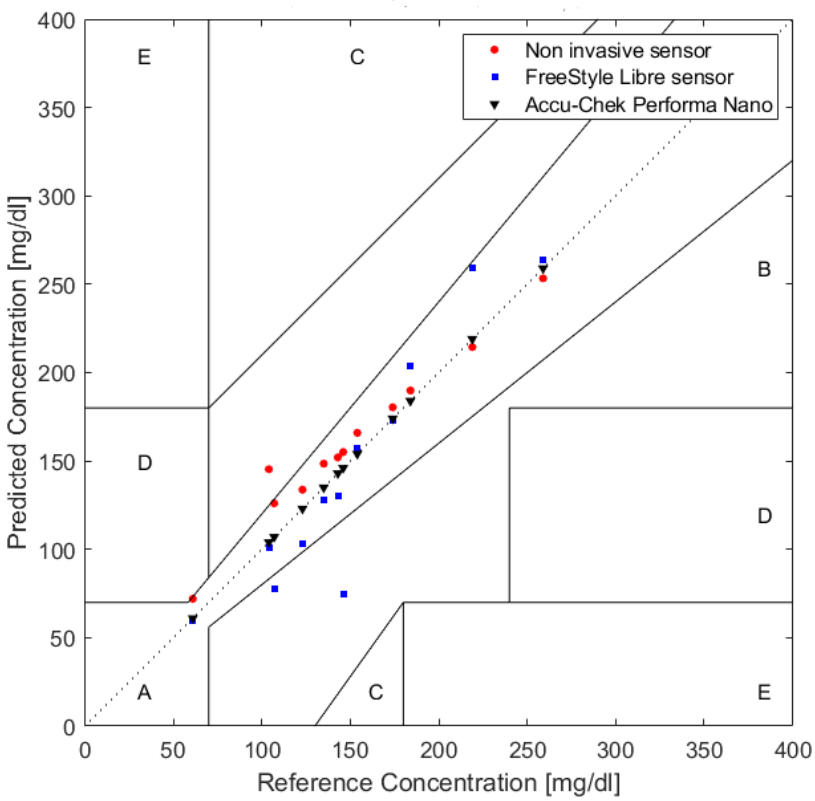

Figure 7 Clarke's error grid analysis.

CONCLUSSIONS

A glucose estimation value using the PPG signal information and calculating the light absorbance by the human tissue was the main objective of the present research and was successfully accomplished using a PLS regression for calibrate the model. From the experimental test, the RMSE between the blood glucose and the non invasive sensor is 11 mg/dl which is more accurate than the RMSE of the blood glucose and the FreeStyle libre sensor. Moreover, when analyzing the Clarke's grid error, it was possible to obtain that 91.67 % of the data was in zone A and 8.33 % of the data was in zone B therefore this results are clinically acceptable as long as there is no estimated glucose in zones C, D and E. Moreover, from the experimental test, it can be concluded that the non invasive sensor has a more accurate estimation than the FreeStyle Libre which only presented 83.67 % of data in zone A and 16.67 % of data in zone B.

Despite the lack of data to calibrate the model and test how well it behaves when it has to predict glucose value compared to other investigations, the results obtained are promising. Especially, although there was not much data, the non invasive sensor shows better RMSE than the FreeStyle Libre when compared to blood glucose. Besides, the estimated glucose could be considered clinically valid for the subject we obtained the information.

Future work

As this was the first step towards a non invasive glucose sensor, it is consider that for future work involving this method, the amount of data must be large enough to obtain more reliable results and a better calibration. Moreover, with more data it could be possible to have more feasible RMSE and Clark's error grid analysis so it can be clinically accepted. For the

estimation model, it could be implemented an artificial neural network where it considers other information that gives the PPG signal as blood pressure, blood oxygenation, respiration, heart rate and see if the model is better or not compared to the PLS regression model. Finally, this method could work as a closed loop with an insulin pump with the principal objective to imitates an artificial pancreas.

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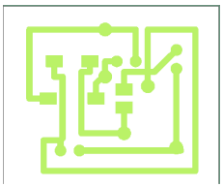
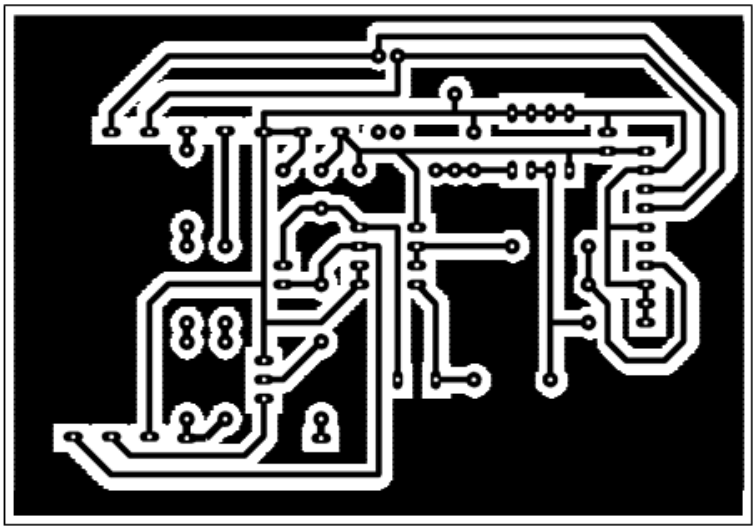
ANNEX A: SURFACE CONTACT PCB FOOTPRINT



ANNEX B: PCB CIRCUIT BOARD FOOTPRINT



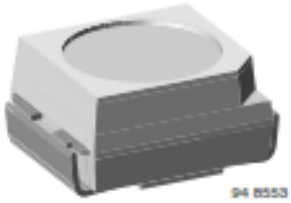
ANNEX C: DATASHEETS OF VSMB3940X01

VISHAY

VSMB3940X01

Vishay Semiconductors

High Speed Infrared Emitting Diode, 940 nm, GaAlAs Double Hetero



FEATURES

- Package type: surface mount
- Package form: PLCC-2
- Dimensions (L x W x H in mm): 3.5 x 2.8 x 1.75
- Peak wavelength: λ_p = 940 nm
- High reliability
- High radiant power
- High radiant intensity
- Angle of half intensity: φ = ± 60°
- Low forward voltage
- Suitable for high pulse current operation
- High modulation bandwidth: f_c = 24 MHz
- Good spectral matching with Si photodetectors
- Floor life: 168 h, MSL 3, acc. J-STD-020
- Lead (Pb)-free reflow soldering acc. J-STD-020
- AEC-Q101 qualified
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC
- Find out more about Vishay's Automotive Grade Product requirements at: www.vishay.com/applications

AUTOMOTIVE GRADE

Pb-free

e3

RoHS COMPLIANT

GREEN (5-2008)**

DESCRIPTION

VSMB3940X01 is an infrared, 940 nm emitting diode in GaAlAs double hetero (DH) technology with high radiant power and high speed, molded in a PLCC-2 package for surface mounting (SMD).

APPLICATIONS

- IrDA compatible data transmission
- Miniature light barrier
- Photointerrupters
- Optical switch
- Control and drive circuits
- Shaft encoders

PRODUCT SUMMARY

COMPONENT	I_e (mW/sr)	φ (deg)	λ_p (nm)	t_r (ns)
VSMB3940X01	13	± 60	940	15

Note

Test conditions see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
VSMB3940X01-GS08	Tape and reel	MOQ: 7500 pcs, 1500 pcs/reel	PLCC-2
VSMB3940X01-GS18	Tape and reel	MOQ: 8000 pcs, 8000 pcs/reel	PLCC-2

Note

MOQ: minimum order quantity

** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

VSMB3940X01

Vishay Semiconductors High Speed Infrared Emitting Diode, 940 nm, GaAlAs Double Hetero

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
Reverse voltage		V_R	5	V
Forward current		I_F	100	mA
Peak forward current	$t_p/T = 0.5$, $t_p = 100\ \mu s$	I_{FM}	200	mA
Surge forward current	$t_p = 100\ \mu s$	I_{FSM}	1	A
Power dissipation		P_V	160	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	- 40 to + 85	°C
Storage temperature range		T_{stg}	- 40 to + 100	°C
Soldering temperature	$t \le 5$ s, 2 mm from case	T_{sd}	260	°C
Thermal resistance junction/ambient	J-STD-051, leads 7 mm, soldered on PCB	R_{thJA}	250	K/W

Note

T_{amb} = 25 °C, unless otherwise specified

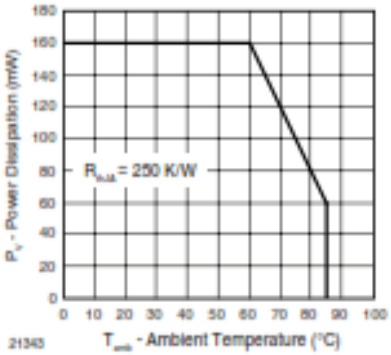


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

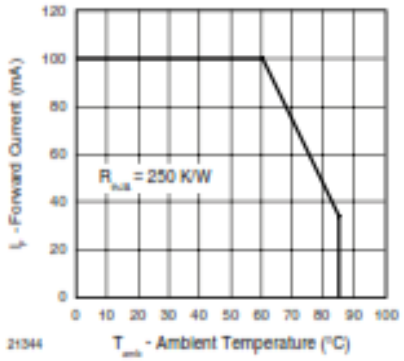


Fig. 2 - Forward Current Limit vs. Ambient Temperature

BASIC CHARACTERISTICS						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Forward voltage	$I_F = 100$ mA, $t_p = 20$ ms	V_F	1.15	1.35	1.6	V
	$I_F = 1$ A, $t_p = 100\ \mu s$	V_F		2.2		V
Temperature coefficient of V_F	$I_F = 1$ mA	TK_{VF}		- 1.8		mV/K
	$I_F = 100$ mA	TK_{VF}		- 1.1		mV/K
Reverse current	$V_R = 5$ V	I_R			10	µA
Junction capacitance	$V_R = 0$ V, $f = 1$ MHz, $E = 0$ mW/cm^2	C_J		70		pF
Radiant intensity	$I_F = 100$ mA, $t_p = 20$ ms	I_e	7	13	21	mW/sr
	$I_F = 1$ A, $t_p = 100\ \mu s$	I_e		130		mW/sr
Radiant power	$I_F = 100$ mA, $t_p = 20$ ms	ϕ_e		40		mW
Temperature coefficient of ϕ_e	$I_F = 1$ mA	$TK\phi_e$		- 1.1		%/K
	$I_F = 100$ mA	$TK\phi_e$		- 0.51		%/K
Angle of half intensity		φ		± 60		deg
Peak wavelength	$I_F = 30$ mA	λ_p		940		nm
Spectral bandwidth	$I_F = 30$ mA	$\Delta\lambda$		25		nm
Temperature coefficient of λ_p	$I_F = 30$ mA	$TK\lambda_p$		0.25		nm/K
Rise time	$I_F = 100$ mA, 20 % to 80 %	t_r		15		ns
Fall time	$I_F = 100$ mA, 20 % to 80 %	t_f		15		ns
Cut-off frequency	$I_{DC} = 70$ mA, $I_{AC} = 30$ mA pp	f_c		24		MHz
Virtual source diameter		d		0.5		mm

Note

T_{amb} = 25 °C, unless otherwise specified

For technical questions, contact: emittertechsupport@vishay.com

Document Number: 81894
Rev. 1.4, 06-Nov-09

BASIC CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

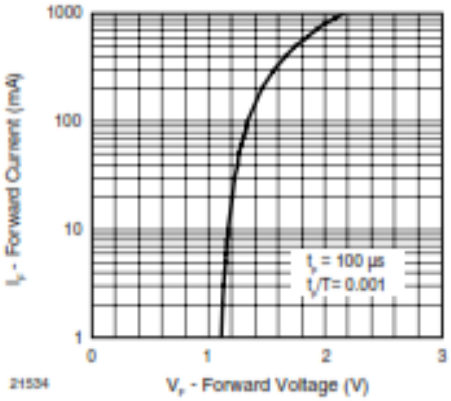


Fig. 3 - Forward Current vs. Forward Voltage

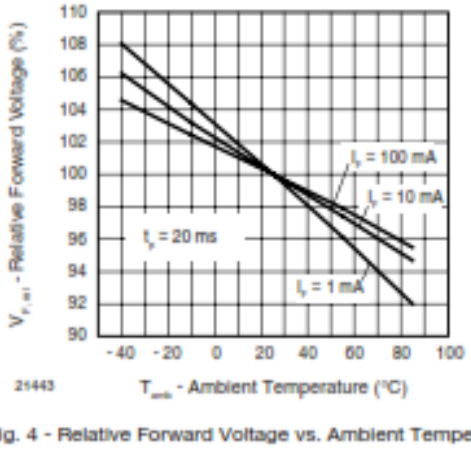


Fig. 4 - Relative Forward Voltage vs. Ambient Temperature

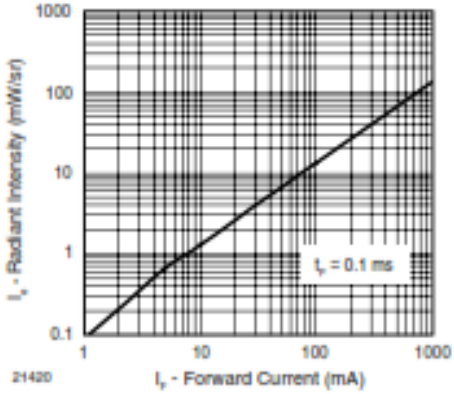
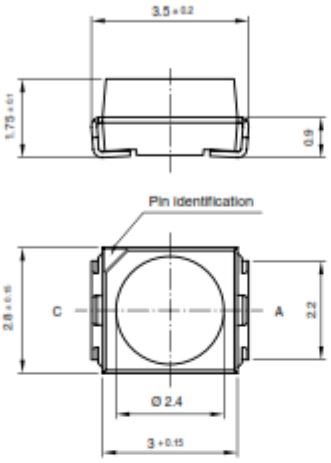


Fig. 5 - Radiant Intensity vs. Forward Current

VSMB3940X01

Vishay Semiconductors High Speed Infrared Emittin
940 nm, GaAlAs Double H

PACKAGE DIMENSIONS in millimeters



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Issue: 5; 04.11.08
20541

SOLDER PROFILE

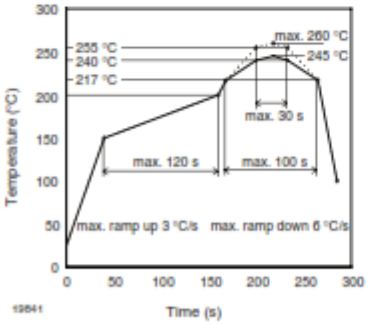

Fig. 9 - Lead (Pb)-free Reflow Solder Profile acc. J-STD-020

DRYPA
Devices
prevent
transport

FLOOR
Floor life
must not
Floor life:
Condition
Moisture

DRYING
In case
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Devices
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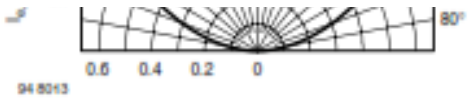
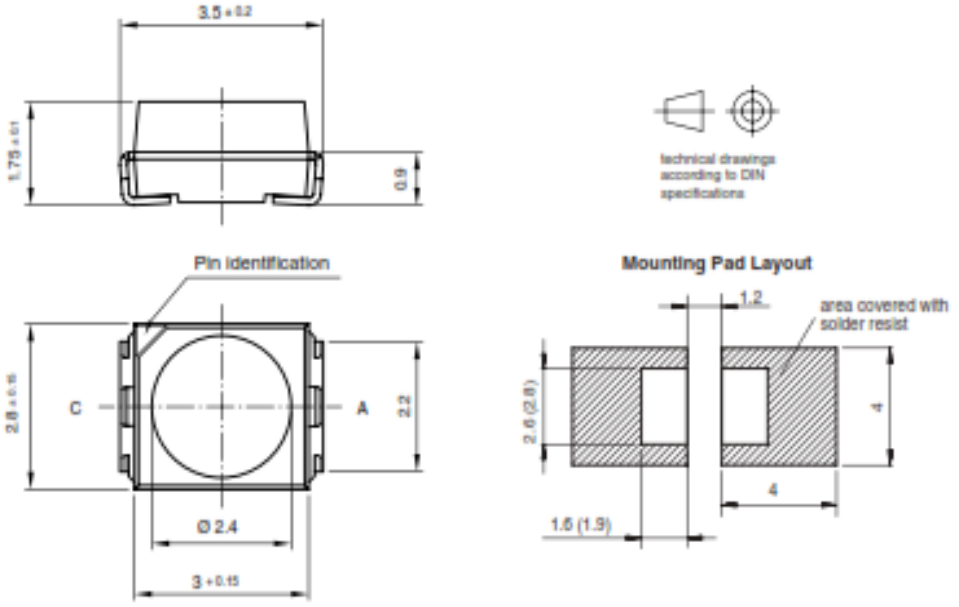


Fig. 8 - Relative Radiant Intensity vs. Angular Displacement

VSMB3940X01

Vishay Semiconductors High Speed Infrared Emitting Diode, 940 nm, GaAlAs Double Hetero

PACKAGE DIMENSIONS in millimeters



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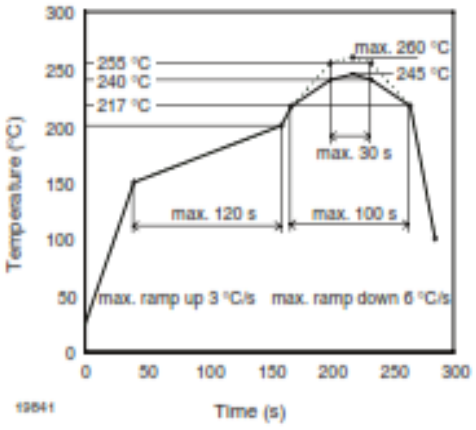

Fig. 9 - Lead (Pb)-free Reflow Solder Profile acc. J-STD-020

DRYPACK

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

FLOOR LIFE

Floor life (time between soldering and removing from MBB) must not exceed the time indicated on MBB label:
Floor life: 168 h
Conditions: T_{amb} < 30 °C, RH < 60 %
Moisture sensitivity level 3, acc. to J-STD-020.

DRYING

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions 192 h at 40 °C (+ 5 °C), RH < 5 %.

TAPE AND REEL

PLCC-2 components are packed in antistatic blister tape (DIN IEC (CO) 564) for automatic component insertion. Cavities of blister tape are covered with adhesive tape.

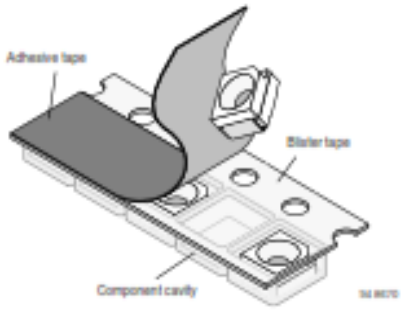

Fig. 10 - Blister Tape

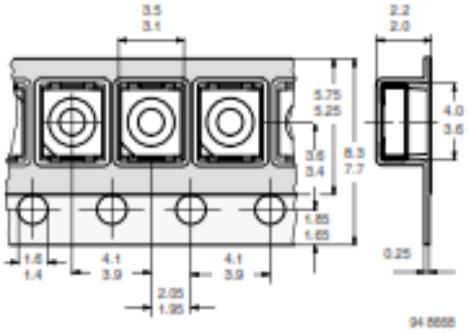

Fig. 11 - Tape Dimensions in mm for PLCC-2

MISSING DEVICES

A maximum of 0.5 % of the total number of components per reel may be missing, exclusively missing components at the beginning and at the end of the reel. A maximum of three consecutive components may be missing, provided this gap is followed by six consecutive components.

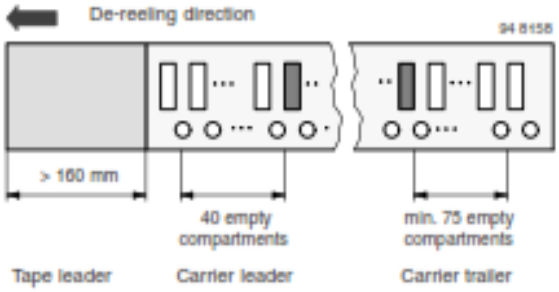

Fig. 12 - Beginning and End of Reel

The tape leader is at least 160 mm and is followed by a carrier tape leader with at least 40 empty compartements. The tape leader may include the carrier tape as long as the cover tape is not connected to the carrier tape. The least component is followed by a carrier tape trailer with a least 75 empty compartements and sealed with cover tape.

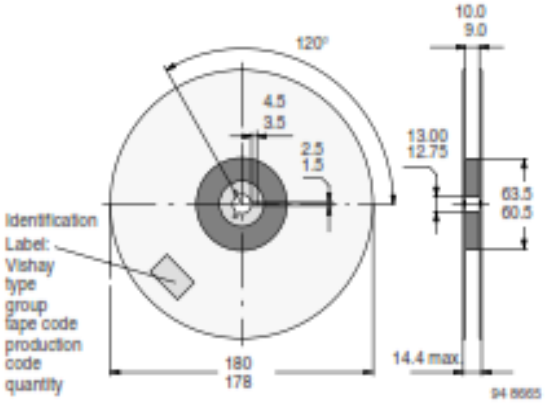

Fig. 13 - Dimensions of Reel-GS08

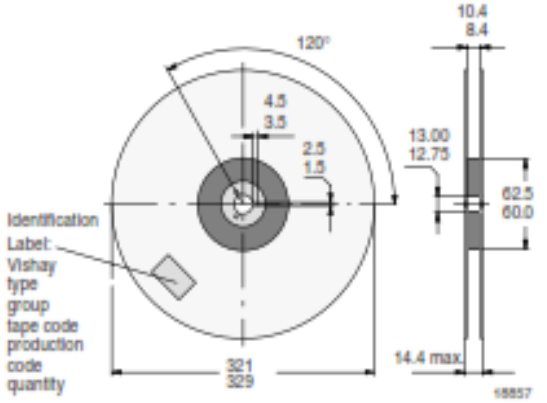

Fig. 14 - Dimensions of Reel-GS18

COVER TAPE REMOVAL FORCE

The removal force lies between 0.1 N and 1.0 N at a removal speed of 5 mm/s. In order to prevent components from popping out of the blisters, the cover tape must be pulled off at an angle of 180° with regard to the feed direction.

Legal Disclaimer Notice

Vishay

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ANNEX D: DATASHEET OF VSLY5850

High Speed Infrared Emitting Diode, 850 nm, Surface Emitter Technology

FEATURES

- Package type: leaded
- Package form: T-1¾
- Dimensions (in mm): Ø 5
- Leads with stand-off
- Peak wavelength: λ_p = 850 nm
- High reliability
- High radiant power
- High radiant intensity
- Narrow angle of half intensity: φ = ± 3°
- Suitable for high pulse current operation
- Good spectral matching with CMOS cameras
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE
GREEN

DESCRIPTION

As part of the SurfLight™ portfolio, the VSLY5850 is an infrared, 850 nm emitting diode based on GaAlAs surface emitter chip technology with extreme high radiant intensity, high optical power and high speed, molded in a clear, untinted plastic package, with a parabolic lens.

APPLICATIONS

- Infrared radiation source for operation with CMOS cameras
- High speed IR data transmission
- Smoke-automatic fire detectors
- IR Flash

PRODUCT SUMMARY

COMPONENT	I_e (mW/sr)	φ (deg)	λ_p (nm)	t_r (ns)
VSLY5850	600	± 3	850	10

Note

- Test conditions see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
VSLY5850	Bulk	MOQ: 4000 pcs, 4000 pcs/bulk	T-1¾

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	5	V
Forward current		I_F	100	mA
Peak forward current	t_p/T = 0.5, t_p = 100 µs	I_{FM}	200	mA
Surge forward current	t_p = 100 µs	I_{FSM}	1	A
Power dissipation		P_V	190	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	- 40 to + 85	°C
Storage temperature range		T_{stg}	- 40 to + 100	°C
Soldering temperature	t ≤ 5 s, 2 mm from case	T_{sd}	260	°C
Thermal resistance junction/ambient	J-STD-051, leads 7 mm, soldered on PCB	R_{thJA}	230	K/W

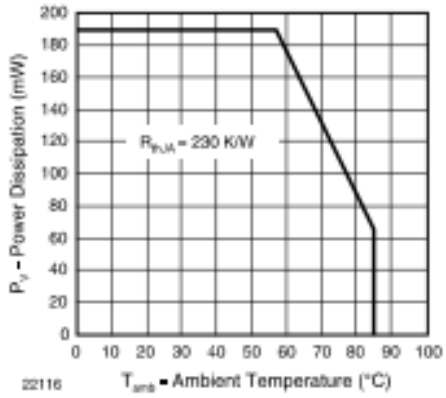


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

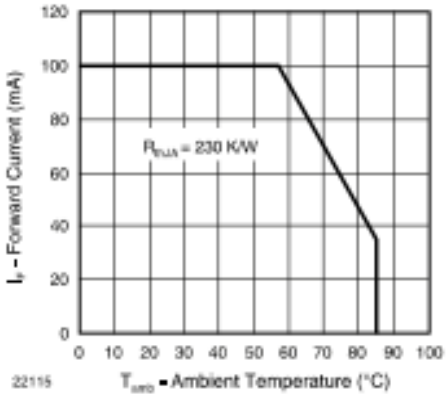


Fig. 2 - Forward Current Limit vs. Ambient Temperature

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Forward voltage	I_F = 100 mA, t_p = 20 ms	V_F		1.65	1.9	V
	I_F = 1 A, t_p = 100 µs	V_F		2.9		V
Temperature coefficient of V_F	I_F = 1 mA	TK_{VF}		- 1.45		mV/K
	I_F = 10 mA	TK_{VF}		- 1.25		mV/K
Reverse current		I_R	not designed for reverse operation			µA
Junction capacitance	V_R = 0 V, f = 1 MHz, E = 0	C_j		125		pF
Radiant intensity	I_F = 100 mA, t_p = 20 ms	I_e	300	600	900	mW/sr
	I_F = 1 A, t_p = 100 µs	I_e		5100		mW/sr
Radiant power	I_F = 100 mA, t_p = 20 ms	ϕ_e		55		mW
Temperature coefficient of ϕ_e	I_F = 100 mA	$TK\phi_e$		- 0.35		%/K
Angle of half intensity		φ		± 3		deg
Peak wavelength	I_F = 100 mA	λ_p	840	850	870	nm
Spectral bandwidth	I_F = 100 mA	$\Delta\lambda$		30		nm
Temperature coefficient of λ_p	I_F = 100 mA	$TK\lambda_p$		0.25		nm/K
Rise time	I_F = 100 mA	t_r		10		ns
Fall time	I_F = 100 mA	t_f		10		ns

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

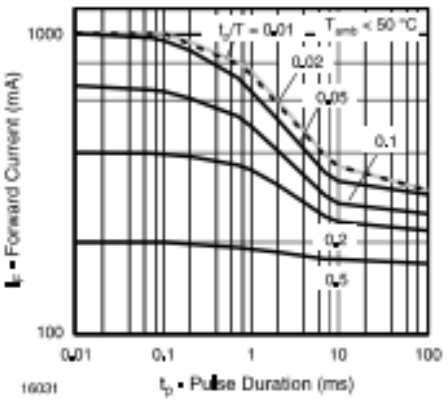


Fig. 3 – Pulse Forward Current vs. Pulse Duration

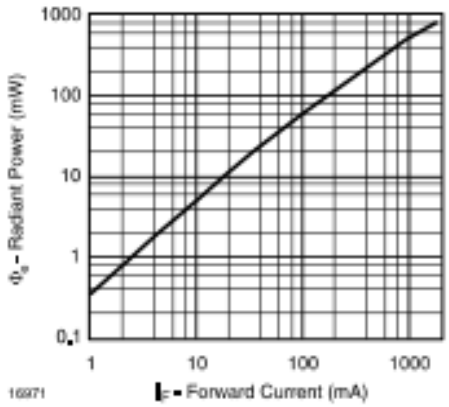


Fig. 6 – Radiant Power vs. Forward Current

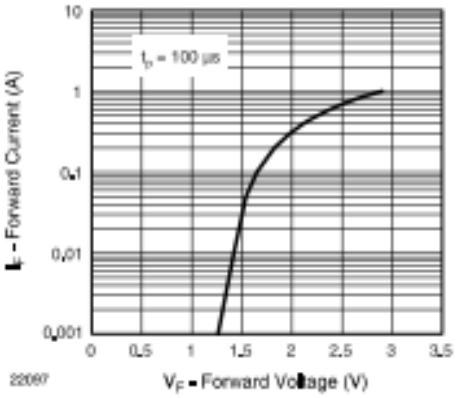


Fig. 4 – Forward Current vs. Forward Voltage

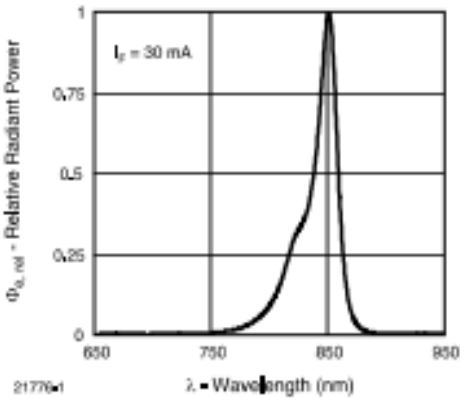


Fig. 7 – Relative Radiant Power vs. Wavelength

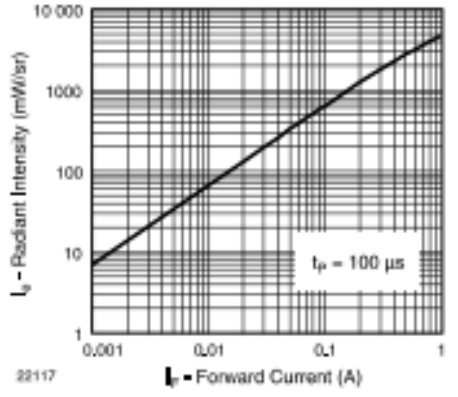


Fig. 5 – Radiant Intensity vs. Forward Current

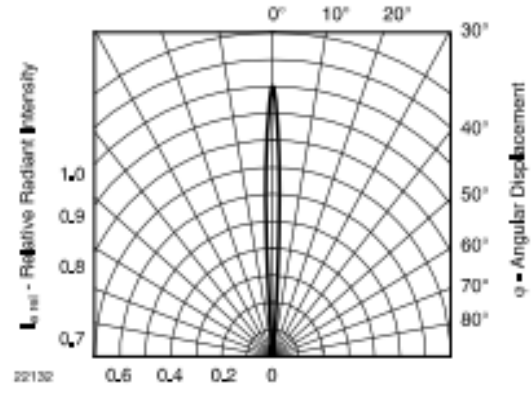
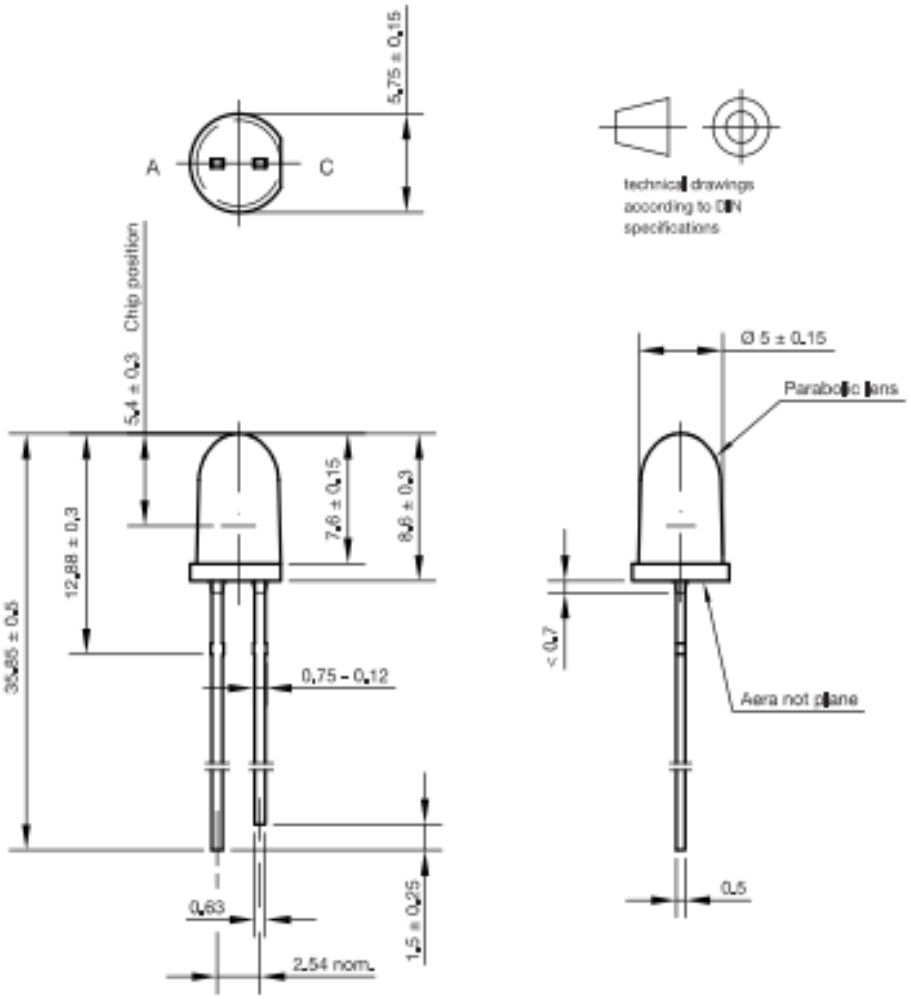


Fig. 8 – Relative Radiant Intensity vs. Angular Displacement

PACKAGE DIMENSIONS in millimeters



Drawing-No.: 6.544-5385.01-4
Issue: 2; 08.03.10
20631

Not indicated tolerances ± 0,1

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ANNEX E: DATASHEET OF QSB34GR

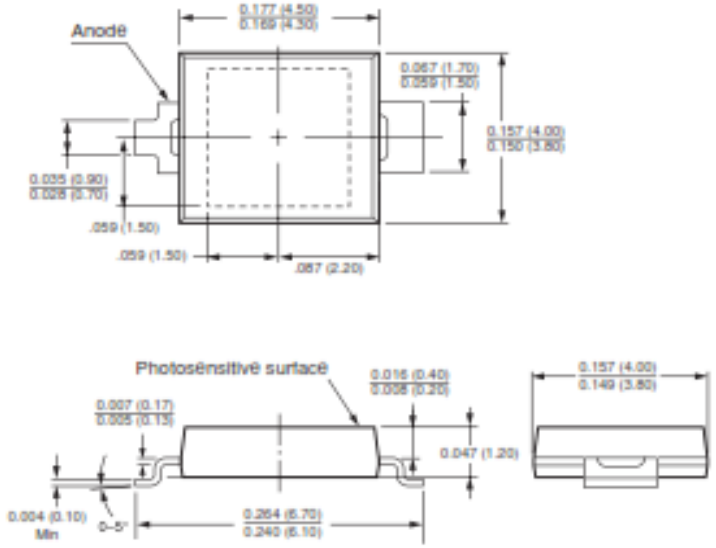
FAIRCHILD SEMICONDUCTOR®

SURFACE MOUNT SILICON PIN PHOTODIODE

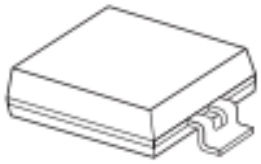
QSB34

QSB34GR, QSB34ZR

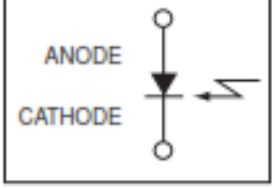
PACKAGE DIMENSIONS, QSB34GR



NOTE:
1. Dimensions for all drawings are in inches (mm).
2. Tolerance of ±.005 (.13) on all non-nominal dimensions unless otherwise specified.



SCHEMATIC



FEATURES

- Daylight Filter
- Surface Mount Packages:
  – QSB34GR for overmount board
  – QSB34ZR for undermount board
- Fast PIN Photodiode
- Wide Reception Angle, 120°
- Large Chip Size = .014 in^2 (9 mm^2)
- High Sensitivity
- Low Capacitance
- Available in 0.470" (12mm) width tape on 7" (178mm) diameter reel; 1,000 units per reel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Operating Temperature	T_{OPR}	-40 to +85	°C
Storage Temperature	T_{STG}	-40 to +85	°C
Soldering Temperature (Reflow)[2,3]	T_{SOL-F}	240 for 5 sec	°C
Reverse Voltage	V_R	32	V
Power Dissipation[1]	P_D	150	mW

Notes:
1. Derate power dissipation linearly 2.50 mW/°C above 25°C.
2. Solder iron (15W max temp 260°C for 5 max sec.)
3. Methanol or isopropyl alcohols are recommended as cleaning agents.
4. Light source is an GaAs LED which has a peak emission wavelength of 940 nm.

FAIRCHILD SEMICONDUCTOR®

SURFACE MOUNT SILICON PIN PHOTODIODE

QSB34

QSB34GR, QSB34ZR

ELECTRICAL / OPTICAL CHARACTERISTICS (T_A =25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Reverse Voltage	I_R = 0.1 mA	V_R	32		—	V
Dark Reverse Current	V_R = 10 V	$I_{R(D)}$	—		30	nA
Peak Sensitivity	V_R = 5 V	λ_{PK}		940		nm
Reception Angle @ 1/2 Power		Θ		±60		Degrees
Photo Current	Ee = 1.0 mW/cm^2, V_{CE} = 5 V[4]	I_{PH}	25	37	—	µA
Capacitance	V_R = 3 V	C		25		pF
Rise Time Fall Time	V_R = 10 V, R_L = 50 Ω	t_r t_f		20 20		ns ns
Spectral Sensitivity		S_λ		.40		A/W

TYPICAL PERFORMANCE CURVES

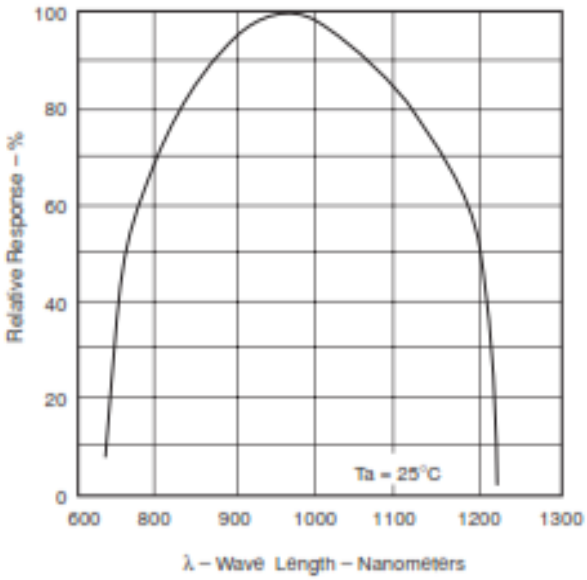


Fig. 1 Relative Spectral Sensitivity vs. Wavelength

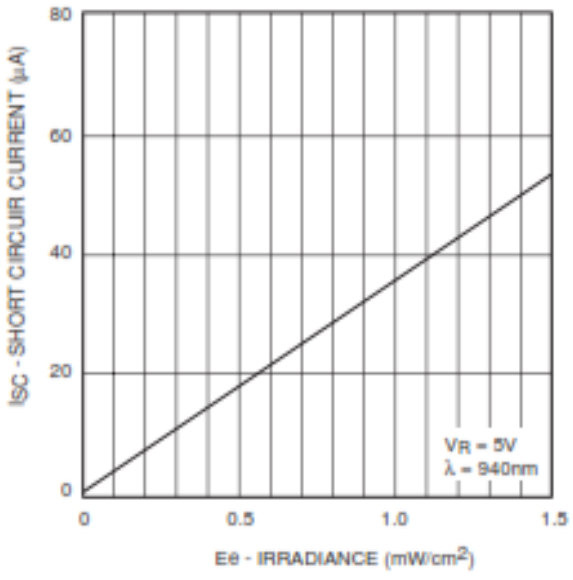


Fig. 2 Short Circuit Current vs. Irradiance

FAIRCHILD
SEMICONDUCTOR®

SURFACE MOUNT SILICON PIN PHOTODIODE

QSB34

QSB34GR, QSB34ZR

TYPICAL PERFORMANCE CURVES (Cont.)

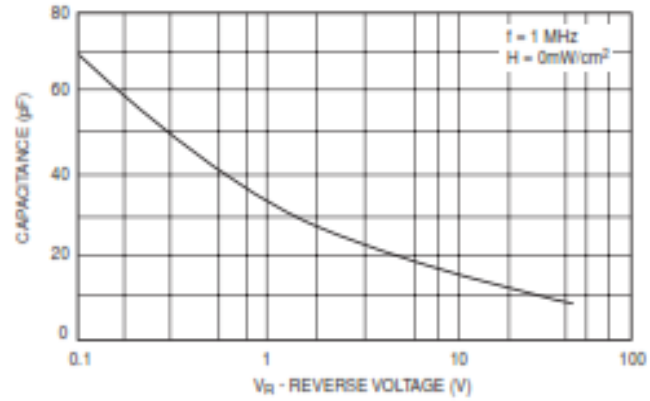


Fig. 3 Capacitance vs. Reverse Voltage

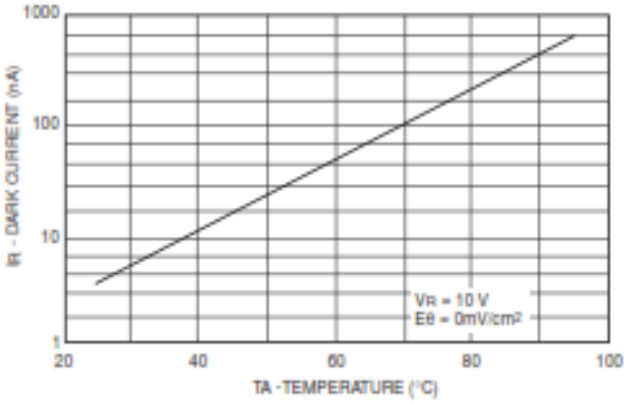


Fig. 4 Dark Current vs. Temperature

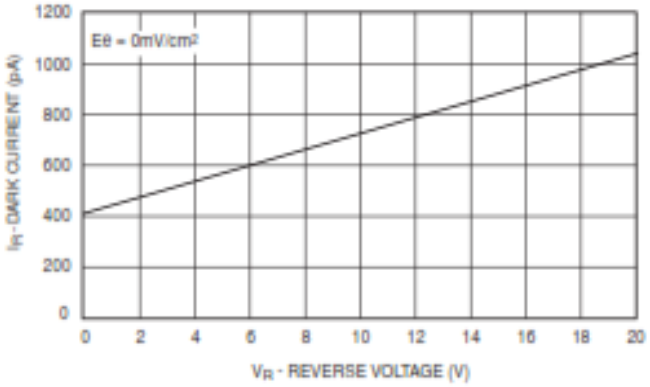


Fig. 5 Dark Current vs. Reverse Voltage

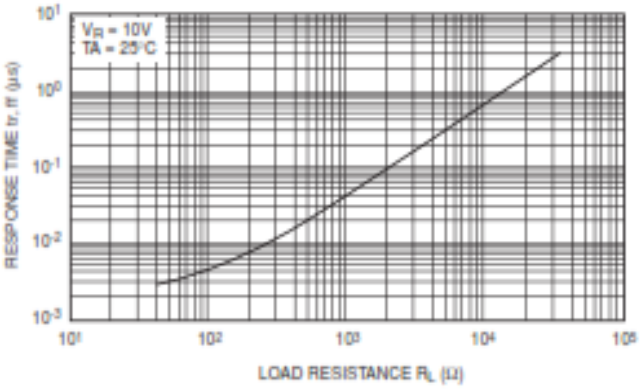


Fig. 6 Response Time vs. Load Resistance

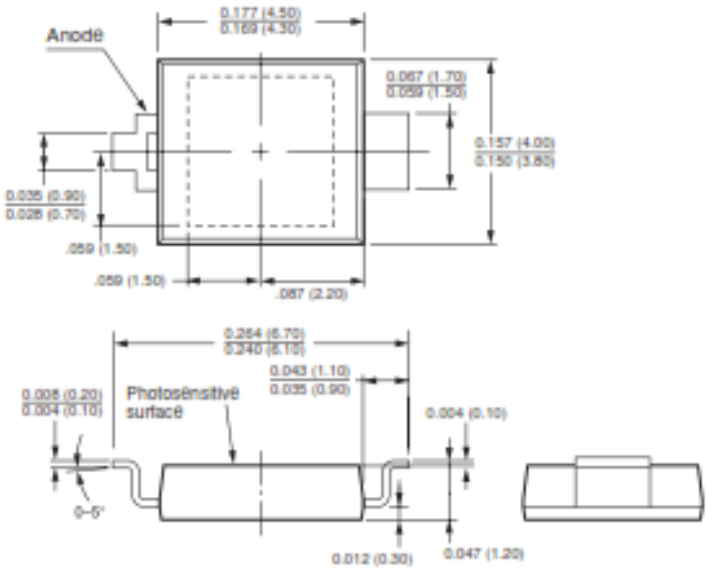
FAIRCHILD
SEMICONDUCTOR®

SURFACE MOUNT SILICON PIN PHOTODIODE

QSB34

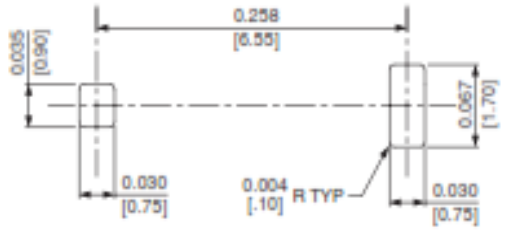
QSB34GR, QSB34ZR

PACKAGE DIMENSIONS, QSB34ZR

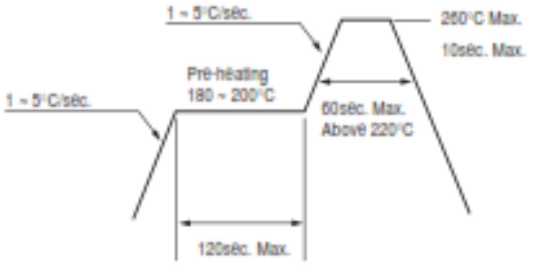


NOTE:
1. Dimensions for all drawings are in inches (mm).
2. Tolerance of ±.005 (.13) on all non-nominal dimensions unless otherwise specified.

RECOMMENDED SOLDER SCREEN PATTERN (For Reference Only)



RECOMMENDED IR REFLOW SOLDERING PROFILE



ORDERING INFORMATION	
Option	**Description**
QSB34GR	Gullwing, 1000 units per reel
QSB34ZR	Z-Bend reversed, 1000 units per reel

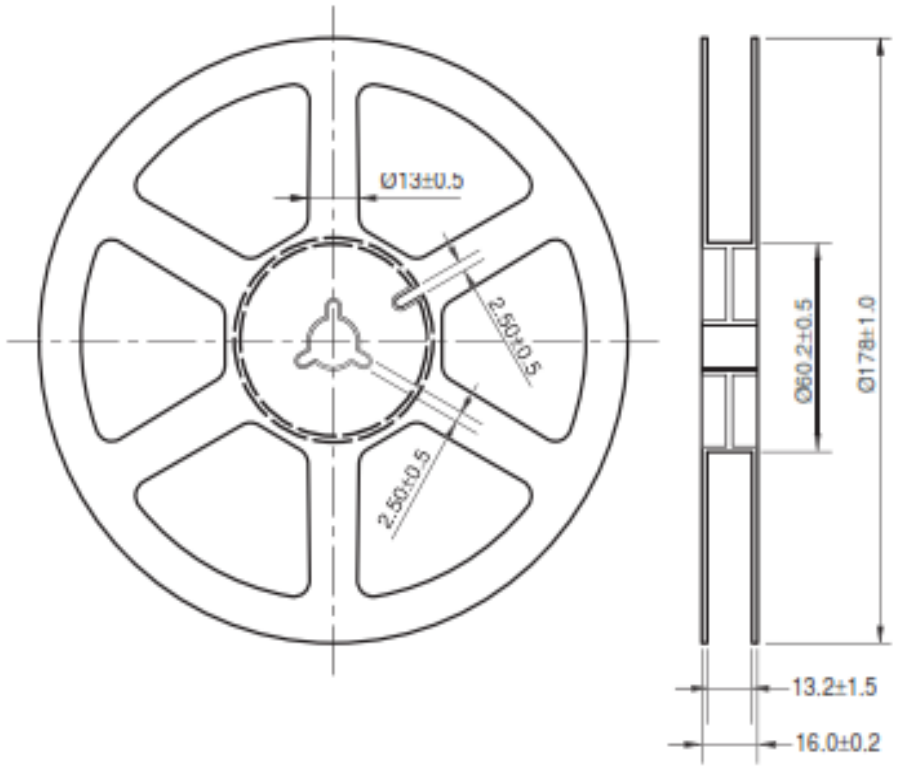
FAIRCHILD
SEMICONDUCTOR®

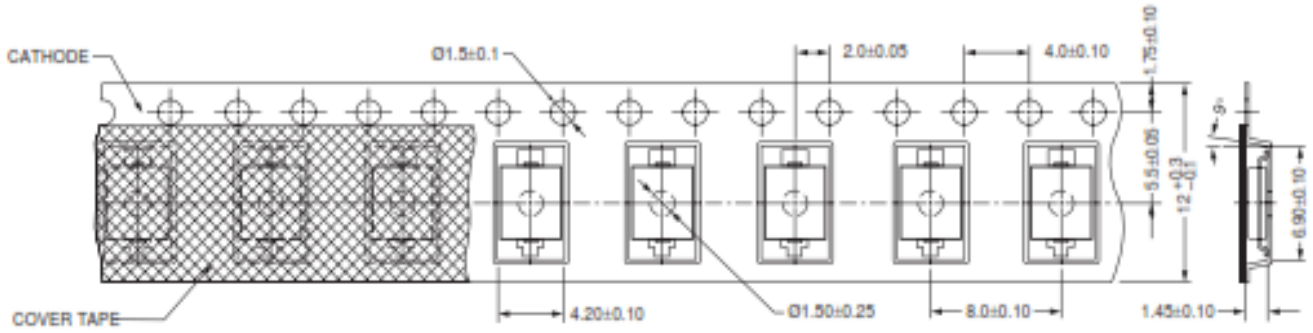
SURFACE MOUNT SILICON PIN PHOTODIODE

QSB34

QSB34GR, QSB34ZR

TAPE & REEL DIMENSIONS





Unit: mm

FAIRCHILD
SEMICONDUCTOR®

SURFACE MOUNT SILICON PIN PHOTODIODE

QSB34

QSB34GR, QSB34ZR

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANNEX F: DATASHEET OF ADS1115

TEXAS INSTRUMENTS

ADS1113
ADS1114
ADS1115

www.ti.com

SBAS444A – MAY 2009 – REVISED AUGUST 2009

Ultra-Small, Low-Power, 16-Bit Analog-to-Digital Converter with Internal Reference

Check for Samples: ADS1113 ADS1114 ADS1115

FEATURES

- ULTRA-SMALL QFN PACKAGE: 2mm × 1,5mm × 0,4mm
- WIDE SUPPLY RANGE: 2.0V to 5.5V
- LOW CURRENT CONSUMPTION: Continuous Mode: Only 150µA Single-Shot Mode: Auto Shut-Down
- PROGRAMMABLE DATA RATE: 8SPS to 860SPS
- INTERNAL LOW-DRIFT VOLTAGE REFERENCE
- INTERNAL OSCILLATOR
- INTERNAL PGA
- I²C ™ INTERFACE: Pin-Selectable Addresses
- FOUR SINGLE-ENDED OR TWO DIFFERENTIAL INPUTS (ADS1115)
- PROGRAMMABLE COMPARATOR (ADS1114 and ADS1115)
- OPERATING TEMPERATURE: –40°C to +140°C

APPLICATIONS

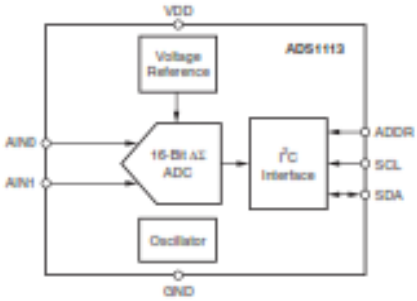
- PORTABLE INSTRUMENTATION
- CONSUMER GOODS
- BATTERY MONITORING
- TEMPERATURE MEASUREMENT
- FACTORY AUTOMATION AND PROCESS CONTROLS

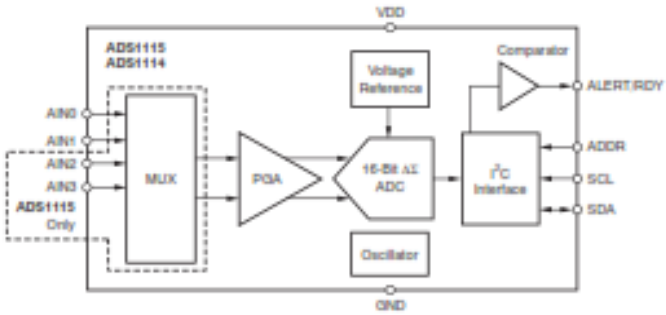
DESCRIPTION

The ADS1113, ADS1114, and ADS1115 are precision analog-to-digital converters (ADCs) with 16 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1113/4/5 are designed with precision, power, and ease of implementation in mind. The ADS1113/4/5 feature an onboard reference and oscillator. Data are transferred via an I²C-compatible serial interface; four I²C slave addresses can be selected. The ADS1113/4/5 operate from a single power supply ranging from 2.0V to 5.5V.

The ADS1113/4/5 can perform conversions at rates up to 860 samples per second (SPS). An onboard PGA is available on the ADS1114 and ADS1115 that offers input ranges from the supply to as low as ±256mV, allowing both large and small signals to be measured with high resolution. The ADS1115 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

The ADS1113/4/5 operate either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1113/4/5 are specified from –40°C to +125°C.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)

	ADS1113, ADS1114, ADS1115	UNIT
VDD to GND	–0.3 to +5.5	V
Analog input current	100, momentary	mA
Analog input current	10, continuous	mA
Analog input voltage to GND	–0.3 to VDD + 0.3	V
SDA, SCL, ADDR, ALERT/RDY voltage to GND	–0.5 to +5.5	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +140	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT FAMILY

DEVICE	PACKAGE DESIGNATOR MSOP/QFN	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	COMPARATOR	PGA	INPUT CHANNELS (Differential/ Single-Ended)
ADS1113	BRO/N6J	16	860	No	No	1/1
ADS1114	BRN/N5J	16	860	Yes	Yes	1/1
ADS1115	BOG/N4J	16	860	Yes	Yes	2/4
ADS1013	BRM/N9J	12	3300	No	No	1/1
ADS1014	BRQ/N8J	12	3300	Yes	Yes	1/1
ADS1015	BRP/N7J	12	3300	Yes	Yes	2/4

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C.

PARAMETER	TEST CONDITIONS	ADS1113, ADS1114, ADS1115			UNIT
		MIN	TYP	MAX	
ANALOG INPUT					
Full-scale input voltage (1)	$V_{IN} = (AIN_P) - (AIN_N)$		±4.096/PGA		V
Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Differential input impedance			See Table 2		
Common-mode input impedance	FS = ±6.144V (1)		10		MΩ
	FS = ±4.096V (1), ±2.048V		6		MΩ
	FS = ±1.024V		3		MΩ
	FS = ±0.512V, ±0.256V		100		MΩ
SYSTEM PERFORMANCE					
Resolution	No missing codes	16			Bits
Data rate (DR)			8, 16, 32, 64, 128, 250, 475, 860		SPS
Data rate variation	All data rates	–10		10	%
Output noise		See Typical Characteristics			
Integral nonlinearity	DR = 8SPS, FS = ±2.048V, best fit (2)			1	LSB
Offset error	FS = ±2.048V, differential inputs		±1	±3	LSB
	FS = ±2.048V, single-ended inputs		±3		LSB
Offset drift	FS = ±2.048V		0.005		LSB/°C
Offset power-supply rejection	FS = ±2.048V		1		LSB/V
Gain error (3)	FS = ±2.048V at 25°C		0.01	0.15	%
Gain drift (3)	FS = ±0.256V		7		ppm/°C
	FS = ±2.048V		5	40	ppm/°C
	FS = ±6.144V (1)		5		ppm/°C
Gain power-supply rejection			80		ppm/V
PGA gain match (3)	Match between any two PGA gains		0.02	0.1	%
Gain match	Match between any two inputs		0.05	0.1	%
Offset match	Match between any two inputs		3		LSB
Common-mode rejection	At dc and FS = ±0.256V		105		dB
	At dc and FS = ±2.048V		100		dB
	At dc and FS = ±6.144V (1)		90		dB
	f_{CM} = 60Hz, DR = 8SPS		105		dB
	f_{CM} = 50Hz, DR = 8SPS		105		dB
DIGITAL INPUT/OUTPUT					
Logic level					
V_{IH}		0.7VDD		5.5	V
V_{IL}		GND – 0.5		0.3VDD	V
V_{OL}	I_{OL} = 3mA	GND	0.15	0.4	V
Input leakage					
I_H	V_{IH} = 5.5V			10	µA
I_L	V_{IL} = GND	10			µA

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.
(2) 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.

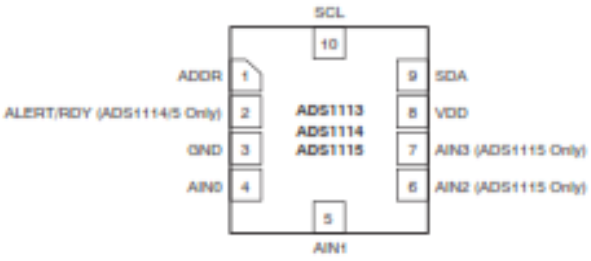
ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C.

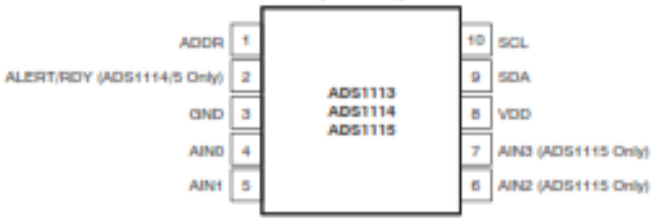
PARAMETER	TEST CONDITIONS	ADS1113, ADS1114, ADS1115			UNIT
		MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage		2		5.5	V
Supply current	Power-down current at 25°C		0.5	2	µA
	Power-down current up to 125°C			5	µA
	Operating current at 25°C		150	200	µA
	Operating current up to 125°C			300	µA
Power dissipation	VDD = 5.0V		0.9		mW
	VDD = 3.3V		0.5		mW
	VDD = 2.0V		0.3		mW
TEMPERATURE					
Storage temperature		–60		+150	°C
Operating temperature		–40		+140	°C
Specified temperature		–40		+125	°C

PIN CONFIGURATIONS

RUG PACKAGE
QFN-10
(TOP VIEW)



DGS PACKAGE
MSOP-10
(TOP VIEW)



PIN DESCRIPTIONS

PIN #	DEVICE			ANALOG/ DIGITAL INPUT/ OUTPUT	DESCRIPTION
	ADS1113	ADS1114	ADS1115		
1	ADDR	ADDR	ADDR	Digital Input	I²C slave address select
2	NC (1)	ALERT/RDY	ALERT/RDY	Digital Output	Digital comparator output or conversion ready (NC for ADS1113)
3	GND	GND	GND	Analog	Ground
4	AIN0	AIN0	AIN0	Analog Input	Differential channel 1: Positive input or single-ended channel 1 input
5	AIN1	AIN1	AIN1	Analog Input	Differential channel 1: Negative input or single-ended channel 2 input
6	NC	NC	AIN2	Analog Input	Differential channel 2: Positive input or single-ended channel 3 input (NC for ADS1113/4)
7	NC	NC	AIN3	Analog Input	Differential channel 2: Negative input or single-ended channel 4 input (NC for ADS1113/4)
8	VDD	VDD	VDD	Analog	Power supply: 2.0V to 5.5V
9	SDA	SDA	SDA	Digital I/O	Serial data: Transmits and receives data
10	SCL	SCL	SCL	Digital Input	Serial clock input: Clocks data on SDA

(1) NC pins may be left floating or tied to ground.

TIMING REQUIREMENTS

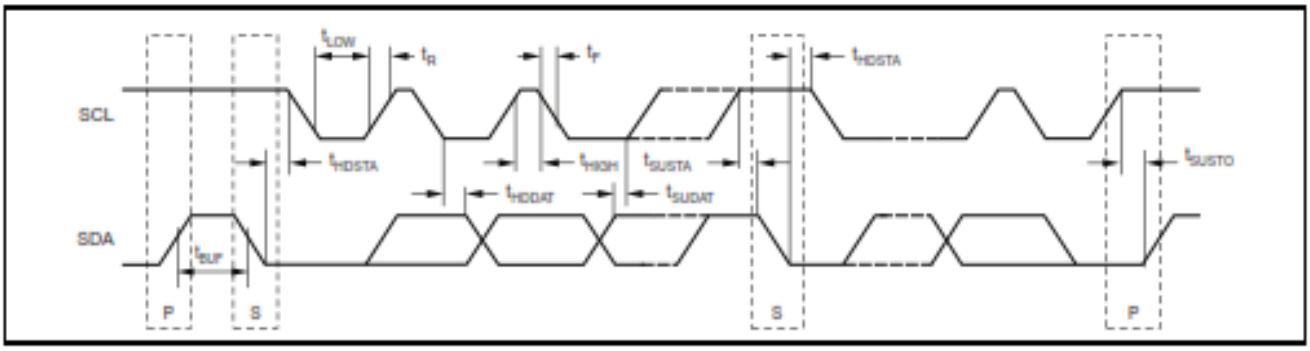


Figure 1. I²C Timing Diagram

Table 1. I²C Timing Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL operating frequency	f_{SCL}	0.01	0.4	0.01	3.4	MHz
Bus free time between START and STOP condition	t_{BUF}	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	t_{HDSTA}	600		160		ns
Repeated START condition setup time	t_{SUSTA}	600		160		ns
Stop condition setup time	t_{SUSTO}	600		160		ns
Data hold time	t_{HDDAT}	0		0		ns
Data setup time	t_{SUDAT}	100		10		ns
SCL clock low period	t_{LOW}	1300		160		ns
SCL clock high period	t_{HIGH}	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns

TYPICAL CHARACTERISTICS

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

OPERATING CURRENT vs TEMPERATURE

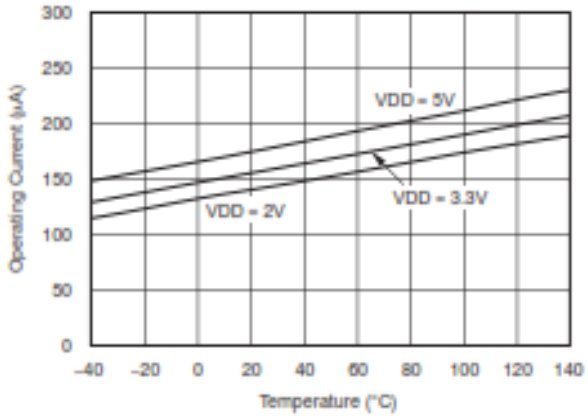


Figure 2.

SHUTDOWN CURRENT vs TEMPERATURE

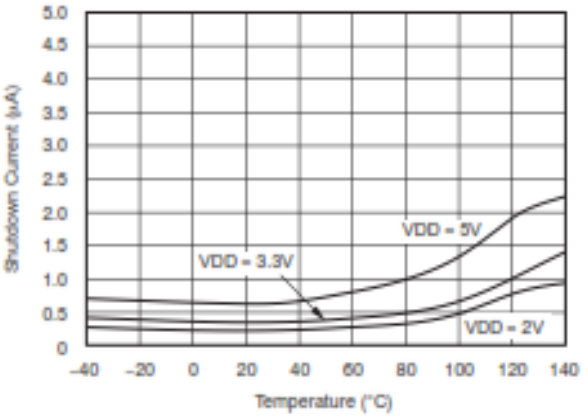


Figure 3.

SINGLE-ENDED OFFSET ERROR vs TEMPERATURE (1)

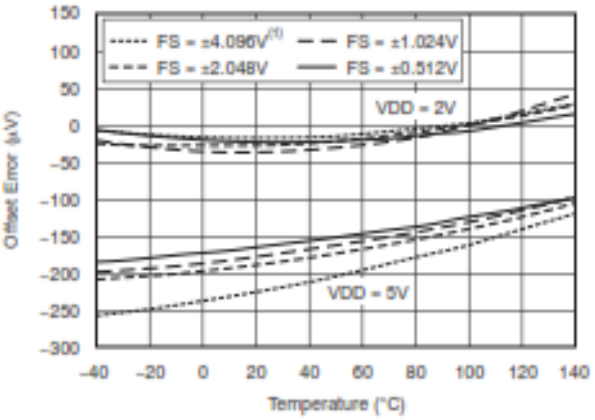


Figure 4.

DIFFERENTIAL OFFSET vs TEMPERATURE

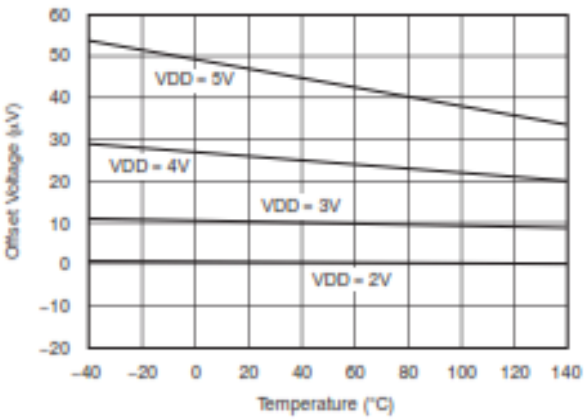


Figure 5.

GAIN ERROR vs TEMPERATURE

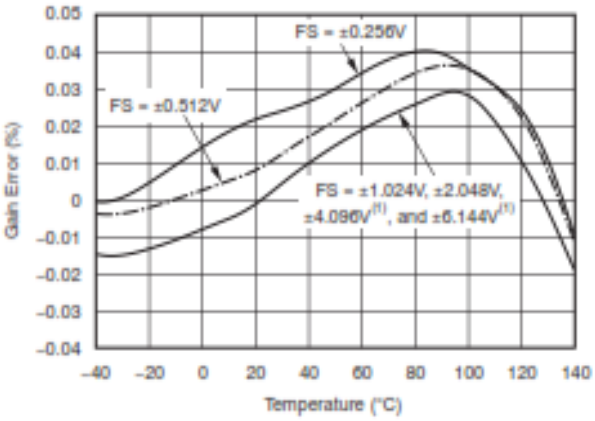


Figure 6.

GAIN ERROR vs SUPPLY

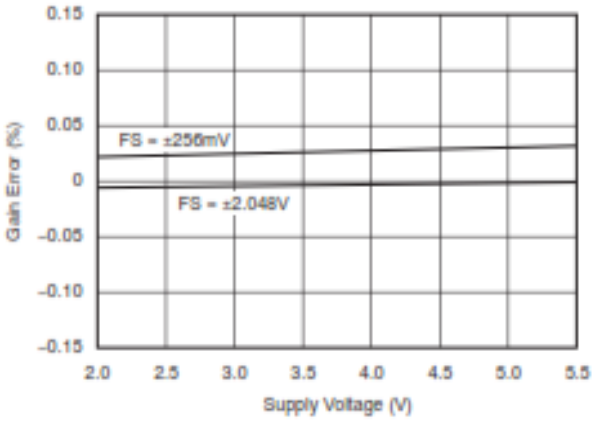


Figure 7.

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

INL vs SUPPLY VOLTAGE(2)

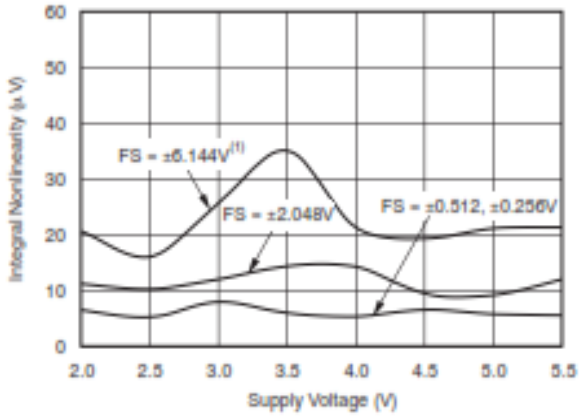


Figure 8.

INL vs INPUT SIGNAL

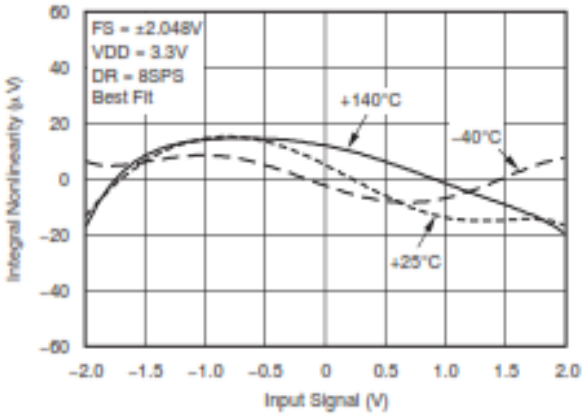


Figure 9.

INL vs INPUT SIGNAL

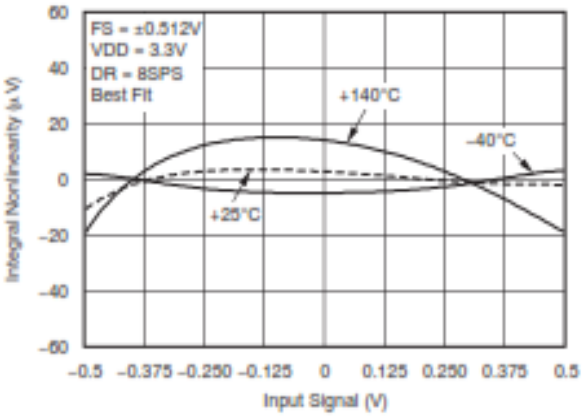


Figure 10.

INL vs INPUT SIGNAL

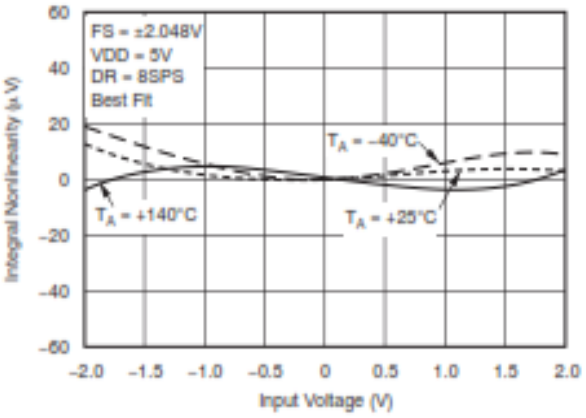


Figure 11.

INL vs INPUT SIGNAL

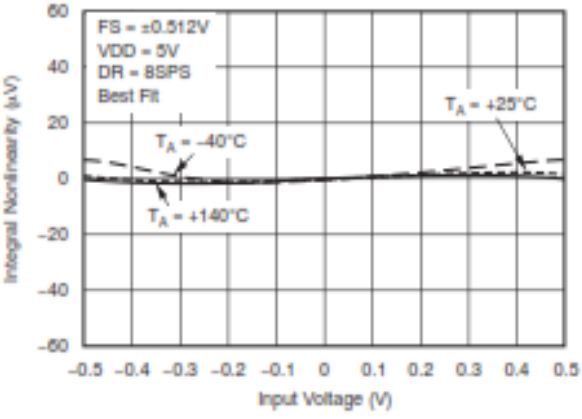


Figure 12.

INL vs TEMPERATURE

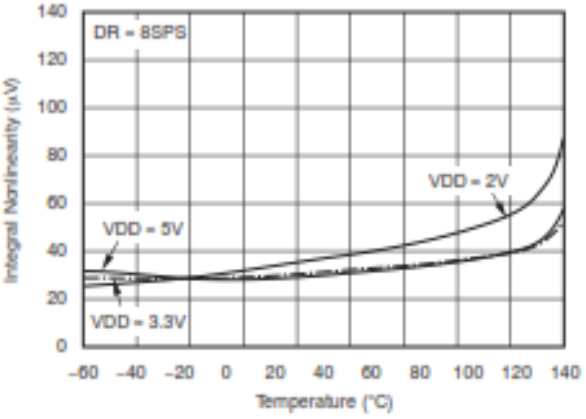


Figure 13.

(2) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

NOISE vs INPUT SIGNAL

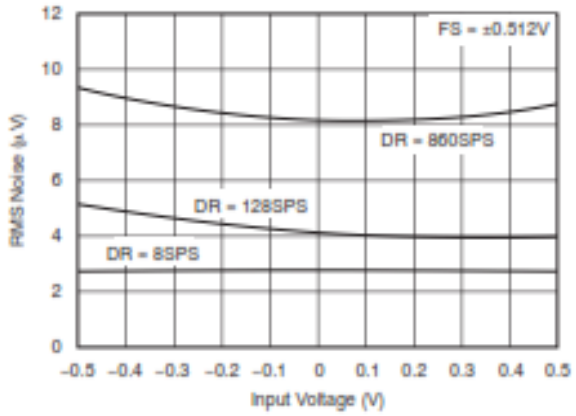


Figure 14.

NOISE vs SUPPLY VOLTAGE

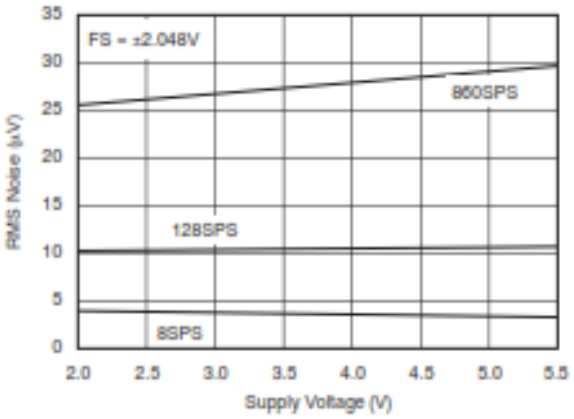


Figure 15.

NOISE vs TEMPERATURE

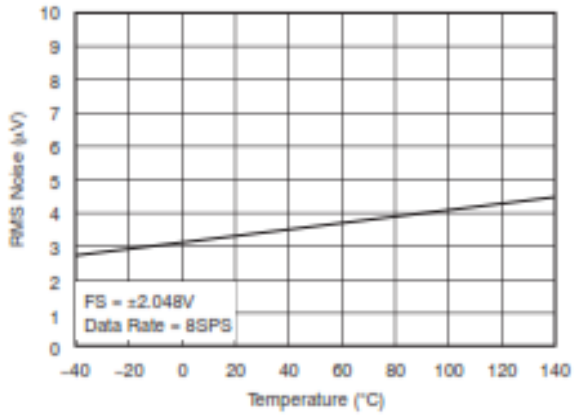


Figure 16.

GAIN ERROR HISTOGRAM

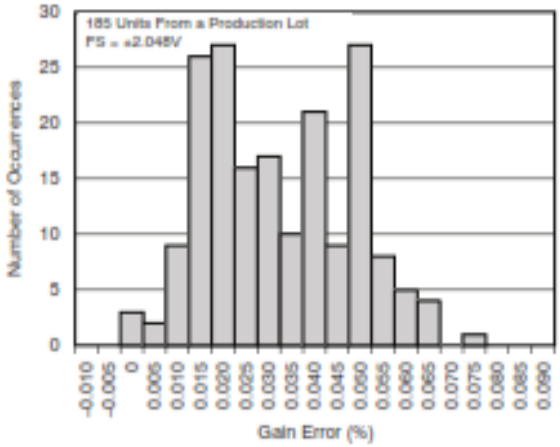


Figure 17.

OFFSET HISTOGRAM

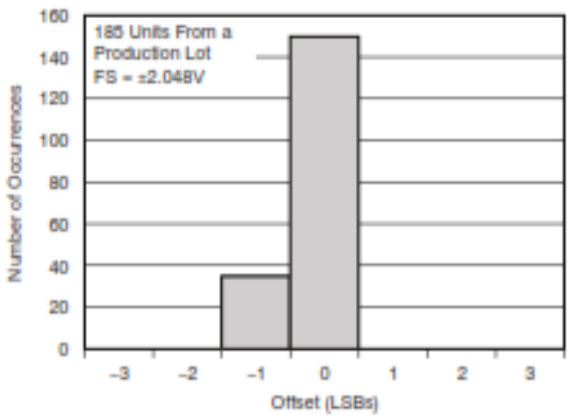


Figure 18.

TOTAL ERROR vs INPUT SIGNAL

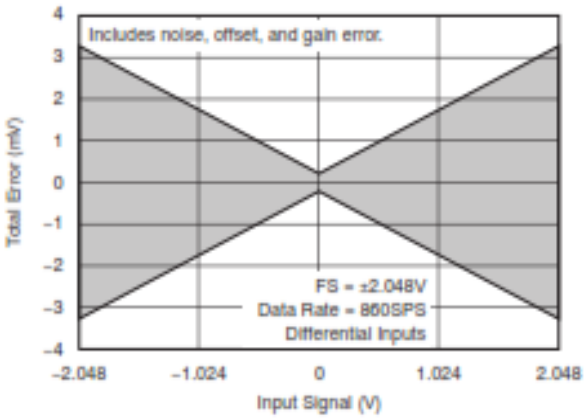


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

DATA RATE vs TEMPERATURE

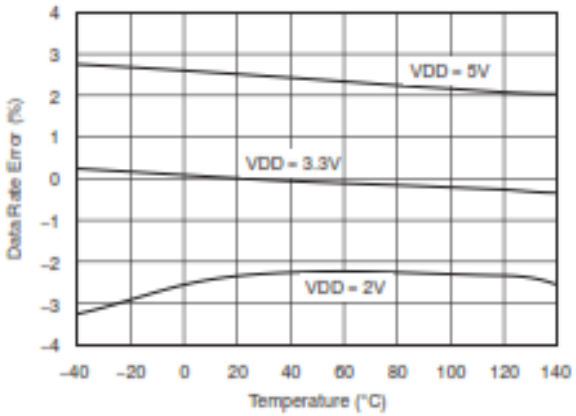


Figure 20.

FREQUENCY RESPONSE

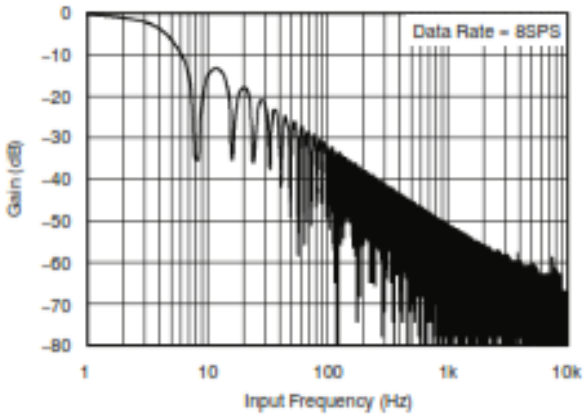


Figure 21.

OVERVIEW

The ADS1113/4/5 are very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS1113/4/5 are extremely easy to configure and design into a wide variety of applications, and allow precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1113/4/5 family to be intuitive and problem-free.

The ADS1113/4/5 consist of a ΔΣ analog-to-digital (A/D) core with adjustable gain (excludes the ADS1113), an internal voltage reference, a clock oscillator, and an I^2C interface. An additional feature available on the ADS1114/5 is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance. Figure 22 shows the ADS1115 functional block diagram.

The ADS1113/4/5 A/D core measures a differential signal, V_{IN}, that is the difference of AIN_P and AIN_N. A MUX is available on the ADS1115. This architecture results in a very strong attenuation in any common-mode signals. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1113/4/5 have two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

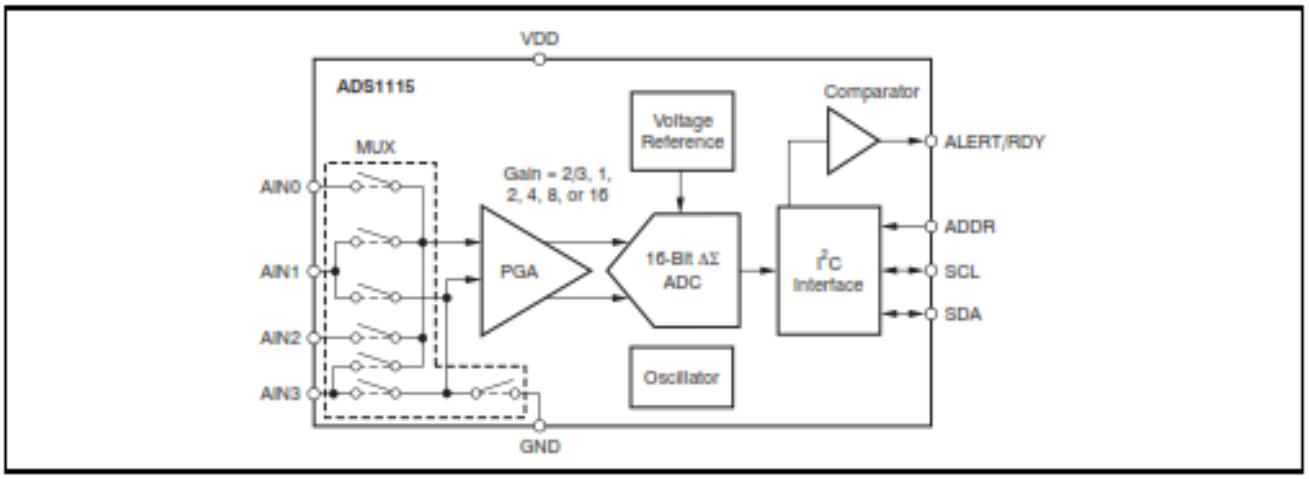


Figure 22. ADS1115 Functional Block Diagram

QUICKSTART GUIDE

This section provides a brief example of ADS1113/4/5 communications. Refer to subsequent sections of this data sheet for more detailed explanations. Hardware for this design includes: one ADS1113/4/5 configured with an I²C address of 1001000; a microcontroller with an I²C interface (TI recommends the MSP430F2002); discrete components such as resistors, capacitors, and serial connectors; and a 2V to 5V power supply. Figure 23 shows the basic hardware configuration.

The ADS1113/4/5 communicate with the master (microcontroller) through an I²C interface. The master provides a clock signal on the SCL pin and data are transferred via the SDA pin. The ADS1113/4/5 never drive the SCL pin. For information on programming and debugging the microcontroller being used, refer to the device-specific product data sheet.

The first byte sent by the master should be the ADS1113/4/5 address followed by a bit that instructs the ADS1113/4/5 to listen for a subsequent byte. The second byte is the register pointer. Refer to Table 9 for a register map. The third and fourth bytes sent from the master are written to the register indicated in the second byte. Refer to Figure 30 and Figure 31 for read and write operation timing diagrams, respectively. All read and write transactions with the ADS1113/4/5 must be preceded by a start condition and followed by a stop condition.

For example, to write to the configuration register to set the ADS1113/4/5 to continuous conversion mode and then read the conversion result, send the following bytes in this order:

Write to Config register:

First byte: 0b10010000 (first 7-bit I²C address followed by a low read/write bit)

Second byte: 0b00000001 (points to Config register)

Third byte: 0b10000100 (MSB of the Config register to be written)

Fourth byte: 0b10000011 (LSB of the Config register to be written)

Write to Pointer register:

First byte: 0b10010000 (first 7-bit I²C address followed by a low read/write bit)

Second byte: 0b00000000 (points to Conversion register)

Read Conversion register:

First byte: 0b10010001 (first 7-bit I²C address followed by a high read/write bit)

Second byte: the ADS1113/4/5 response with the MSB of the Conversion register

Third byte: the ADS1113/4/5 response with the LSB of the Conversion register

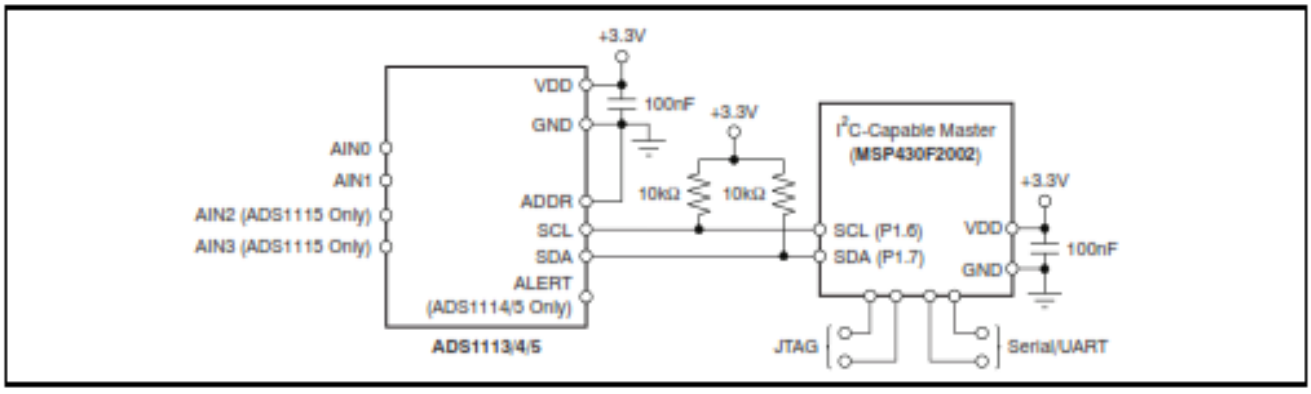


Figure 23. Basic Hardware Configuration

MULTIPLEXER

The ADS1115 contains an input multiplexer, as shown in Figure 24 . Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by three bits in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

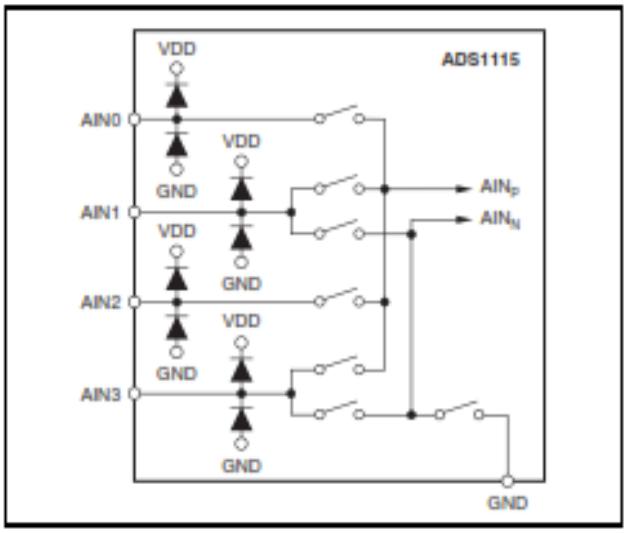


Figure 24. ADS1115 MUX

The ADS1113 and ADS1114 do not have a multiplexer. Either one differential or one single-ended signal may be measured with these devices. For single-ended measurements, connect the AIN1 pin to GND. Note that in subsequent sections of this data sheet, AIN_P refers to AIN0 and AIN_N refers to AIN1 for the ADS1113 and ADS1114.

When measuring single-ended inputs it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals such as $(AIN_P - AIN_N) < 0$. ESD diodes to VDD and GND protect the inputs on all three devices (ADS1113, ADS1114, and ADS1115). To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the following range:

$GND - 0.3V < AINx < VDD + 0.3V$

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Also, overdriving one unused input on the ADS1115 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, again it is recommended to clamp the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1113/4/5 use a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The capacitors used are small, and to external circuitry the average loading appears resistive. This structure is shown in Figure 26 . The resistance is set by the capacitor values and the rate at which they are switched. Figure 25 shows the on/off setting of the switches illustrated in Figure 26 . During the sampling phase, S_1 switches are closed. This event charges C_{A1} to AIN_P, C_{A2} to AIN_N, and C_B to $(AIN_P - AIN_N)$. During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7V and C_B discharges to 0V. This charging draws a very small transient current from the source driving the ADS1113/4/5 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}) where $R_{eff} = V_{IN}/I_{AVERAGE}$.

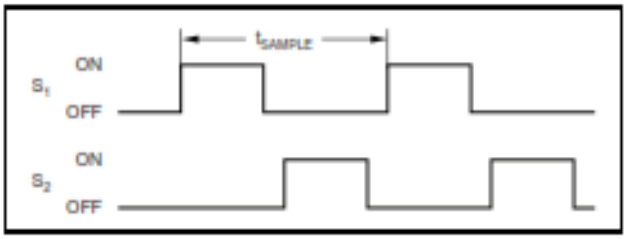


Figure 25. S_1 and S_2 Switch Timing for Figure 26

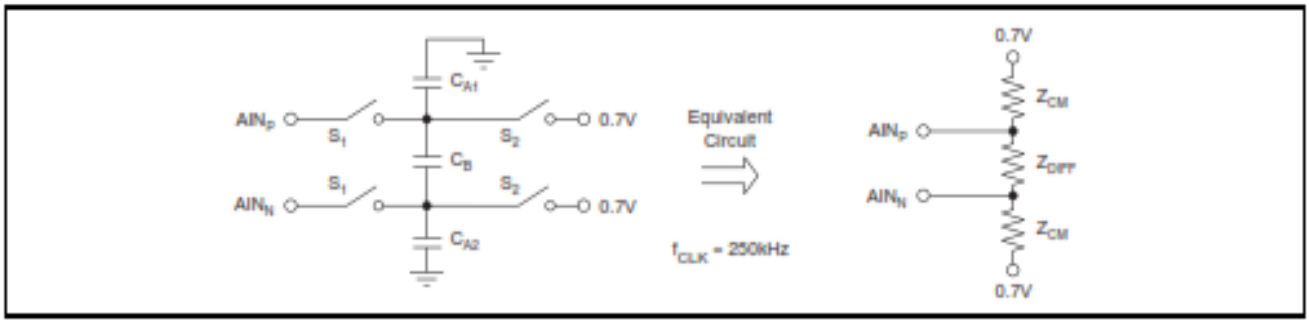


Figure 26. Simplified Analog Input Circuit

The common-mode input impedance is measured by applying a common-mode signal to shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6MΩ for the default PGA gain setting. In Figure 26 , the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the PGA gain setting. In Figure 26 , the differential input impedance is Z_{DIFF}. Table 2 describes the typical differential input impedance.

Table 2. Differential Input Impedance

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
±6.144V(1)	22MΩ
±4.096V(1)	15MΩ
±2.048V	4.9MΩ
±1.024V	2.4MΩ
±0.512V	710kΩ
±0.256V	710kΩ

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1113/4/5 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 2 for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the ΔΣ core of the ADS1114/5. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 3 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The ADS1113 has a fixed full-scale input range of ±2.048V. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4V. Note though that in this case (as well as for PGA = 1 and VDD < 4V), it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table.

Table 3. PGA Gain Full-Scale Range

PGA SETTING	FS (V)
2/3	±6.144V(1)
1	±4.096V(1)
2	±2.048V
4	±1.024V
8	±0.512V
16	±0.256V

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

DATA FORMAT

The ADS1113/4/5 provide 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 4 summarizes the ideal output codes for different input signals. Figure 27 shows code transitions versus input voltage.

Table 4. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ FS $(2^{15} - 1)/2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0
$-FS/2^{15}$	FFFFh
≤ –FS	8000h

1. Excludes the effects of noise, INL, offset, and gain errors.

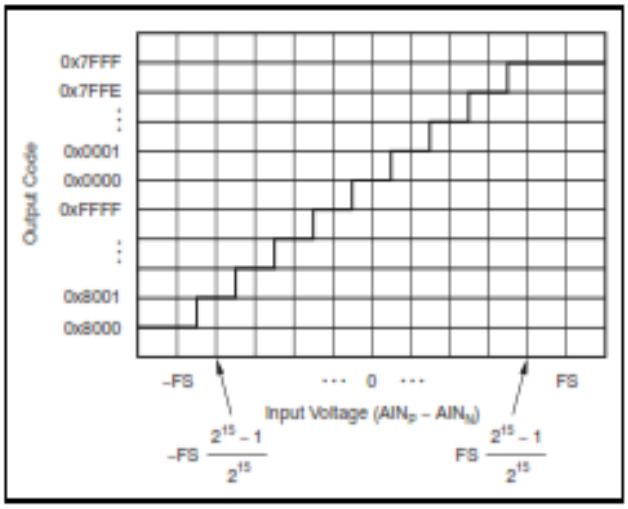


Figure 27. ADS1113/4/5 Code Transition Diagram

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1113/4/5 digital filter provides some attenuation of high-frequency noise, but the digital Sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1113/4/5.

OPERATING MODES

The ADS1113/4/5 operate in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1113/4/5 continuously perform conversions. Once a conversion has been completed, the ADS1113/4/5 place the result in the Conversion register and immediately begins another conversion. In single-shot mode, the ADS1113/4/5 wait until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

RESET AND POWER-UP

When the ADS1113/4/5 powers up, a reset is performed. As part of the reset process, the ADS1113/4/5 set all of the bits in the Config register to the respective default settings.

The ADS1113/4/5 respond to the I^2C general call reset command. When the ADS1113/4/5 receive a general call reset, an internal reset is performed as if the device had been powered on.

DUTY CYCLING FOR LOW POWER

For many applications, the improved performance at low data rates may not be required. For these applications, the ADS1113/4/5 support duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1113/4/5 in power-down mode with a data rate set to 860SPS could be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 860SPS only requires about 1.2ms, the ADS1113/4/5 enter power-down mode for the remaining 123.8ms. In this configuration, the ADS1113/4/5 consume about 1/100th the power of the ADS1113/4/5 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The ADS1113/4/5 offer lower data rates that do not implement duty cycling and offer improved noise performance if it is needed.

COMPARATOR (ADS1114/15 ONLY)

The ADS1114/5 are each equipped with a customizable comparator that can issue an alert on the ALERT/RDY pin. This feature can significantly reduce external circuitry for many applications. The comparator can be implemented as either a traditional comparator or a window comparator via the COMP_MODE bit in the Config register. When implemented as a traditional comparator, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the high threshold register. The comparator then deasserts when the input signal falls below the low threshold register value. In window comparator mode, the ALERT/RDY pin asserts if conversion data exceed the high threshold register or fall below the low threshold register.

In either window or traditional comparator mode, the comparator can be configured to latch once asserted by the COMP_LAT bit in the Config register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can be cleared by issuing an SMBus alert response or by reading the Conversion register. The COMP_POL bit in the Config register configures the ALERT/RDY pin as active high or active low. Operational diagrams for the comparator modes are shown in Figure 28 and Figure 29 .

The comparator can be configured to activate the ALERT/RDY pin after a set number of successive readings exceed the threshold. The comparator can be configured to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin by changing the COMP_QUE bits in the Config register. The COMP_QUE bits can also disable the comparator function.

CONVERSION READY PIN (ADS1114/5 ONLY)

The ALERT/RDY pin can also be configured as a conversion ready pin. This mode of operation can be realized if the MSB of the high threshold register is set to '1' and the MSB of the low threshold register is set to '0'. The COMP_POL bit continues to function and the COMP_QUE bits can disable the pin; however, the COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion ready pin, ALERT/RDY continues to require a pull-up resistor. When in continuous conversion mode, the ADS1113/4/5 provide a brief (~8µs) pulse on the ALERT/RDY pin at the end of each conversion. When in single-shot shutdown mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to '0'.

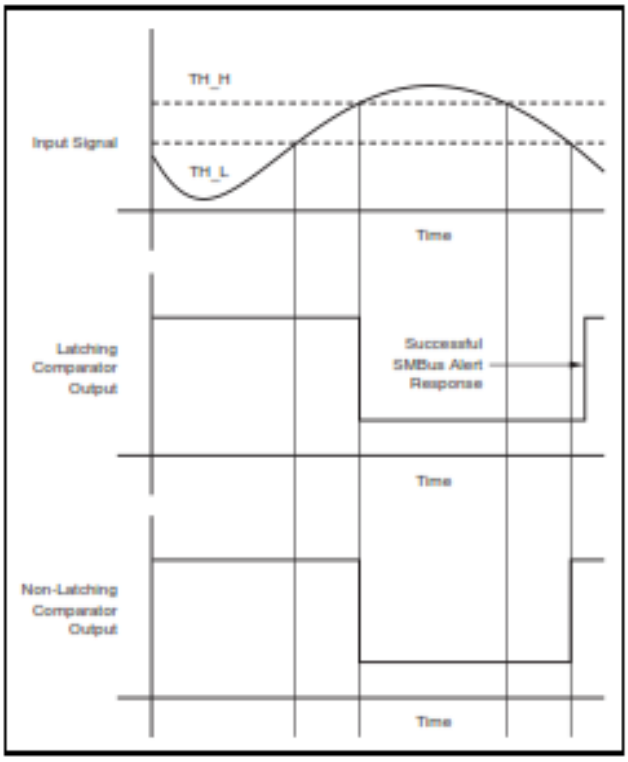


Figure 28. Alert Pin Timing Diagram When Configured as a Traditional Comparator

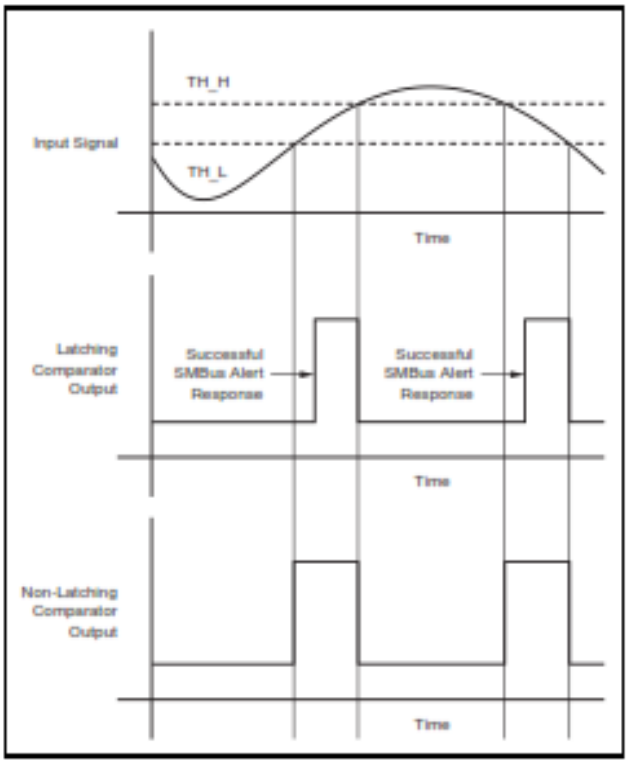


Figure 29. Alert Pin Timing Diagram When Configured as a Window Comparator

SMBus ALERT RESPONSE

When configured in latching mode (COMP_LAT = '1' in the Config register), the ALERT/RDY pin can be implemented with an SMBus alert. The pin asserts if the comparator detects a conversion that exceeds an upper or lower threshold. This interrupt is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I²C address. If conversion data exceed the upper or lower thresholds after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin, as with the SDA pin, is an open-drain pin. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that it does not interfere with other devices on the same bus line.

When the master senses that the ALERT/RDY pin has latched, it issues an SMBus alert command (00011001) to the I²C bus. Any ADS1114/5 data converters on the I²C bus with the ALERT/RDY pins asserted respond to the command with the slave address. In the event that two or more ADS1114/5 data converters present on the bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert decides which device clears its assertion. The device with the lowest I²C address always wins arbitration. If a device loses arbitration, it does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have had the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a '1' if signals exceed the high threshold and a '0' if signals exceed the low threshold.

I²C INTERFACE

The ADS1113/4/5 communicate through an I²C interface. I²C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the ADS1113/4/5 can only act as slave devices.

An I²C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I²C bus in groups of eight bits. To send a bit on the I²C bus, the SDA line is driven to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). Once the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I²C bus is held idle for more than 25ms, the bus times out.

The I²C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1113/4/5 never drive SCL, because they cannot act as a master. On the ADS1113/4/5, SCL is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the *address byte*. Each device on an I²C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I²C bus, whether it is address or data, is acknowledged with an *acknowledge* bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls SDA low to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

See the *Timing Requirements* section for a timing diagram showing the ADS1113/4/5 I²C transaction.

I²C ADDRESS SELECTION

The ADS1113/4/5 have one address pin, ADDR, that sets the I²C address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 5 . The state of the address pin ADDR is sampled continuously.

Table 5. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN	SLAVE ADDRESS
Ground	1001000
VDD	1001001
SDA	1001010
SCL	1001011

I²C GENERAL CALL

The ADS1113/4/5 respond to the I²C general call address (0000000) if the eighth bit is '0'. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the ADS1113/4/5 reset the internal registers and enter power-down mode.

I²C SPEED MODES

The I²C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called Hs mode) allows a clock frequency of up to 3.4MHz. The ADS1113/4/5 are fully compatible with all three modes.

No special action is required to use the ADS1113/4/5 in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of *00001xxx* following the START condition, where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes; the eighth bit does not indicate read/write status.) The ADS1113/4/5 do not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. Upon receiving a master code, the ADS1113/4/5 switch on Hs mode filters, and communicate at up to 3.4MHz. The ADS1113/4/5 switch out of Hs mode with the next STOP condition.

For more information on high-speed mode, consult the I²C specification.

SLAVE MODE OPERATIONS

The ADS1113/4/5 can act as either slave receivers or slave transmitters. As a slave device, the ADS1113/4/5 cannot drive the SCL line.

Receive Mode:

In slave receive mode the first byte transmitted from the master to the slave is the address with the R/$\overline{W}$ bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the register pointer byte. The ADS1113/4/5 then acknowledge receipt of the register pointer byte. The next two bytes are written to the address given by the register pointer. The ADS1113/4/5 acknowledge each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

Transmit Mode:

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/$\overline{W}$ bit. This byte places the slave into transmit mode and indicates that the ADS1113/4/5 are being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register pointer. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

WRITING/READING THE REGISTERS

To access a specific register from the ADS1113/4/5, the master must first write an appropriate value to the Pointer register. The Pointer register is written directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. After the Pointer register is written, the slave acknowledges and the master issues a STOP or a repeated START condition.

When reading from the ADS1113/4/5, the previous value written to the Pointer register determines the register that is read from. To change which register is read, a new value must be written to the Pointer register. To write a new value to the Pointer register, the master issues a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data need to be transmitted, and a STOP condition can be issued by the master. The master may now issue a START condition and send the slave address byte with the R/$\overline{W}$ bit high to begin the read. Table 10 details this sequence. If repeated reads from the same register are desired, there is no need to continually send Pointer register bytes, because the ADS1113/4/5 store the value of the Pointer register until it is modified by a write operation. However, every write operation requires the Pointer register to be written.

REGISTERS

The ADS1113/4/5 have four registers that are accessible via the I^2C port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1113/4/5 operating modes and query the status of the devices. Two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

POINTER REGISTER

The four registers are accessed by writing to the Pointer register byte; see Figure 30 . Table 6 and Table 7 indicate the Pointer register byte map.

Table 6. Register Address

BIT 1	BIT 0	REGISTER
0	0	Conversion register
0	1	Config register
1	0	Lo_thresh register
1	1	Hi_thresh register

CONVERSION REGISTER

The 16-bit register contains the result of the last conversion in binary twos complement format. Following reset or power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is completed.

The register format is shown in Table 8 .

CONFIG REGISTER

The 16-bit register can be used to control the ADS1113/4/5 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in Table 9 .

Table 7. Pointer Register Byte (Write-Only)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	Register address	

Table 8. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 9. Config Register (Read/Write)

BIT	15	14	13	12	11	10	9	8
NAME	OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
BIT	7	6	5	4	3	2	1	0
NAME	DR2	DR1	DR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0

Default = 8583h.

Bit [15] **OS: Operational status/single-shot conversion start**

This bit determines the operational status of the device.
This bit can only be written when in power-down mode.

For a write status:
0 : No effect
1 : Begin a single conversion (when in power-down mode)
For a read status:
0 : Device is currently performing a conversion
1 : Device is not currently performing a conversion

Bits [14:12] **MUX[2:0]: Input multiplexer configuration (ADS1115 only)**

These bits configure the input multiplexer. They serve no function on the ADS1113/4.

000 : AIN_P = AIN0 and AIN_N = AIN1 (default)	100 : AIN_P = AIN0 and AIN_N = GND
001 : AIN_P = AIN0 and AIN_N = AIN3	101 : AIN_P = AIN1 and AIN_N = GND
010 : AIN_P = AIN1 and AIN_N = AIN3	110 : AIN_P = AIN2 and AIN_N = GND
011 : AIN_P = AIN2 and AIN_N = AIN3	111 : AIN_P = AIN3 and AIN_N = GND

Bits [11:9] **PGA[2:0]: Programmable gain amplifier configuration (ADS1114 and ADS1115 only)**

These bits configure the programmable gain amplifier. They serve no function on the ADS1113.

000 : FS = ±6.144V (1)	100 : FS = ±0.512V
001 : FS = ±4.096V (1)	101 : FS = ±0.256V
010 : FS = ±2.048V (default)	110 : FS = ±0.256V
011 : FS = ±1.024V	111 : FS = ±0.256V

Bit [8] **MODE: Device operating mode**

This bit controls the current operational mode of the ADS1113/4/5.
0 : Continuous conversion mode
1 : Power-down single-shot mode (default)

Bits [7:5] **DR[2:0]: Data rate**

These bits control the data rate setting.

000 : 8SPS	100 : 128SPS (default)
001 : 16SPS	101 : 250SPS
010 : 32SPS	110 : 475SPS
011 : 64SPS	111 : 860SPS

Bit [4] **COMP_MODE: Comparator mode (ADS1114 and ADS1115 only)**

This bit controls the comparator mode of operation. It changes whether the comparator is implemented as a traditional comparator (COMP_MODE = '0') or as a window comparator (COMP_MODE = '1'). It serves no function on the ADS1113.
0 : Traditional comparator with hysteresis (default)
1 : Window comparator

Bit [3] **COMP_POL: Comparator polarity (ADS1114 and ADS1115 only)**

This bit controls the polarity of the ALERT/RDY pin. When COMP_POL = '0' the comparator output is active low. When COMP_POL='1' the ALERT/RDY pin is active high. It serves no function on the ADS1113.
0 : Active low (default)
1 : Active high

Bit [2] **COMP_LAT: Latching comparator (ADS1114 and ADS1115 only)**

This bit controls whether the ALERT/RDY pin latches once asserted or clears once conversions are within the margin of the upper and lower threshold values. When COMP_LAT = '0', the ALERT/RDY pin does not latch when asserted. When COMP_LAT = '1', the asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master, the device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line. This bit serves no function on the ADS1113.
0 : Non-latching comparator (default)
1 : Latching comparator

Bits [1:0] **COMP_QUE: Comparator queue and disable (ADS1114 and ADS1115 only)**

These bits perform two functions. When set to '11', they disable the comparator function and put the ALERT/RDY pin into a high state. When set to any other value, they control the number of successive conversions exceeding the upper or lower thresholds required before asserting the ALERT/RDY pin. They serve no function on the ADS1113.
00 : Assert after one conversion
01 : Assert after two conversions
10 : Assert after four conversions
11 : Disable comparator (default)

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Lo_thresh AND Hi_thresh REGISTERS

The upper and lower threshold values used by the comparator are stored in two 16-bit registers. These registers store values in the same format that the output register displays values; that is, they are stored in twos complement format. Because it is implemented as a digital comparator, special attention should be taken to readjust values whenever PGA settings are changed.

A secondary conversion ready function of the comparator output pin can be realized by setting the Hi_thresh register MSB to '1' and the Lo_thresh register MSB to '0'. However, in all other cases, the Hi_thresh register must be larger than the Lo_thresh register. The threshold register formats are shown in Table 10 . When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode and pulses when in continuous conversion mode.

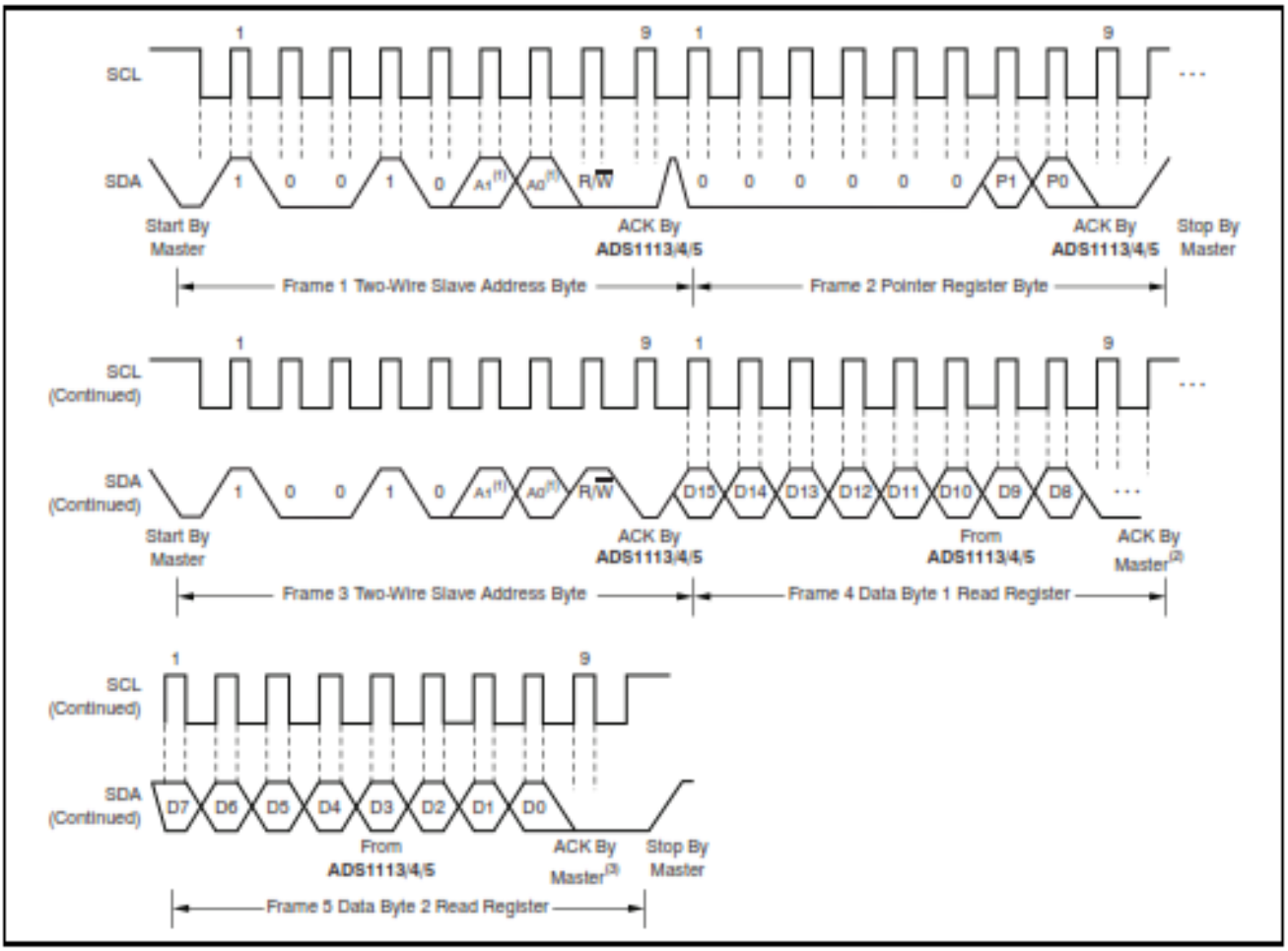
Table 10. Lo_thresh and Hi_thresh Registers

REGISTER	Lo_thresh (Read/Write)							
BIT	15	14	13	12	11	10	9	8
NAME	Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
BIT	7	6	5	4	3	2	1	0
NAME	Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0

REGISTER	Hi_thresh (Read/Write)							
BIT	15	14	13	12	11	10	9	8
NAME	Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
BIT	7	6	5	4	3	2	1	0
NAME	Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0

Lo_thresh default = 8000h.

Hi_thresh default = 7FFFh.

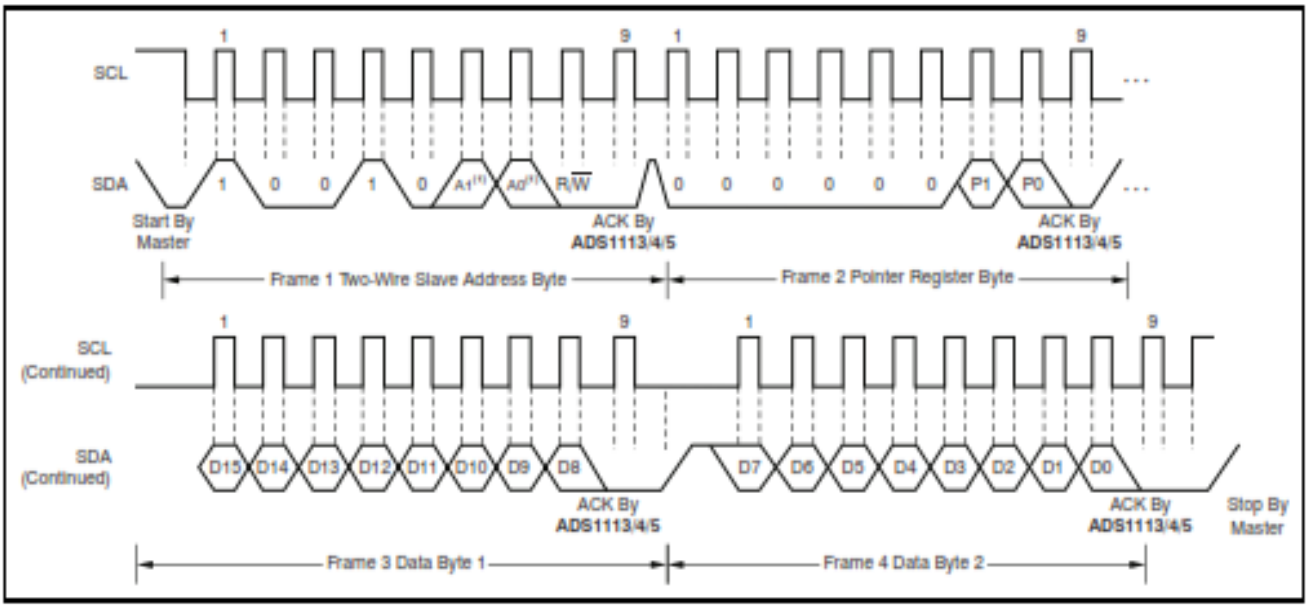


(1) The values of A0 and A1 are determined by the ADDR pin.

(2) Master can leave SDA high to terminate a single-byte read operation.

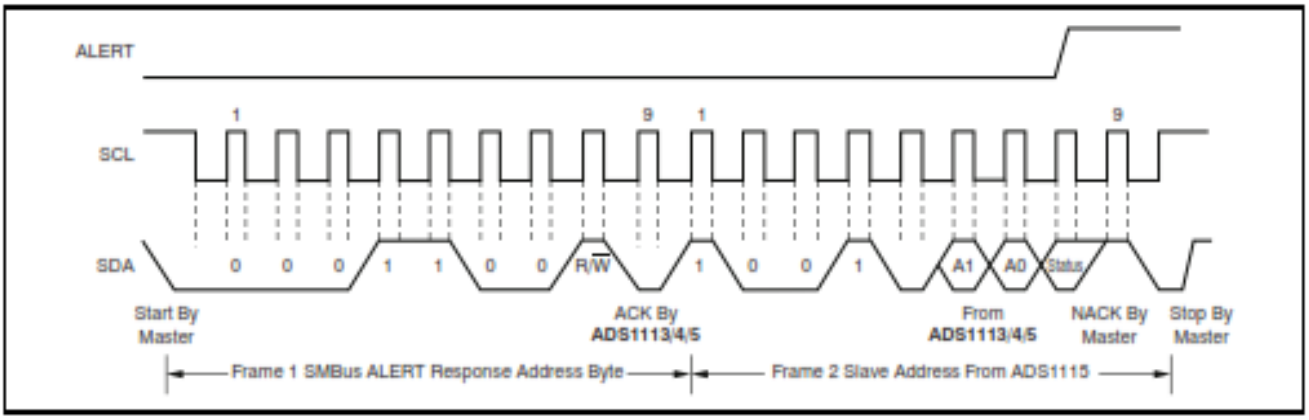
(3) Master can leave SDA high to terminate a two-byte read operation.

Figure 30. Two-Wire Timing Diagram for Read Word Format



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 31. Two-Wire Timing Diagram for Write Word Format



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 32. Timing Diagram for SMBus ALERT Response

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1113/4/5 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1113/4/5 is simple. A basic connection diagram for the ADS1115 is shown in Figure 33 .

The fully differential voltage input of the ADS1113/4/5 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1113/4/5 can read bipolar differential signals, they cannot accept negative voltages on either input. It may be helpful to think of the ADS1113/4/5 positive voltage input as *noninverting*, and of the negative input as *inverting*.

When the ADS1113/4/5 are converting data, they draw current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1113/4/5 interface directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, can operate with the ADS1113/4/5. The ADS1113/4/5 do not perform clock-stretching (that is, they never pull the clock line low), so it is not necessary to provide for this function unless other clock-stretching devices are on the same I^2C bus.

Pull-up resistors are required on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

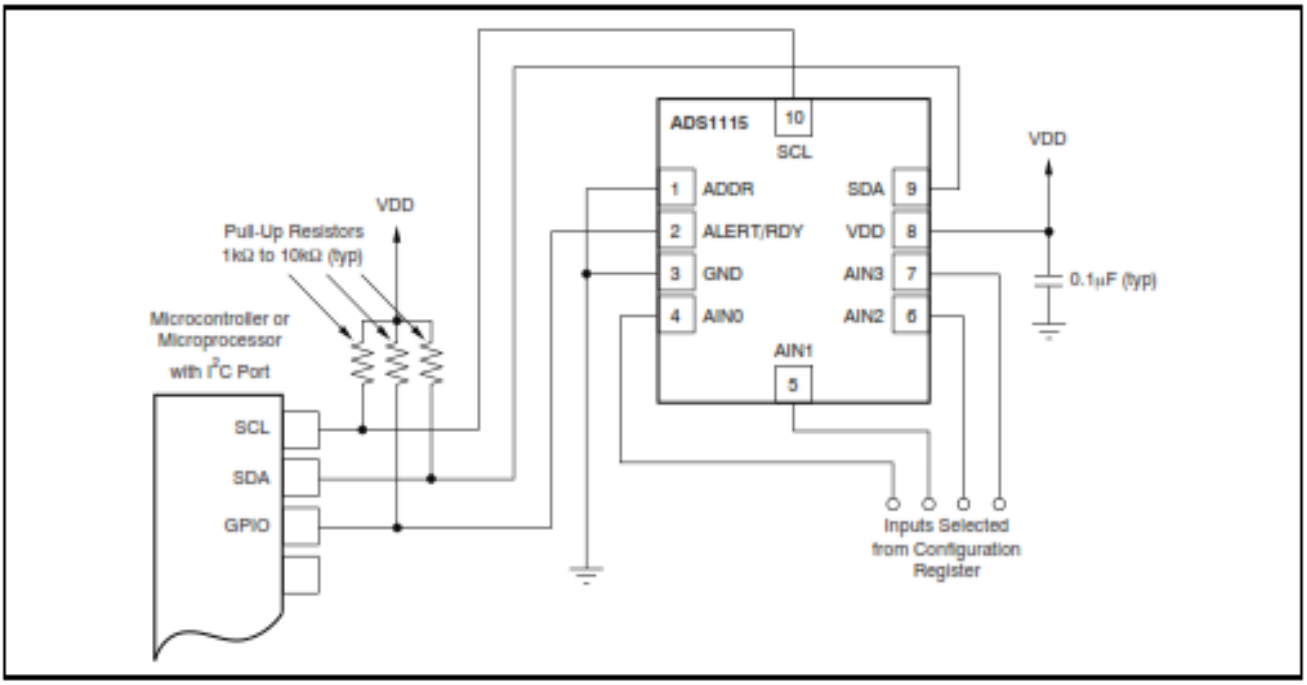


Figure 33. Typical Connections of the ADS1115

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1113/4/5s to a single bus is simple. Using the address pin, the ADS1113/4/5 can be set to one of four different I²C addresses. An example showing three ADS1113/4/5 devices is given in Figure 35 . Up to four ADS1113/4/5s (using different address pin configurations) can be connected to a single bus.

Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

The TMP421 and DAC8574 devices detect the respective I²C bus addresses based on the states of pins. In the example, the TMP421 has the address 0101010, and the DAC8574 has the address 1001100. Consult the DAC8574 and TMP421 data sheets, available at www.ti.com, for further details.

USING GPIO PORTS FOR COMMUNICATION

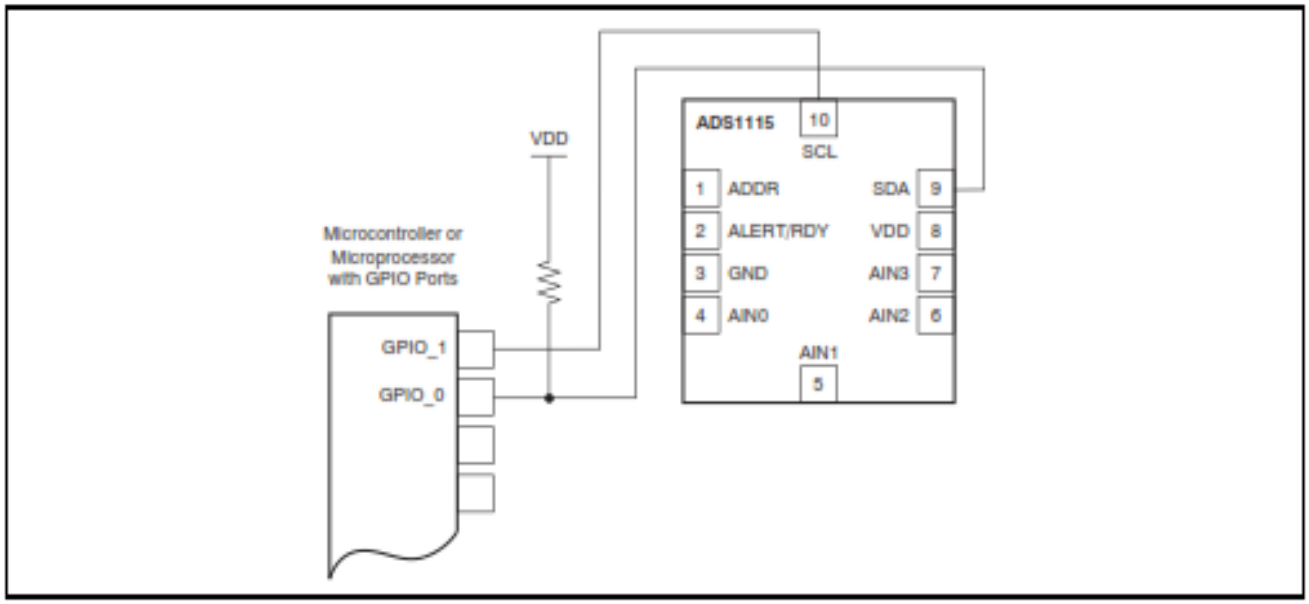
Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1113/4/5 can be connected to GPIO pins and the I²C bus protocol simulated, or *bit-banged*, in software. An example of this configuration for a single ADS1113/4/5 is shown in Figure 34 .

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to '0' and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this configuration reads as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. This action is possible because the ADS1113/4/5 never drive the clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption as a result of the absence of a resistive pull-up.

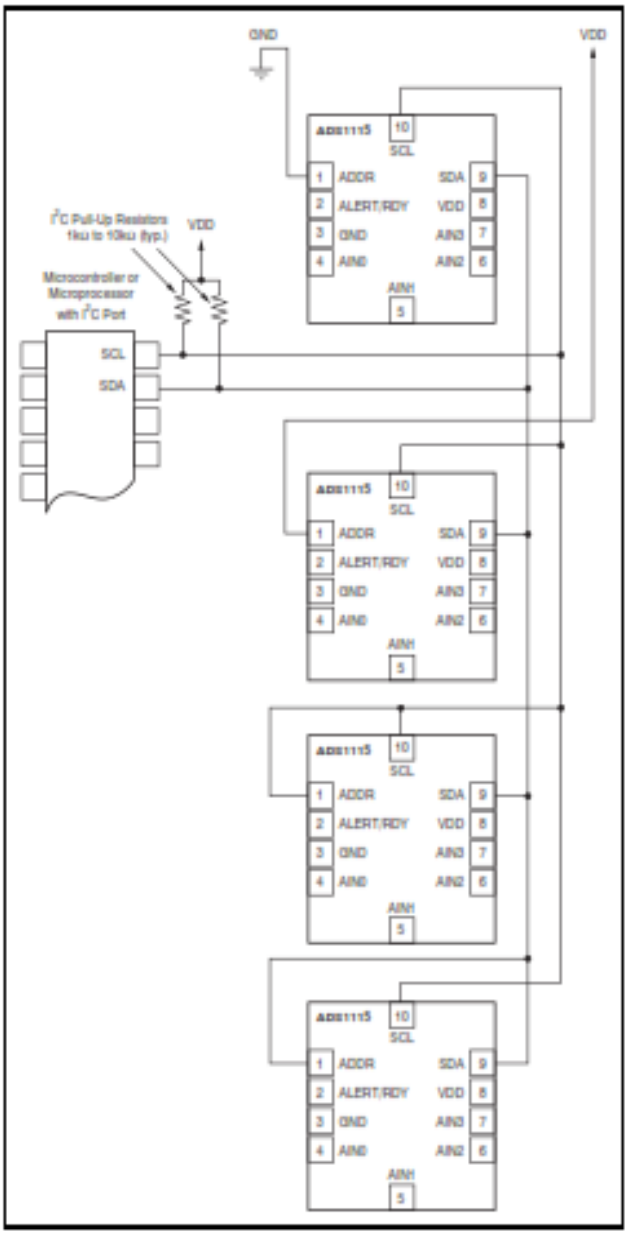
If there are any devices on the bus that may drive the clock lines low, this method should not be used; the SCL line should be high-Z or '0' and a pull-up resistor provided as usual.

Some microcontrollers have selectable strong pull-up circuits built in to the GPIO ports. In some cases, these circuits can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.



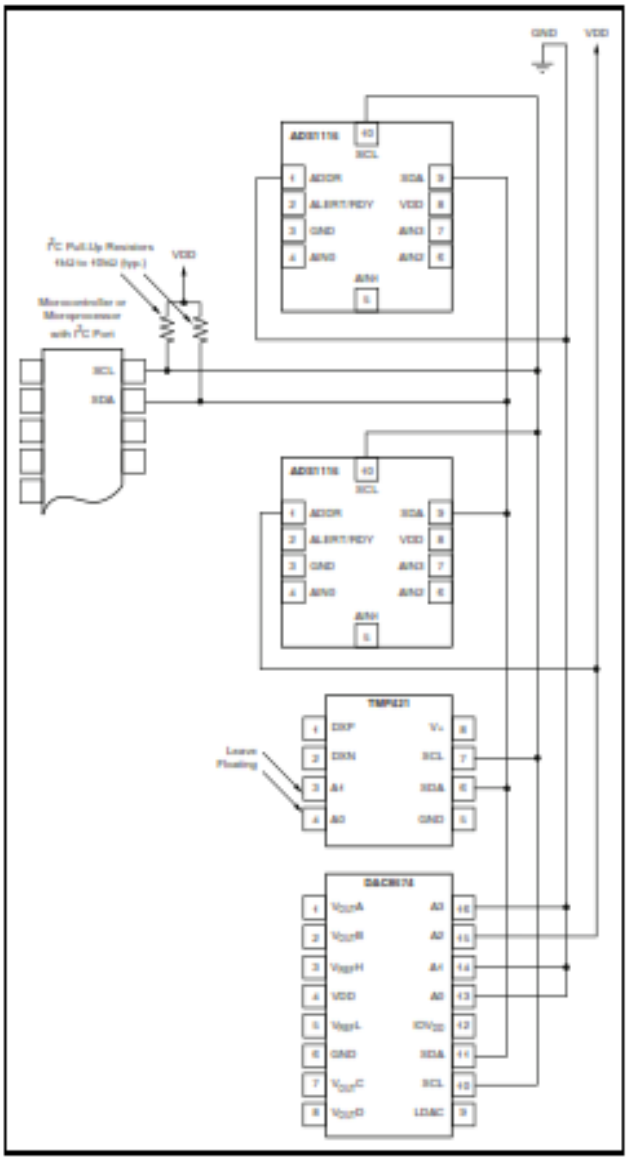
NOTE: ADS1113/4/5 power and input connections omitted for clarity.

Figure 34. Using GPIO with a Single ADS1115



NOTE: ADS1113/4/5 power and input connections omitted for clarity. The ADDR pin selects the I²C address.

Figure 35. Connecting Multiple ADS1113/4/5s



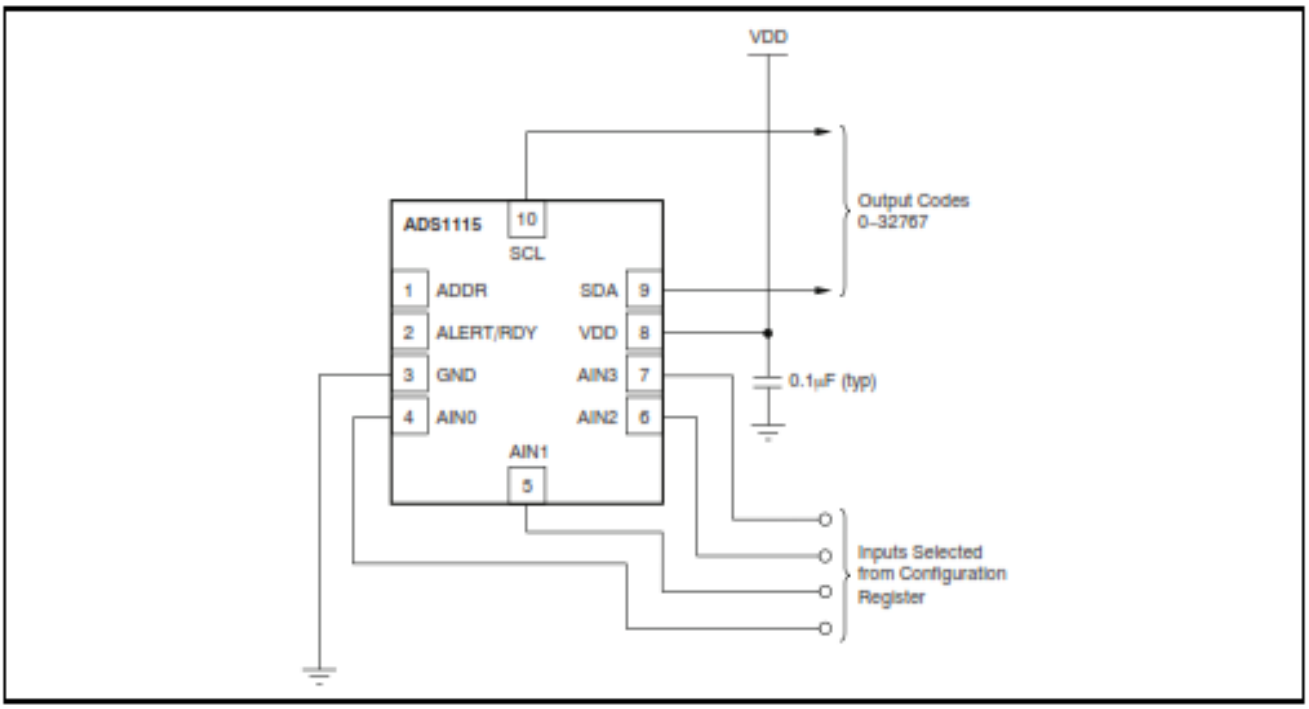
NOTE: ADS1113/4/5 power and input connections omitted for clarity. ADDR, A3, A2, A1, and A0 select the I²C addresses.

Figure 36. Connecting Multiple Device Types

SINGLE-ENDED INPUTS

Although the ADS1115 has two differential inputs, the device can easily measure four single-ended signals. Figure 37 shows a single-ended connection scheme. The ADS1115 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0V to supply. The ADS1115 loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1115 can only accept positive voltages.

The ADS1115 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 37 covers only half the ADS1115 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.



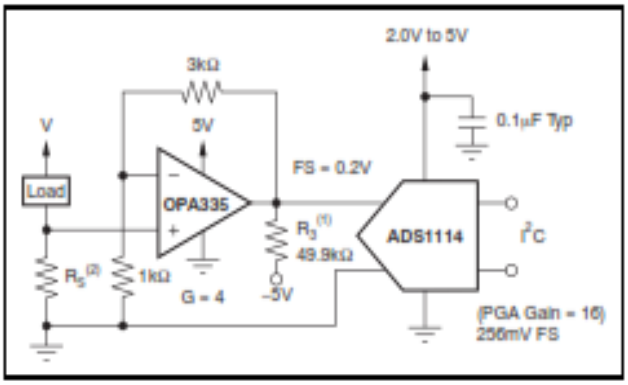
NOTE: Digital and address pin connections omitted for clarity.

Figure 37. Measuring Single-Ended Inputs

LOW-SIDE CURRENT MONITOR

Figure 38 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an OPA335 low-drift op amp, and the result is read by the ADS1114/5.

It is suggested that the ADS1114/5 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 16, the op amp should be set up to give a maximum output voltage no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1114/5 is 0.2V.



(1) Pull-down resistor to allow accurate swing to 0V.

(2) R_S is sized for a 50mV drop at full-scale current.

Figure 38. Low-Side Current Measurement

The ADS1113/4/5 are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1113/4/5 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1113/4/5 analog inputs can withstand momentary currents as large as 100mA.

If the ADS1113/4/5 are driven by an op amp with high-voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1113/4/5. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with an ADS1113/4/5, performance characteristics must be taken into account when designing the application.

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS1113IDGSR	PREVIEW	MSOP	DGS	10	2500	TBD	Call TI	Call TI
ADS1113IDGST	PREVIEW	MSOP	DGS	10	250	TBD	Call TI	Call TI
ADS1113IRUGR	PREVIEW	QFN	RUG	10	3000	TBD	Call TI	Call TI
ADS1113IRUGT	PREVIEW	QFN	RUG	10	250	TBD	Call TI	Call TI
ADS1114IDGSR	PREVIEW	MSOP	DGS	10	2500	TBD	Call TI	Call TI
ADS1114IDGST	PREVIEW	MSOP	DGS	10	250	TBD	Call TI	Call TI
ADS1114IRUGR	PREVIEW	QFN	RUG	10	3000	TBD	Call TI	Call TI
ADS1114IRUGT	PREVIEW	QFN	RUG	10	250	TBD	Call TI	Call TI
ADS1115IDGSR	PREVIEW	MSOP	DGS	10	2500	TBD	Call TI	Call TI
ADS1115IDGST	PREVIEW	MSOP	DGS	10	250	TBD	Call TI	Call TI
ADS1115IRUGR	PREVIEW	QFN	RUG	10	3000	TBD	Call TI	Call TI
ADS1115IRUGT	PREVIEW	QFN	RUG	10	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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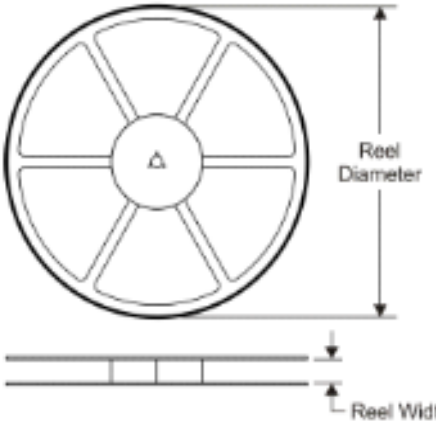
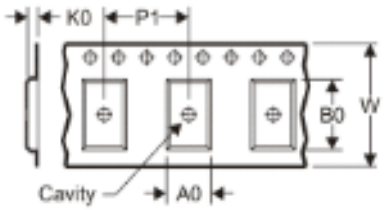
TAPE AND REEL INFORMATION

REEL DIMENSIONS

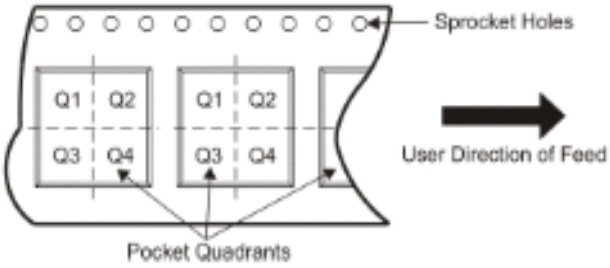


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1113IDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1113IDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1114IDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1114IDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1115IDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1115IDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

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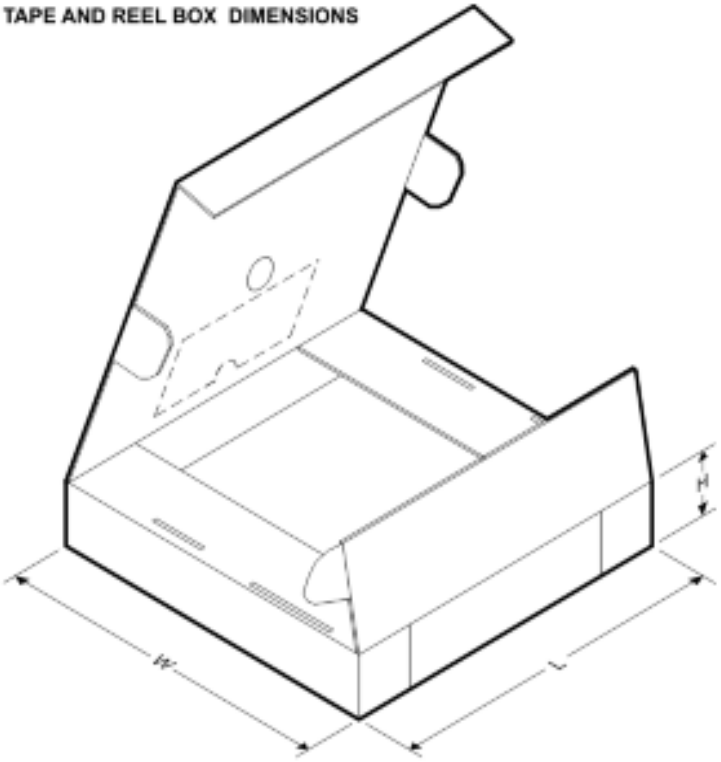
TAPE AND REEL BOX DIMENSIONS

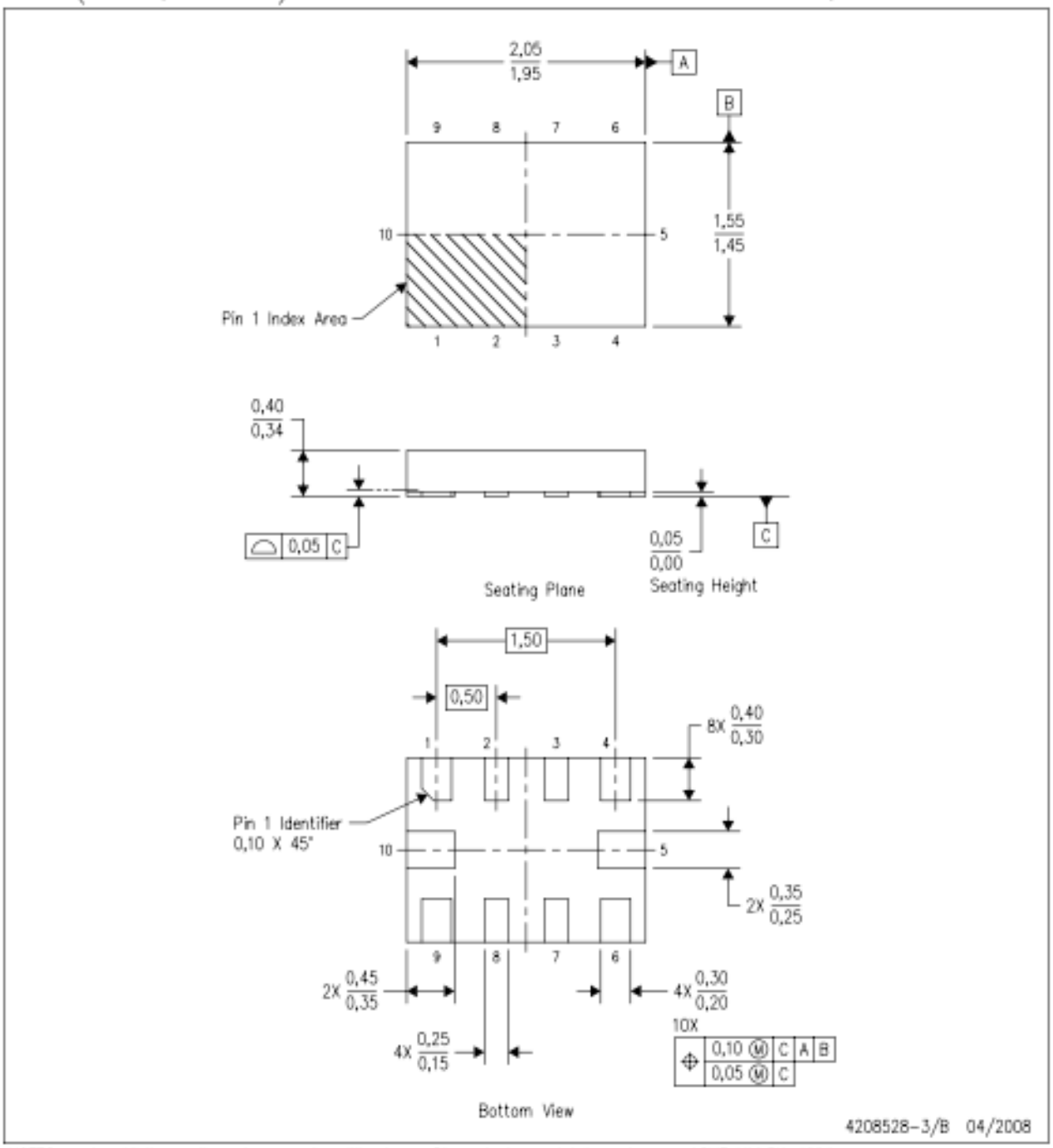


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1113IDGSR	MSOP	DGS	10	2500	370.0	355.0	55.0
ADS1113IDGST	MSOP	DGS	10	250	195.0	200.0	45.0
ADS1114IDGSR	MSOP	DGS	10	2500	370.0	355.0	55.0
ADS1114IDGST	MSOP	DGS	10	250	195.0	200.0	45.0
ADS1115IDGSR	MSOP	DGS	10	2500	370.0	355.0	55.0
ADS1115IDGST	MSOP	DGS	10	250	195.0	200.0	45.0

MECHANICAL DATA

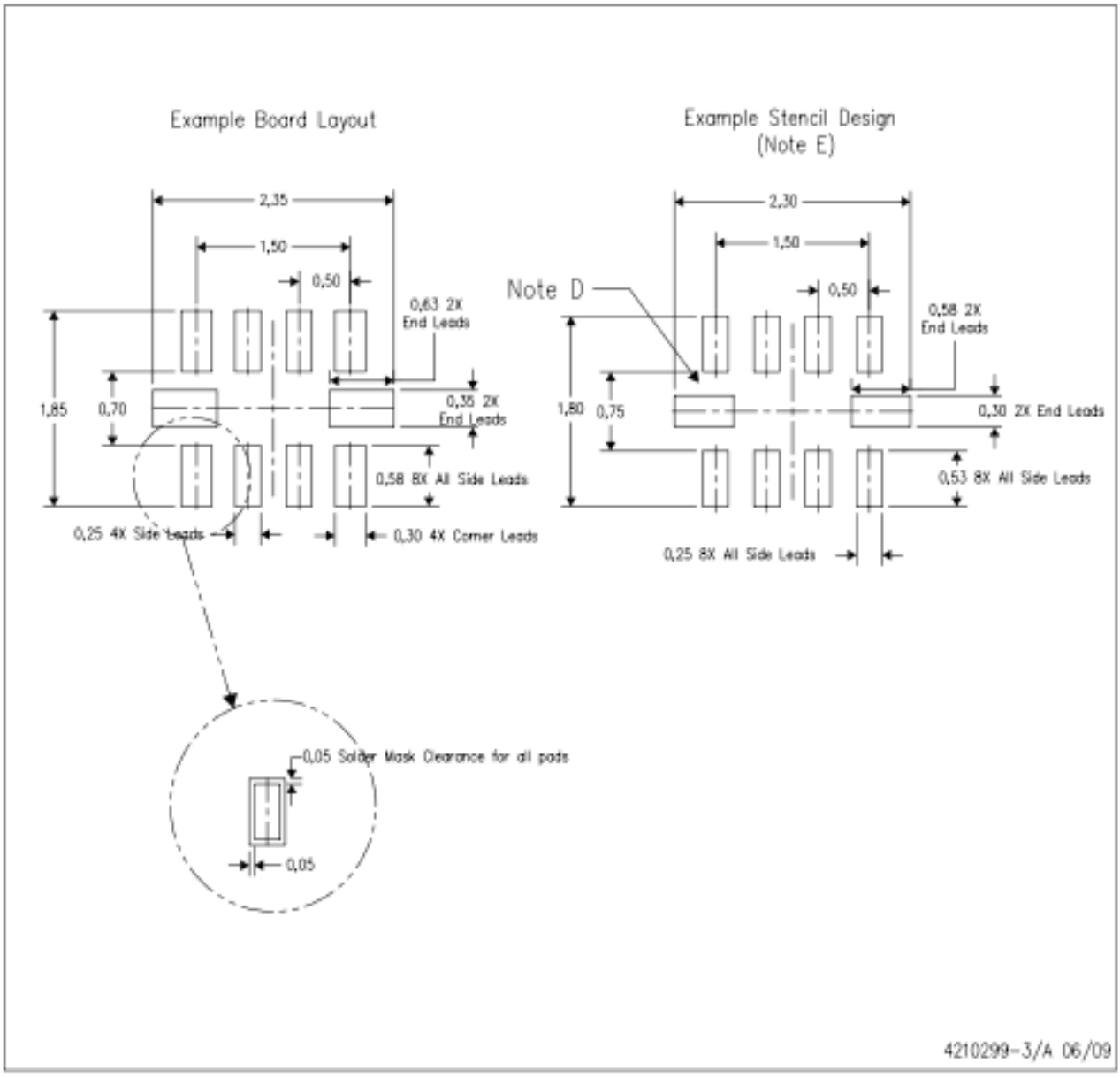
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

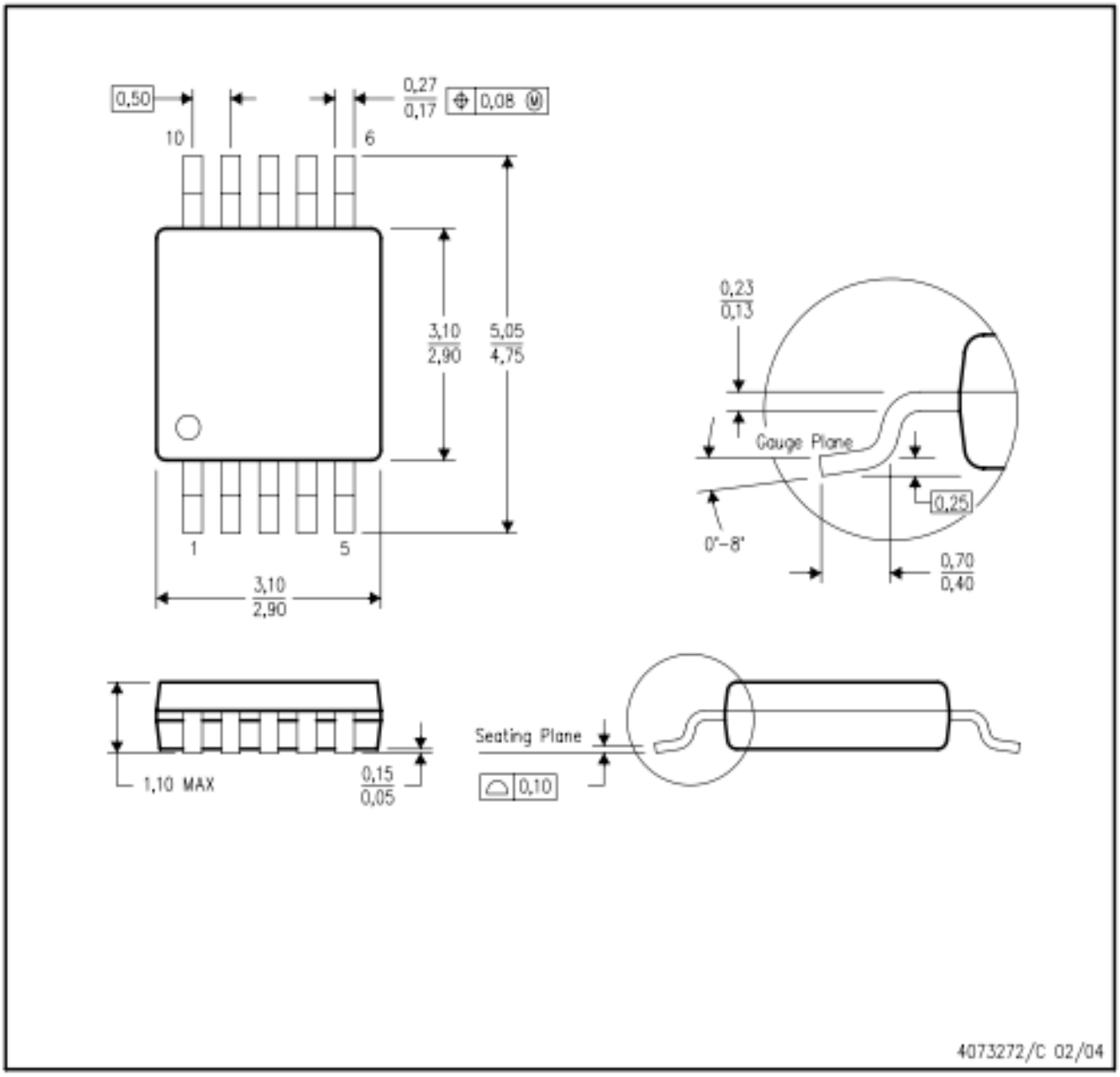
LAND PATTERN

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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