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Modular interface electronic card design for BIMNOV project

Tesis en torno a una hipótesis o problema de investigación y su contrastación

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DEDICATORIA

A mis padres Roberto y Nelly, y a mi hermano Bryan por todo el apoyo durante el transcurso de este posgrado

Oscar Omar

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1. RESUMEN

Cada producto que NOVATEM diseña y construye debe ser sometido a pruebas para asegurar los requerimientos, en este momento, para probar las soluciones desarrolladas, NOVATEM también diseña pequeños prototipos con los cuales se pueden hacer los ensayos. Evidentemente, cada nuevo producto implica obligatoriamente desarrollar la fase de construcción del prototipo para el ensayo lo cual consume recursos y requiere de grandes cantidades de tiempo de diseño.

BIMNOV tiene por objetivo eliminar esta fase, se plantea como una solución modular en la cual el banco de ensayos estará totalmente listo. Para lograr ésta modularidad, una tarjeta madre será concebida como el núcleo central del proyecto donde muchas otras tarjetas electrónicas podrán ser conectadas de acuerdo a los requerimientos del dispositivo bajo prueba.

Es así que BIMNOV contendrá todos los módulos necesarios y arquitecturas para la etapa de pruebas y validación de los principales productos y nuevos desarrollados por NOVATEM. Será suficiente conectar e intercambiar las tarjetas módulo de acuerdo con el tamaño del dispositivo bajo pruebas, en tipo de señales a ser medidas y la información a ser recolectada.

BIMNOV también tiene una visión de escalabilidad en la cuál si una nueva tarjeta modular es desarrollada, esta pasará a formar parte del catálogo disponible y podrá ser utilizada para pruebas futuras.

La principal contribución al proyecto BIMNOV fue desarrollar una solución capaz de identificar las tarjetas módulo que son conectadas en la tarjeta madre, cada tarjeta depende del tipo de dispositivo mecatrónico bajo prueba. Para realizar esta conceptualización se debe identificar los componentes, tipos de señales y protocolos de comunicación que serán utilizados, todo esto se detalla en las siguientes secciones

2. ABSTRACT

Every product that NOVATEM designs, and builds must be tested to ensure the requirements, at this stage, to test the developed solutions NOVATEM uses to also design small prototypes to carry on the essays with. Evidently, each new product implies mandatory the development of this prototype building phase, which consumes resources and demands large amounts of designing time. BINMOV focuses on eliminating this stage, it is proposed as a modular solution where the test bench will be already set. To achieve this modularity a motherboard will be conceived as the heart of the project where several card modules can be plugged in according to the requirements of the tested device.

Therefore, BINMOV will contain all necessary modules and architectures for the testing and validation stage of the principal and new products of NOVATEM. It will be enough to connect and exchange the card modules according to the size of the device under test and the type of signals to be measured and information to be gathered. BINMOV also envisages the scalability where if a new card module is developed for a special device, this module will form part of the available modules catalog and will be used in for future test.

The main contribution to BINMOV project was to conceptualize a solution capable of identifying several card modules which are plugged into a motherboard, in general, each card module corresponds to a sensor, actuator, monitor or control signal that depends on the type and size of the final mechatronic device under test. To achieve this conceptualization, it was indispensable first to identify the available hardware and software that we will be using for, to know which type of signals we will work with, to determine the protocol of communication and to design the electronics that will perform the identification tasks. Next sections summarize the principal tasks performed during the internship.

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3. INTRODUCTION

BINMOV is a project from NOVATEM society, it is pretended to be a test bench module that will help he company to reduce time when testing new developed devices.

The main characteristic of BINMOV is its modularity, it consists of a series of card modules that are plugged in a motherboard, they can be changed according to the type and size of the mechatronic system being tested so that if a new system should be tested it will be enough to connect a card according to the new device characteristics to perform a complete test. In this way the time is drastically reduced since the test bench module is ready and there is no need to create additional subsystems to test the main device.

During the internship I worked in conceptualizing a solution that allows the identification of each card, this identifier permits to know which card is being used and in which position is in the motherboard. The cards are different purposes modules, for instance, a card to measure the current of a motor, another to measure the voltage of a brake or the temperature of an engine. Therefore, with this identification system one can know both the measured variable and to which mechatronic device the transmitted electronic signal corresponds to.

BINMOV relays in the implementation of this card modules together with Speedgoat, a real-time target machine, that executes the routine test. This machine offers several I/O ports, PWM channels, single-ended and differential analog ports, and different communication protocols.

This document exposes how the identification task was accomplished first by understanding the available hardware characteristics, proposing different analog and digital solutions according to the requirements and finally by validating the design trough a PCB prototype.

3.1 The Company

NOVATEM SAS is an enterprise created in 2007 by Mr. Bertrand NOGAREDE, doctor, researcher, and former professor at engineering school ENSEEIHT in the field of electrical engineering specializing in electrodynamics.

NOVATEM deals with the design, sizing, manufacturing, and production of electric actuators combining electromechanics, electromagnetism, electrodynamics, and in general, electrical engineering.

The company acts in several fields of activity due to the versatility of its solutions such as: aeronautics, space, automobile, medicine, nuclear, naval

The dynamism of NOVATEM has allowed to collaborate and manage projects from numerous partners such as AIRBUS, SAFRAN, NAVAL GROUP, FINE HEART (Figure 1).

The company is present into two sites, a Production & Head office center in Coursan near Narbonne and a Research & Engineering center in Toulouse.

Figure 1. At he left - NEXGED project for Latécoère, electric piloting of an aircraft door.
At the right - Powerful electric motor developed by Novatem.
(NOVATEM SA, 2020)

3.2 Presentation of services

Table 1. NOVATEM services

NOVATEM Recherche	• High performance mechatronic integration • Reliability & Availability of electromagnetic converters • High frequency electromagnetic machines
NOVATEM Ingénierie	• Establishment of specifications according to demand • Study and calculate the sizing of mechanical, electromechanical, and electronic parts • Perform a multitude of simulations in order to have the best possible results • Develop a manufacturing file containing the different characteristics of the products (design, plan, power, etc.) • Perform the tests of the mechatronics assembly on a test bench, suitable for the latter
NOVATEM Production	• Test bench • Electronic card • Active part

3.3 NOVATEM Team

Table 2. NOVATEM staff

Ioav RAMOS	Engineer doctor *Head of the design office*
Bertrand NOGAREDE	Doctor of Electrical Engineering - Electrodynamics *Manager of NOVATEM*
Reda ABDOUH	Electromechanical engineer *Calculation Engineer*
Maxime NOMDEDEU	Mechatronics technician *Responsible for production and technical assistance*
Martin CRONEL	Engineer doctor in industrial computing *Industrial IT and control engineer*
Magali TRESSOL	ICA Auditor *Quality manager, administrative*
Alexandre GIRAUD	Engineer doctor *Post-doctoral researcher*

	Diploma
	Position in charge
Coursan site	
Toulouse site	

3.4 The project BINMOV

The BIMNOV project – Baies d'Interface Mécatronique NOVATEM (in french) – NOVATEM Mechatronic Interface Racks – aims to equip the company with a mean of testing, interfacing, and controlling mechatronic systems. Its main characteristics are its modularity and long-term availability. This structure (Figure 2) should make it possible to control and characterize mechatronic assemblies of various architectures.

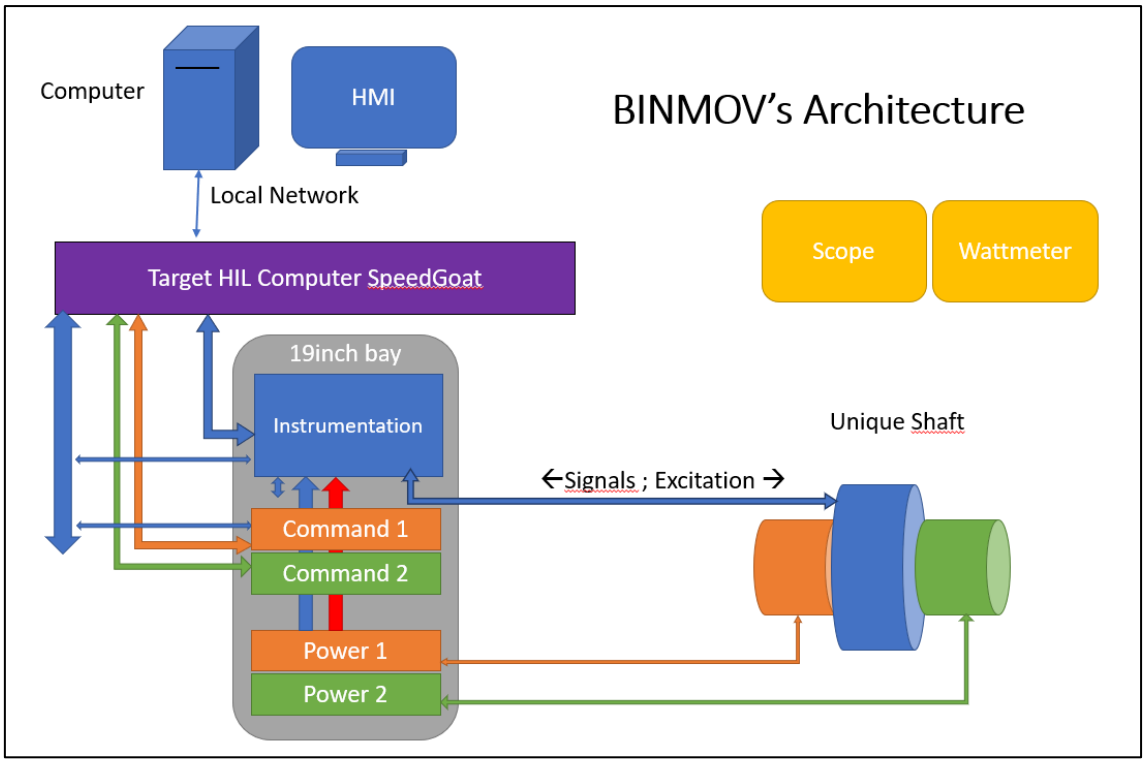

Figure 2. BINMOV's general architecture.

(NOVATEM SA, 2020)

The envisaged modularity is based on several aspects:

- The type of assembly under test:
  - Permanent magnet machine.
  - Induction machine.
  - MRV (variable reluctance machines) with limited number of phases.
  - Linear actuator based on the three machines above.
  - Zero current brake.
  - Controllable magnetic coupler.
  - Power electronics.

- The ability to switch easily between:
  - Behavioral simulation based on models.
  - Real-time simulation of a mechatronic assembly.
  - Mechatronic assembly control (RCP philosophy).
  - HIL simulation.
- The electronics of the bench that can be replaced by electronics under test with or without a mechatronic assembly.

The MBD philosophy, coupled with those of HIL and RPC, will allow the analytically simulated modules to be interchanged with those physically simulated, but also with hardware modules. This makes it possible, for example, to reduce the risk of errors being introduced during development or to make functions more easily according to the specifications. This new process also intrinsically makes it possible to reduce the time to market while increasing the operating safety of the assemblies.

Some of the electronic modules developed specifically for instrumentation will complete a fundamental research project on the intrinsic ferromagnetic qualities of materials intended for the manufacture of electrical machines. In addition, other modules will collect data intended for understanding the operation of a switching cell, precisely at the switching scale.

From an industrial research point of view, BIMNOV will allow the development of safe operating architectures, making it possible to place the functions as close as possible to the mechatronic assemblies while simulating them at the highest level of the developed system.

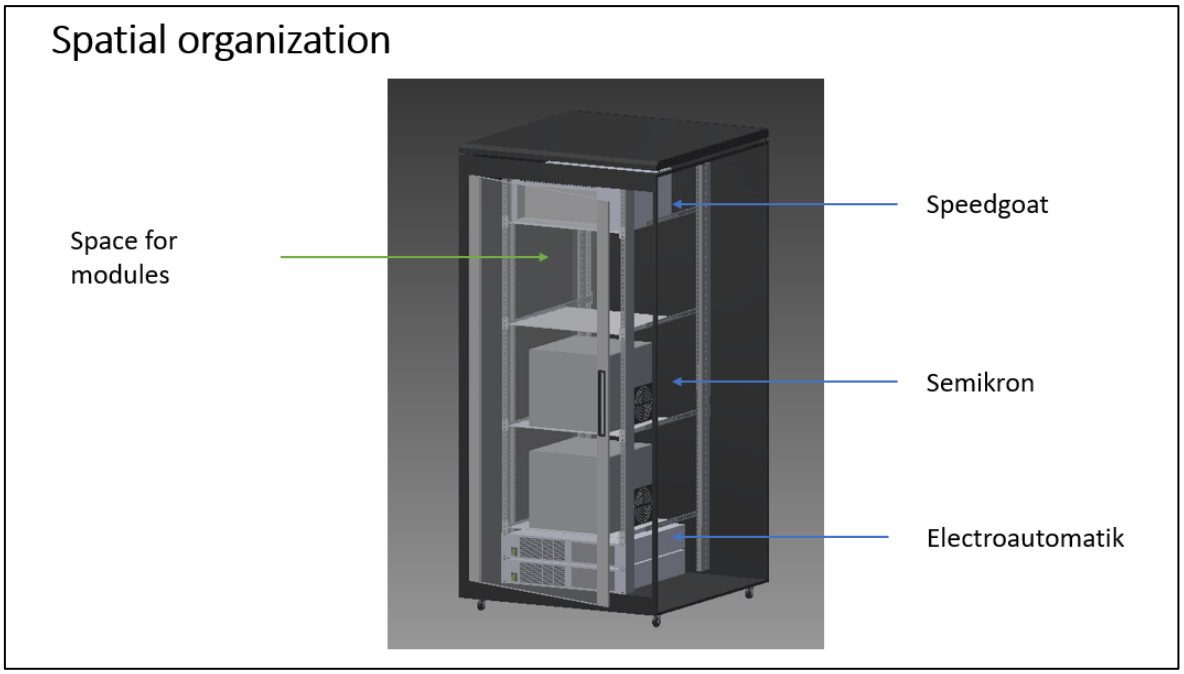

Figure 3. BINMOV's Spatial distribution

(NOVATEM SA, 2020)

The BIMNOV project therefore represents a double stake for the company, firstly as an extension of its own test resources, while constituting a significant opportunity to expand its commercial offer in the direction of the marketing of a modular and scalable test and characterization tool for its customers (NOVATEM SA, 2020).

3.5 State of the Project

When I was integrated in the project, the architecture, the modules that BINMOV owns and the general planning of the project had already been defined. How the tasks were going to be divided, the equipment required and necessary time to complete each stage were also defined, however the design work itself was just starting.

At that date BINMOV had an approximate advance of 40%. During the development of the internship the design part was attacked, especially the electronic and programming part. In these 6 months, several work teams including 2 interns participated

in the design of signal acquisition circuits, signal conditioning, filters, control and communication circuits.

By the time I am writing this report, it is estimated that BINMOV is at 65 %, in the coming months the functional tests will begin, and it is expected to achieve the 1.0 BINMOV version by the end of the year.

4. LITERATURE REVIEW

4.1 Hardware and Software Characterization

NOVATEM tests its developed devices employing the Hardware-in-the-loop methodology (Figure 4), HIL testing allows simulate sensors, actuators, and mechanical components in a way that all inputs/outputs of the device under test are connected long before the final system is integrated, this approach relays on the use of representative real-time responses, electrical stimuli and functional use cases (Add2, 2021).

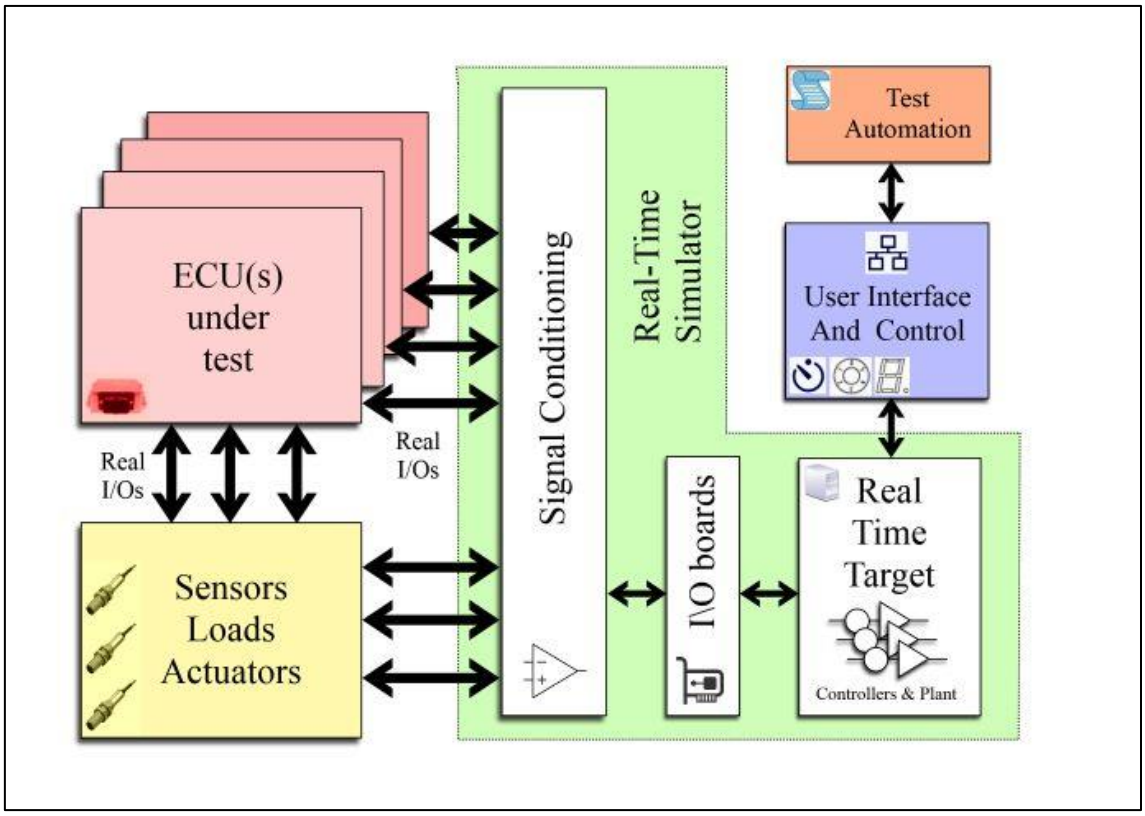

Figure 4. Hardware-in-the-loop representation
(Add2, 2021)

The modeling environment used by NOVATEM is Simulink where the plant models are created. This environment is run on a workstation, the host PC, and then the plant simulation is compiled into real-time executable code, which is downloaded to a second computer, called the target simulator. This simulator is a specialized hardware

device which contains special I/O boards and all required signal conditioning (Add2, 2021).

SPEEDGOAT is hardware device used to perform the HIL simulations, specifically the “Performance real-time target machine” model (Figure 5) is employed in NOVATEM, this device has a vast range of I/O connectivity and supports industrial protocols, ideal for multi-FPGA solutions requiring MHz closed-loop bandwidths and hundreds of I/O (Speedgoat, 2021).

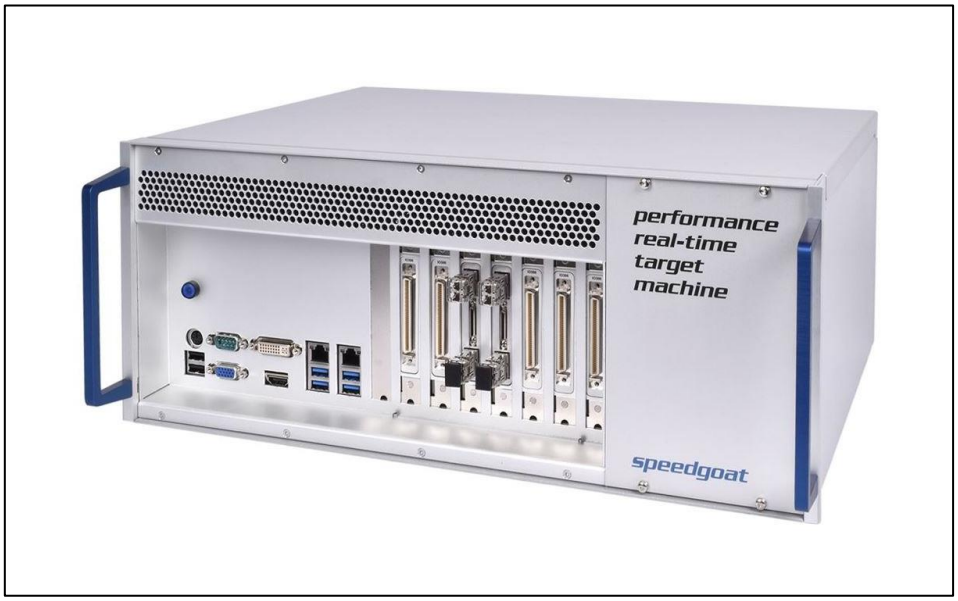

Figure 5. Performance real-time target machine
(Speedgoat, 2021)

This machine is equipped with modules that provides digital LVCMOS I/O lines, differential and common mode analog lines, PWM output lines, communication protocols interface, and interruption ports. They constitute a suitable interface for signal conditioning, converting voltage levels and shielding by adding protection against voltage shifting.

These modules are built in a plug-in concept which allows connect many modules depending on the application requirements (Figure 6). Specifically, the modules that will be used in BINMOV are the IO135-Performance, the IO333-325K-Performance, the

IO333-6-Performance and the IO333-21-Performance A briefly description concerning the electronic main characteristics, voltage levels and samples rates is presented in next sections.

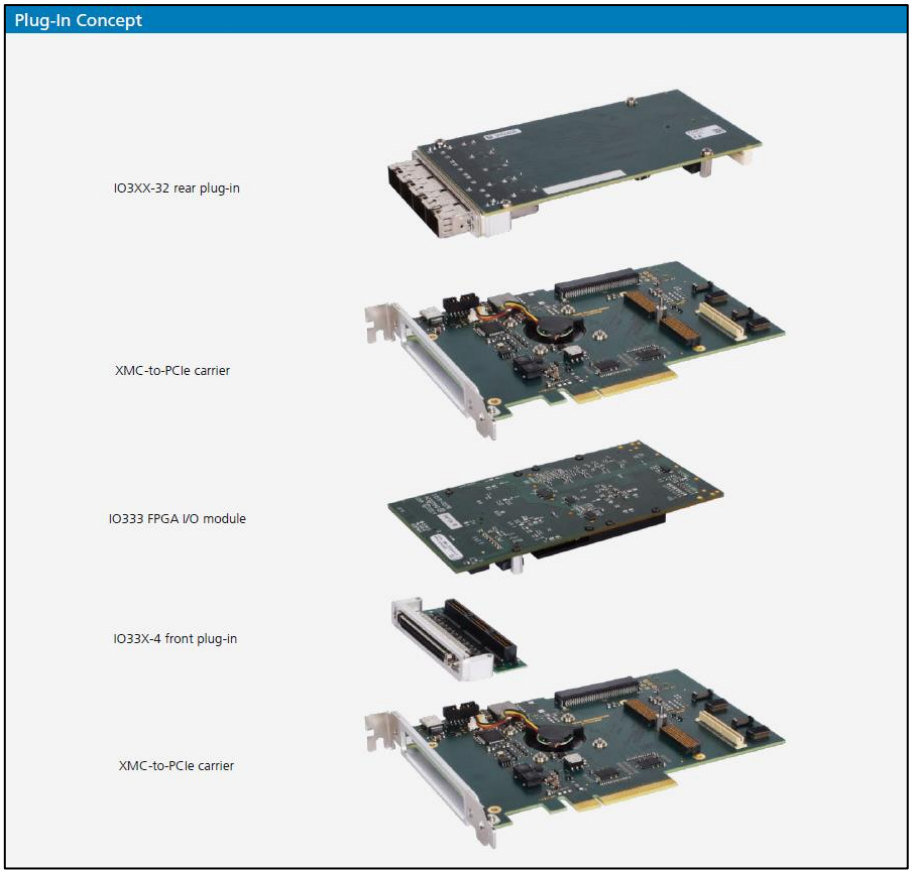

Figure 6. Plug-In Concept
(Speedgoat, 2020)

I/O333-6 Multifunction I/O Mezzanine Module

Input

- **High Speed Analog Input**

  16-bit Analog to Digital Converter (ADC) channels provide simultaneous sampling at a maximum rate of 500 kHz.

- **Programmable Input Voltage Range**

  Four gain selections are available that allow a bipolar input voltage range from ± 1.28 Volts to ± 10.24 Volts.

Output

- **Analog Output**

  Eight 16-bit Digital to Analog Converter (DAC) channels provide simultaneous update with a maximum rate of 100 KHz.

- **Programmable Output Voltage Range**

  Three gain selections are available that allow a bipolar output voltage range from ± 10 Volts to ± 10.5263 Volts (Acromag Inc., 2013).

Communication

The modules front IO333-6 and rear IO333-21 integrate also a 1x SPI Master/Slave (TTL), 1x I2C Master (TTL), 16x PWM (TTL), 1x Interrupt (TTL) channels.

Table 3. Communication protocols

Pin	Code Module Channel	Functionality	Direction	Transceiver
1		Ground		
2	1	SPI - CLK	IN/OUT	TTL
3	1	SPI - CS	IN/OUT	TTL
4	1	SPI - SDO	OUT	TTL
5	1	SPI - SDI	IN	TTL
61	1	I2C Master CLK	OUT	TTL
62	1	I2C Master Data	IN/OUT	TTL

(Speedgoat, 2021)

IO135 Analog and Digital I/O module

The Speedgoat IO135 module is a standard single-wide PCI Mezzanine Card (PMC)

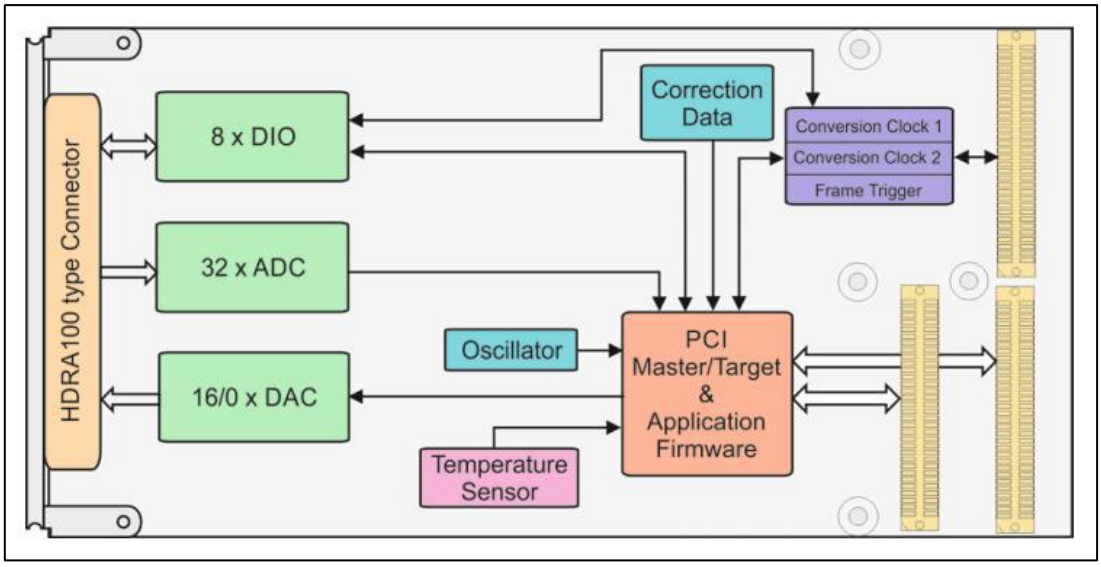

Figure 7. IO135 Block diagram.
(Speedgoat, 2018)

Input

- The IO135 module provide 32 true differential analog input channels (ADC Channels) avail-able at the Front I/O Connector.

- AD7609 from Analog Devices is used for the analog inputs. Each AD7609 provides eight 16-bit differential ADC channels (ADC Channels A-H).

- The IO135 module provide four AD7609s (ADC1, ADC2, ADC3 & ADC4), resulting in 32 analog input channels (Speedgoat, 2018).

- The ADCs offer true differential inputs with software selectable ±5V and ±10V bipolar input voltage ranges (one common setting for all eight channels of each ADC).

- The maximum sample rate of the ADCs is 200kSPS and they offer an oversampling capability with a digital filter (Speedgoat, 2018).

Table 4. ADC Electrical interface

Protection	7kV ESD rating ±16.5V Overvoltage Clamp Protection
Input Type	True bipolar differential
Input Impedance	1MΩ
Input Capacitance	5pF
Maximum Ground-Related Input Voltage	±5V and ±10V
Full Scale Range	±10V and ±20V
Common-Mode Input Range	±4V
Sample Rate	200kSPS

(Speedgoat, 2018)

Output

- The IO135 module provides up to 16 analog output channels (DAC Channels) available at the Front I/O Connector

- AD5754R from Analog Devices is used for the analog outputs. Each AD5754R provides four 16-bit single-ended DAC channels (DAC Channels A-D).

- The IO135 module provides four AD5754Rs (DAC1, DAC2, DAC3 & DAC4), resulting in 16 analog output channels (Speedgoat, 2018).

- The DACs offer software selectable 0-5V, 0-10V, 0-10.8V, ±5V, ±10V and ±10.8V output voltage ranges (individual setting for each of the four channels of each DAC).

- The settling time is typically 10µs and the DAC channels can drive a load of 2kΩ, with a capacitance up to 4000pF (Speedgoat, 2018).

Table 5. DAC Electrical interface

Protection	3.5kV ESD rating 20mA current limit
Output Type	unipolar/bipolar single-ended
Output Voltage Ranges	±5V, ±10V, ±10,8V, +5V, +10V and +10.8V
DC Output Impedance	0.5Ω
Maximum Load	2kΩ
Capacitive Load	4000pF
Settling Time	10µs

(Speedgoat, 2018)

In case of a DAC Channel overcurrent condition, the DAC Channel is powered down and its output is clamped to ground with a resistance of ~4kΩ.

Digital I/O

Each of the 8 Digital I/O lines on the Front I/O connector and each of the Global Conversion Signals on the P14 Rear I/O are realized by separated input and output buffers with a 4.7kΩ pull resistor.

Additionally, each signal is equipped with an electronic protection array for ESD protection.

Table 6. Digital I/O and P14 Rear I/O Electrical Interface

Protection	±15kV ESD protection
Driver Level	LVTTL (3.3V)
Receiver	5V tolerant
Source current per line	15mA
Sink current per line	6mA

(Speedgoat, 2018)

4.2 Signals Assignation/Identification

Once the available hardware components and its electrical performances were identified, next step was to identify the principal systems and groups of signals that BINMOV will be managing when testing the mechatronic devices.

The principal groups are control signals that will be transmitted from Speedgoat to the final actuator devices, data signals used to communicate sensors information, fast instrumentation signals used to detect abnormal behavior, and slow signals employed to identify each mechatronic assembly under test.

The assignation task was achieved by mapping all signals to the card modules pins, in this way we define the signals going from Speedgoat to the Bay and after conditioning and level conversion at this stage, the corresponding signals going from the Bay to final mechatronic device under test and vice versa.

For instance, an extrait of the signals identified going from Speedgoat to the Bay is showed in Table 7 where we can notice which final device the signal corresponds to, the number pin where it is connected to, the card module associated (IO35) and the type of signal (analog differential). This table is quite extensive comprising the 3 Speedgoat card modules, however an extrait is presented to give the lector a general idea of the signal routing.

Table 7. Extrait of signals going from Speedgoat to the Bay.

Carte	Port	N°	Pin	Dispositif	Signal Name
IO135-Performance [200 kSPS]	Analog Inputs (Differential)	1	1	DARS	LVDT V1 +
			51		LVDT V1 -
		2	2		LVDT V2 +
			52		LVDT V2 -
		3	3		LVDT V +
			53		LVDT V -
		4	4	BANC	LVDT V1 +
			54		LVDT V1 -
		5	5		LVDT V2 +
			55		LVDT V2 -
		6	6		LVDT V +
			56		LVDT V -
		7	7	COMBO Temp	COM +
			57	COM	COM -
		8	8	COMBO Temp	MON +
			58	MON	MON -
			9	GND	
			59	GND	
		9	10	COMBO Tension	COM +
			60	COM	COM -
		10	11	COMBO Tension	MON +
			61	MON	MON -
		11	12	COMBO Courant	COM +
			62	COM	COM -
		12	13	COMBO Courant	MON +
			63	MON	MON -
		13	14	Moniteur BUS	+ 24 VC +
			64		+24 VC -
		14	15	Moniteur BUS	+ 24 VP +
			65		+ 24 VP -
		15	16	Moniteur BUS	+ 5 VC +
			66		+ 5 VC -
			17	Moniteur BUS	- 5 VC +
			67		- 5 VC -
		16	18	GND	
			68	GND	
			19	Moniteur BUS	+ 15 VP +
			69		+ 15 VP -
		17	20	SEMIKRON 1	TEMP 1 (10)
			70		
		18	21	SEMIKRON 2	TEMP 2 (11)
			71		

In the same way Table 8 shows un extrait of the pin assignation but this time regarding the signals that output from the Bay to the final mechatronic device like power signals, excitation, and monitoring signals.

Table 8. Extrait of signals going from the Bay to Speedgoat.

		Connector	PIN	Signal Name	Code name	Signal type
DARS	OUT	Power	A	Motor phase 2	ELM_POW-Ph2	Power supply
			B	Motor phase 1	ELM_POW-Ph1	Power supply
			D	Motor phase 3	ELM_POW-Ph3	Power supply
		Signal	2	POB Power supply	POB_POW-H	Power supply
			3	POB Power supply Return	POB_POW-L	Power supply
	OUT		5	LVDT excitation	VP+	Power supply
			22	LVDT excitation Return	VP-	Power supply
	IN		7	LVDT Output V1	V1+	Measurement
			8	LVDT Output V1 Return	V1-	Measurement
			9	LVDT Output V2	V2+	Measurement
			24	LVDT Output V2 Return	V2-	Measurement
			15	PTS COM Power	LV10_COM-H	Power supply
			28	PTS COM Power Return	LV10_COM-L	Power supply
	IN		13	PTS COS Output	COS_COM-H	Measurement
			12	PTS COS Output Return	COS_COM-L	Measurement
			26	PTS SIN Output Return	SIN_COM-L	Measurement
			11	PTS SIN Output	SIN_COM-H	Measurement
			31	PTS MON Power	LV10_MON-H	Power supply
			37	PTS MON Power return	LV10_MON-L	Power supply
	IN		30	PTS TEMP MON Output	TEMP_MON-H	Measurement
			36	PTS TEMP MON Output Return	TEMP_MON-L	Measurement
			33	PTS TEMP COM Output	TEMP_COM-H	Measurement
			34	PTS TEMP COM Output Return	TEMP_COM-L	Measurement
PARKER	OUT			1		
				2		
				3		
BANC	IN			LVDT V1 +		
				LVDT V1 -		
				LVDT V2 +		
				LVDT V2 -		
	OUT			Excitation +		
				Excitation -		

4.3 Selection of the communication protocol.

As the modules IO333-6 and IO333-2 support SPI and I2C communication respectively, it was a key decision to determine among these two communication protocols which one BINMOV will implement to communicate data, monitoring and control signals. Next sections show a brief description and main characteristic of each protocol.

Inter-Integrated Circuit Protocol - I2C

The Inter-Integrated Circuit Protocol (I2C) is a serial communication protocol intended to allow the connection of multiple “speripheral devices” with one or more “controller devices” in a single bus to transmit data (Figure 8). It is only intended for short distance communications within a single device like the Serial Peripheral Interface (SPI) and only requires two signal wires to exchange information like Asynchronous Serial Interfaces such as RS-232 or UARTs (Sparkfun, 2013).

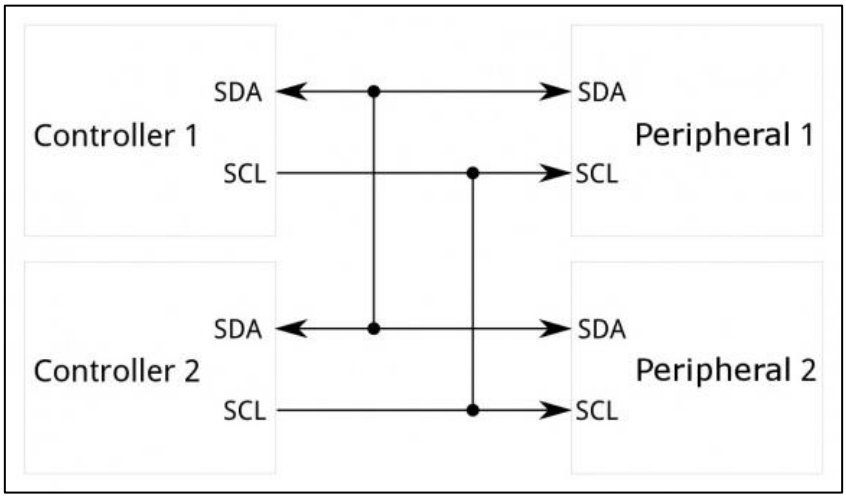

Figure 8. Inter-Integrated Circuit (I2C) Protocol.
(Sparkfun, 2013)

- **SDA (Serial Data):** The line for the master and slave to send and receive data. I2C is a serial communication protocol so data is transferred bit by bit along this line.

- **SCL (Serial Clock):** The line that carries the clock signal. I2C is synchronous, so the output of bits is synchronized to the sampling of bits by a clock signal. The clock signal is always controlled by the master.

Table 9. I2C Main characteristics

Wires Used	2
Maximum Speed	Standard mode= 100 kbps
	Fast mode= 400 kbps
	High speed mode= 3.4 Mbps
	Ultra fast mode= 5 Mbps
Synchronous or Asynchronous?	Synchronous
Serial or Parallel?	Serial
Max # of Masters	Unlimited
Max # of Slaves	1008

(Campbell S. , 2016)

To transmit data, messages are broken up into frames of data (Figure 9). Each message contains the address frame that includes the binary address of the slave, and one or more data frames that contain the data being transmitted. The message also includes start and stop conditions, read/write bits, and ACK/NACK bits between each data frame.

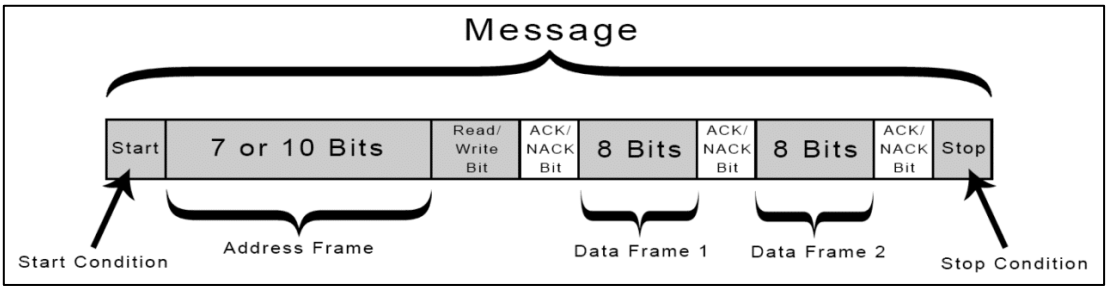

Figure 9. I2C message frame
(Campbell S. , 2016)

- **Start Condition:** The SDA line switches from a high voltage level to a low voltage level before the SCL line switches from high to low.

- **Stop Condition:** The SDA line switches from a low voltage level to a high voltage level after the SCL line switches from low to high.

- **Address Frame:** A 7- or 10-bit sequence unique to each slave that identifies the slave the master wants to talk to.

- **Read/Write Bit:** A single bit specifying whether the master is sending data to the slave (low voltage level) or requesting data from it (high voltage level).

- **ACK/NACK Bit:** Each frame in a message is followed by an acknowledge/no-acknowledge bit. If an address frame or data frame was successfully received, an ACK bit is returned to the sender from the receiving device (Campbell S. , 2016).

Serial Peripheral Interface - SPI

The Serial Peripheral Interface protocol requires at least 4 lines to connect a single controller to a single peripheral (Figure 10), each additional peripheral device requires one additional chip select I/O pin on the controller.

One benefit of SPI is that data can be transferred without interruption and any number of bits can be sent or received in a continuous stream, however SPI only allows one controller on the bus, but it does support an arbitrary number of peripherals (Campbell S. , 2013).

The increment of pins becomes the principal drawback in situations where lots of devices must be connected to one controller. Also, the large number of connections for each device can make routing signals more difficult in tight PCB layout designs (Sparkfun, 2013).

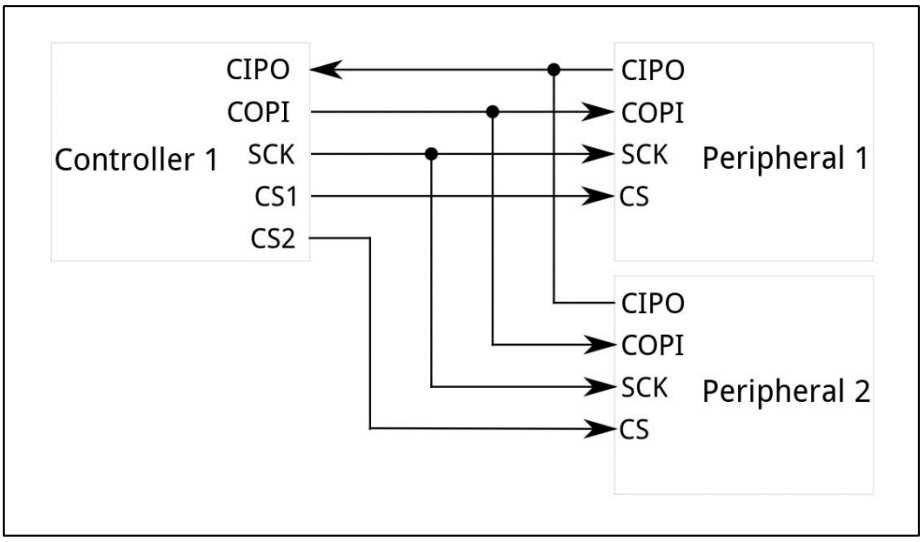

Figure 10. Serial Peripheral Interface (SPI) protocol.
(Sparkfun, 2013)

- **MOSI (Master Output/Slave Input):** Line for the master to send data to the slave.
- **MISO (Master Input/Slave Output):** Line for the slave to send data to the master.
- **SCLK (Clock):** Line for the clock signal.
- **SS/CS (Slave Select/Chip Select):** Line for the master to select which slave to send data to.

Table 10. SPI main characteristics.

Wires Used	4
Maximum Speed	Up to 10 Mbps
Synchronous or Asynchronous?	Synchronous
Serial or Parallel?	Serial
Max # of Masters	1
Max # of Slaves	Theoretically unlimited*

(Campbell S. , 2013)

To summarize, Table 11 shows a brief comparison between I2C and SPI. Considering the characteristics of each protocol, and the nature of BINMOV where several modules are going to be intercommunicated, where a significant but not too large amount of data must be sent and received between the modules and the controller

(Speedgoat) and also considering the restricted size of the Bay, the fact that the physical wiring should be as minimum as possible and the limited number of pins, I2C protocol was stablished as the main communication interface in BINMOV

Table 11. I2C vs SPI

	Advantages	**Drawbacks**
I2C	▪ Only uses two wires ▪ Supports multiple masters and multiple slaves ▪ ACK/NACK bit gives confirmation that each frame is transferred successfully ▪ Hardware is less complicated than with UARTs ▪ Well known and widely used protocol	▪ Slower data transfer rate than SPI ▪ The size of the data frame is limited to 8 bits ▪ More complicated hardware needed to implement than SPI
SPI	▪ No start and stop bits, so the data can be streamed continuously without interruption ▪ No complicated slave addressing system like I2C ▪ Higher data transfer rate than I2C (almost twice as fast) ▪ Separate MISO and MOSI lines, so data can be sent and received at the same time	▪ Uses four wires (I2C and UARTs use two) ▪ No acknowledgement that the data has been successfully received ▪ No form of error checking like the parity bit in UART ▪ Only allows for a single master

(Campbell S. , 2016)

5. RESEARCH METHODOLOGY AND DESIGN

5.1 Card Identification

BINMOV's electronic modules must sense data, condition them into the appropriate electronic levels and transmit them to Speedgoat, the Real-Time Target Machine. Therefore, one should know where data comes from, which module is transmitting to identify which kind of signals we are reading and which final mechatronic device under test we are looking at.

To achieve this signal identification, BINMOV envisages to develop a series of card modules built in a plug-in concept. Each one of these cards can be mounted in a motherboard, the idea is that each card contains a small circuit dedicated to provide a unique identifier for the card itself.

This identification will allow distinguish which card is plugged in the motherboard and like that one can know which signal is being transmitted. BINMOV being a project whose one of its purposes is the modularity and the capability of testing of a large number of developed and new devices, it envisages creating several card modules, for instance, the main cards for testing an engine will consist in a voltage, current, torque and temperature modules, each one will have its own identifier and in case if a similar engine smaller, more powerful or bigger should be tested in another project, a new group of cards according to the new voltage, current levels will be developed implying new identifiers but with the idea that it will be enough to plug-in the new cards into the motherboard and BINMOV will be ready to test the new device without additional electronics.

Figure 11 represents a general view how the motherboard will contain several interchangeable modules, each module dedicated to a specific control or measuring task,

with a single identifier that allows to recognize the type of card and the position where it is connected.

The key contribution to BINMOV project during the internship development was to conceptualize a solution that will deal with the identification task. Next sections describe the main stages and evolution of this conceptualization, going from analog solutions to digital ones, briefly presenting IC components according BINMOV requirements and finally designing, building, and testing a PCB prototype.

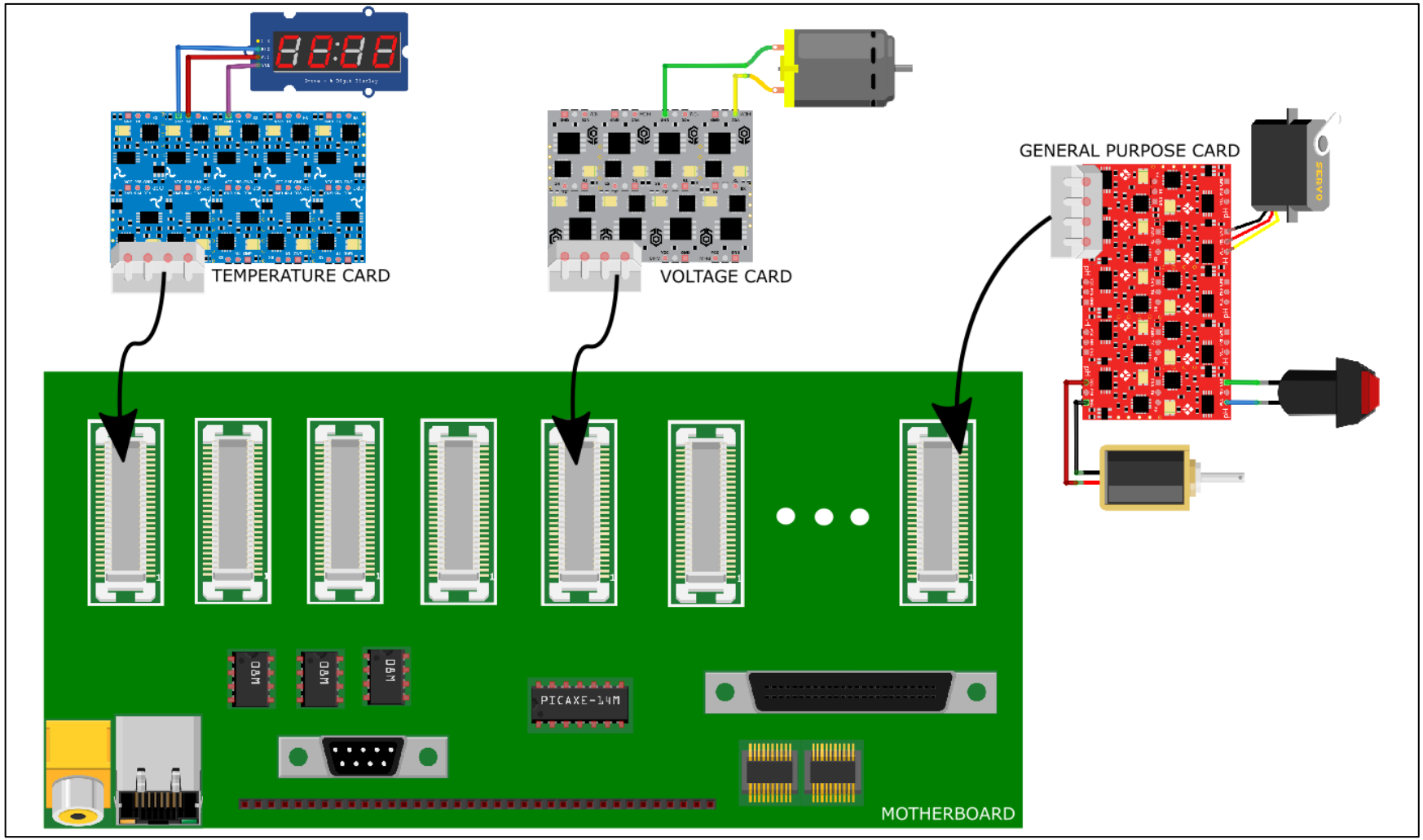

Figure 11. BINMOV's Motherboard and Card Modules representation

6. PROPOSED SOLUTIONS FOR CARD IDENTIFICATION

6.1 Analog Solutions

6.1.1 Voltage Divider

One proposed solution was to generate the identifiers with a single voltage divisor. The idea is to define different resistor values to generate as many tension levels as cards will be connected, then this voltage level will be read and converted to digital value thanks to an ADC, this ADC will send the digitalized voltage level through the I2C bus to Speedgoat.

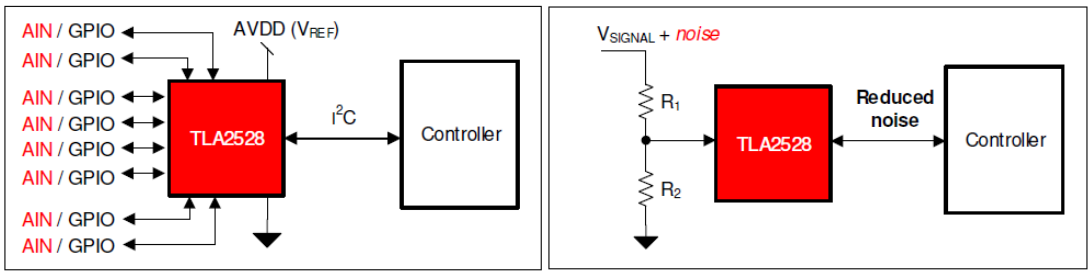

Figure 12. TLA2528 Application
(Texas Instruments, 2019)

Figure 12 represents the architecture that is being proposed, fortunately in the chips market there is enough performing devices dedicated to this kind of applications. The IC TLA2528 was selected to be implemented in this configuration because it integrates an internal multiplexer to read 8 different analog voltage levels, an ADC that can be connected directly to the bus because has an I2C interface.

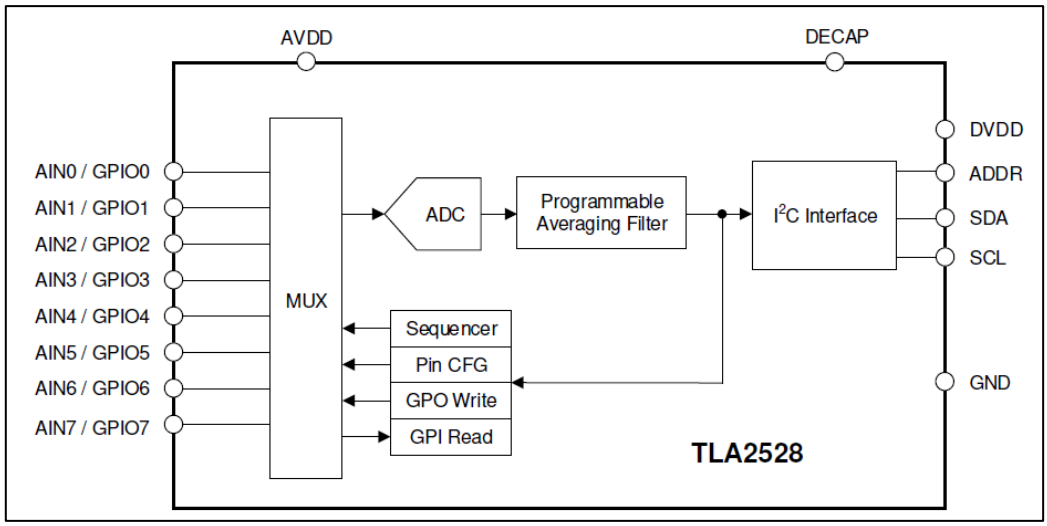

Figure 13. TLA2528 Block Diagram
(Texas Instruments, 2019)

The TLA2528 has an address selection pin that allows to choose 8 different addresses (Table 12), that means we can achieve to have until 64 card modules on the same bus.

Table 12. I2C Address selection

RESISTORS		ADDRESS
R1 (1)	R2 (1)	
0 Ω	DNP (2)	001 0111b (17h)
11 kΩ	DNP (2)	001 0110b (16h)
33 kΩ	DNP (2)	001 0101b (15h)
100 kΩ	DNP (2)	001 0100b (14h)
DNP (2)	DNP (2)	001 0000b (10h)
DNP (2)	11 kΩ	001 0001b (11h)
DNP (2)	33 kΩ	001 0010b (12h)
DNP (2)	100 kΩ	001 0011b (13h)

(Texas Instruments, 2019)

A closer look at the divisor suggests connecting an operational amplifier in the voltage output configured as common follower with an unitary gain (Figure 14). This additional component will help to guarantee the adequate voltage level when connecting the divisor to the IC.

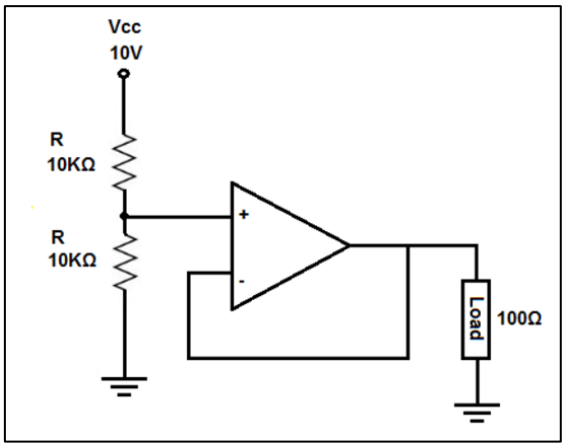

Figure 14. Voltage Stabilizer Circuit using a Buffer

Therefore, an interactive excel sheet was developed to define the R2 values when R1 fixed to a defined value. Table 13 shows an extrait of the sheet for the first 10 tension values and the corresponding R2 values, these values can be adjusted according to the number of cards implemented, the input voltage and the desired power consumption in the divisor.

Table 13. R2 values when R1 is fixed

	Binary Value	Vc Voltage mV	Bit max diff	Voltage diff mV	R2 if R1 is		R2 diff	ZR	I	P
			100	80.57	10000			Ohm	mA	mW
	0	0								
			50	40.28		123.58				
1	100	80.57			250.25		256.55	10250.25	0.32	1.06
			150	120.85		380.13				
			219	176.44		564.87				
2	269	216.72			702.90		279.72	10702.90	0.31	1.02
			319	257.01		844.59				
			388	312.60		1046.39				
3	438	352.88			1197.38		306.16	11197.38	0.29	0.97
			488	393.16		1352.55				
			557	448.75		1573.89				
4	607	489.04			1739.75		336.55	11739.75	0.28	0.93
			657	529.32		1910.44				
			726	584.91		2154.30				
5	776	625.20			2337.35		371.69	12337.35	0.27	0.88
			826	665.48		2525.99				
			895	721.07		2796.00				
6	945	761.35			2999.05		412.64	12999.05	0.25	0.84
			995	801.64		3208.64				
			1064	857.23		3509.23				
7	1114	897.51			3735.75		460.75	13735.75	0.24	0.79
			1164	937.79		3969.99				
			1233	993.38		4306.67				
8	1283	1033.67			4560.97		517.79	14560.97	0.23	0.75
			1333	1073.95		4824.47				
			1402	1129.54		5204.16				
9	1452	1169.82			5491.68		586.13	15491.68	0.21	0.70
			1502	1210.11		5790.29				
			1571	1265.70		6221.78				
10	1621	1305.98			6549.49		668.94	16549.49	0.20	0.66
			1671	1346.26		6890.72				

6.1.2 Voltage reference

As there will be at least 64 different card modules, to achieve a correct identification, resistors must guarantee the appropriate voltage levels, that means that the input tension should be very stable all the time and the resistor selected high-performing so there will be no fluctuation at the output.

For instance, if we set an input voltage like $Vin = 3.3\ [V]$ and considering the TLA2528 ADC resolution $N = 12$, the less significant bit is $LSB = 0.8057\ [mV]$. So, we should mange tension in the millivolts range by simply changing the resistors, evidently the resistor value should be as close as possible to the determined in the green column, however in the market there is standard resistor values and sometimes the available component does not match the required value.

To face this constraint, the solution proposed is to use a voltage reference. The main benefit of using this component is that the output voltage will remain stable so that we can guarantee a different tension level for each module, the division is also done by using two resistors, but as we have large input and output voltage (up to $V = 36\ [V]$ for TL431) there is less risk to overlap the output tension level when choosing the commercial resistor values.

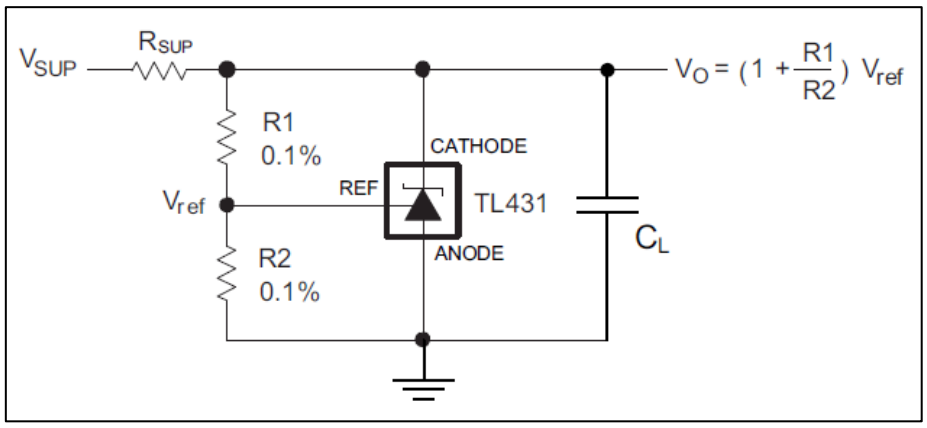

Figure 15. Shunt Regulator Schematic
(Texas Instruments, 2014)

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the midpoint tied to the reference pin. This can be seen in Figure 15, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation (Texas Instruments, 2014).

$$V_o = (1 + \frac{R_1}{R_2})V_{ref}$$

The proposed solutions could have worked if they had been implemented, however at this stage, NOVATEM BINMOV's committee decided to take the digital way because from their experience the environment where this circuit is going to be implement has electromagnetic compatibility issues, the signal quality is going to be degraded, some data will be lost when performing the ADC, the transmission, and the DAC. Therefore, a new solution was required but this time using high or low levels, the new approach to face the identification task is explained in next section.

6.2 Digital Solutions

To identify different cards, the proposed digital solution envisages the use of an integrated circuit which allows the communication of data via the I2C protocol, so that we can send the unique identifier associated with each type of card trough this bus.

I2C communication is done through a unique address, specific to each device on the bus, it is this identifier that allows the devices to recognize who is sending the message and who will receive it. However, since ICs are used, it is the manufacturers in general who have already set the address linked to each of the devices.

In this context, we are limited by the number of devices (same kind of devices) that we can put in the communication bus. There are some ICs that have dedicated addressing pins, then it is possible to configure in the device another address so that we can have multiple components on the same bus. However, the same manufacturer limits the addressing by the number of pins dedicated to this function, in the best case it is possible to have 8 different addresses which means that we are limited to connecting 8 ICs on the bus if we use the same chip.

In order to overcome this limitation, it is proposed to use an IC capable of managing the identification of several cards. If we use a byte for the card’s identifier, we will have the possibility of having up to 255 different types of cards knowing that we reserve the identifier 0000 0000 when there is no module on the motherboard. So, three new solutions were proposed.

6.2.1 Solution 1: 8 TCA9555 Chip Implementation – Until 16 modules on the motherboard

An assemble of 8 chips TCA9555 on the same bus will allow to have until 16 different cards because this IC owns 3 configurable slave address pins and 2 ports of 8 bits each (Figure 16), so each one of them can manage a pair of devices at the same time. The chip main characteristics are stated:

- 400-kHz Fast I2C Bus
- Configurable Slave Address with 3 Address Pins
- Low Standby-Current Consumption of 3.5 µA Maximum
- 16-bit I2C to Parallel Port Expander
- General-purpose remote I/O expansion for most microcontroller families via the I2C
- Designed for 1.65-V to 5.5-V VCC operation
- At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits (Texas Instruments, 2019).

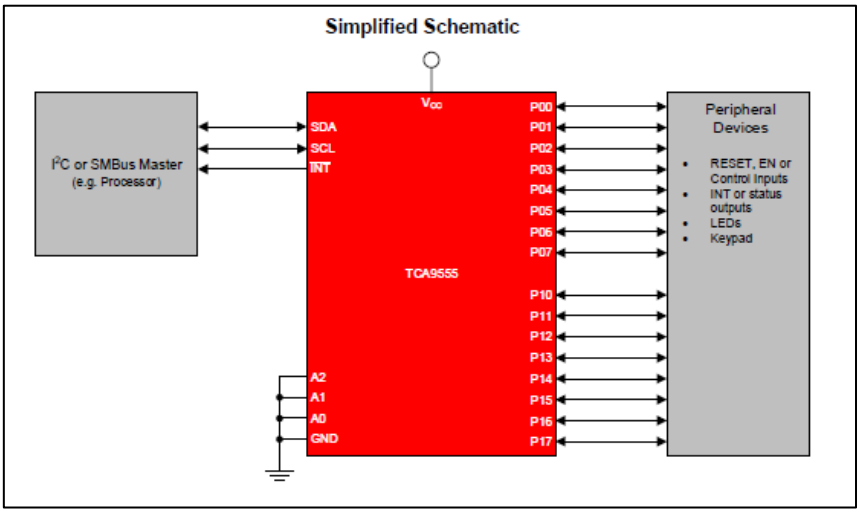

Figure 16. TCA955 Chip general description
(Texas Instruments, 2019)

As stated, the slave address selection is done by connecting the pins A2, A1 and A0 to +Vcc or GND (Figure 17). The last bit corresponds to the type of operation that we perform on the device, 1 if we read the ports' state, or 0 if we want to write on these ports.

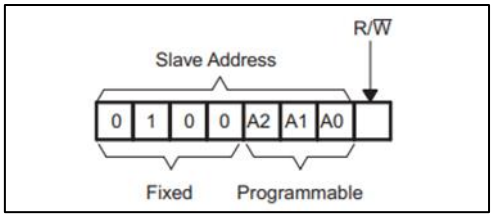

Figure 17. TCA9555 Address
(Texas Instruments, 2019)

This selection address pins allow to have according to the manufacturer a maximum of 8 different devices on the same I2C bus as depicted in the Table 14.

Table 14. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 0x20 (hexadecimal)
L	L	H	33 (decimal), 0x21 (hexadecimal)
L	H	L	34 (decimal), 0x22 (hexadecimal)
L	H	H	35 (decimal), 0x23 (hexadecimal)
H	L	L	36 (decimal), 0x24 (hexadecimal)
H	L	H	37 (decimal), 0x25 (hexadecimal)
H	H	L	38 (decimal), 0x26 (hexadecimal)
H	H	H	39 (decimal), 0x27 (hexadecimal)

(Texas Instruments, 2019)

A typical application of this component proposed by the fabricant is detailed in the following diagram (Figure 18) where the TCA9555 is used to control subsystems which are generally far from the master (processor - microcontroller). The TCA955 is dedicated to manage discrete signals 1 or 0 generally related to enabling, reset, activation, inactivation of other devices and it can also read other devices' outputs and send this data to the master through the I2C bus.

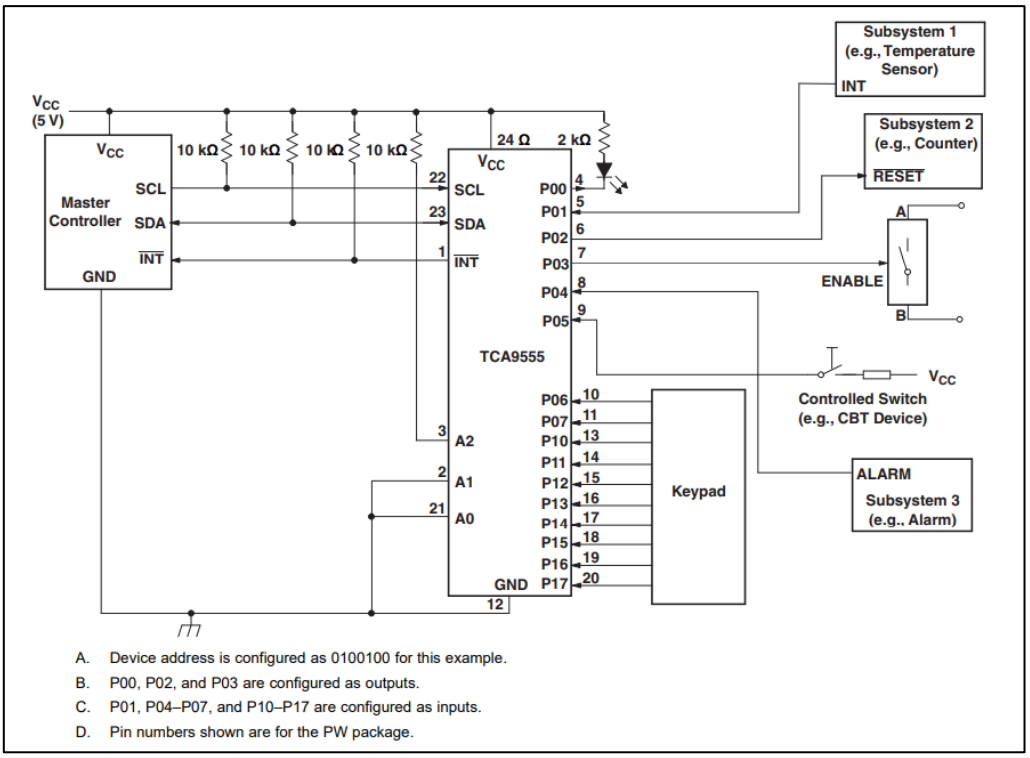

Figure 18. Typical Application
(Texas Instruments, 2019)

Fault Detection

BINMOV test bench uses several sensors to detect failures like overvoltage, short circuits and temperatures out of range, this kind of signals together with control signals play a critical role to ensure whole integrity of the architecture and should be monitored instantly.

Time reaction becomes a critical factor when an undesired condition occurs and the SPEEDGOAT machine, the master, should take the corrective action, even stop all modules as quickly as possible. In this way, the master must know when a such critical condition occurs, so to communicate with sensors it disposes a direct line of communication that can be connected to the controlling and monitoring devices, this channel corresponds to one of the SPEEDGOAT interruption pins.

The TCA9555 has also a dedicated interruption output $\overline{INT}$ (Figure 19), this output can be connected directly to the master interruption input. In this way the device can directly inform SPEEDGOAT that a change in the inputs of the TCA9555 has just happened without the need to use the I2C bus.

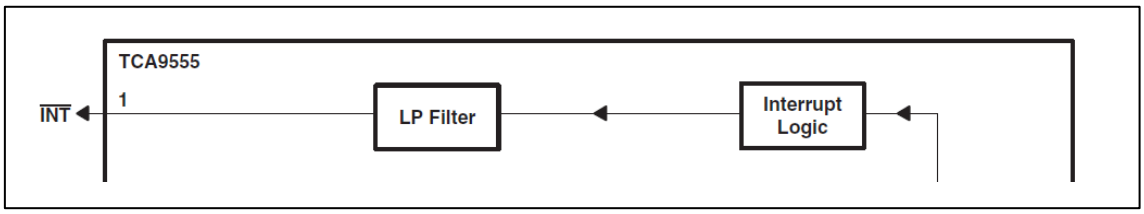

Figure 19. Interruption output pin
(Texas Instruments, 2019)

The interrupt is generated by the falling or rising of a signal connected to the component's inputs ports when configured as a reading device.

Then, 16 inputs of one TCA955 can focus on monitoring “1” or “0” type signals dedicated to fault management and as soon as a change in the input ports is detected, the TCA955 will immediately set the $\overline{INT}$ channel to low informing directly SPEEDGOAT, without using a communication protocol, that one of the detection critical signals has changed.

Therefore, the microprocessor will know in advance that a change or rather an error in the system has just occurred before establishing communication with the slave via the I2C bus and it will be able to stop everything or perform the dedicated actions because faults are found faster.

With this proposal we will also avoid having to do a check every x second in order to confirm the integrality of the entire system, this means that the I2C bus will only be used for data transmission and not for the check routines reducing the volume of data in the communication channel.

These all-stated features, the type, amount of data and how it is transmitted make the TCA9555 a strong solution to perform the card identification for BINMOV. Therefore, the following architecture presented in Figure 20 is proposed to deal with the module identification.

One can notice that two cards can be connected to each TCA9555 chip making this device able to manage until 16 different cards in this configuration, however, one is reserved for fault detection functionality

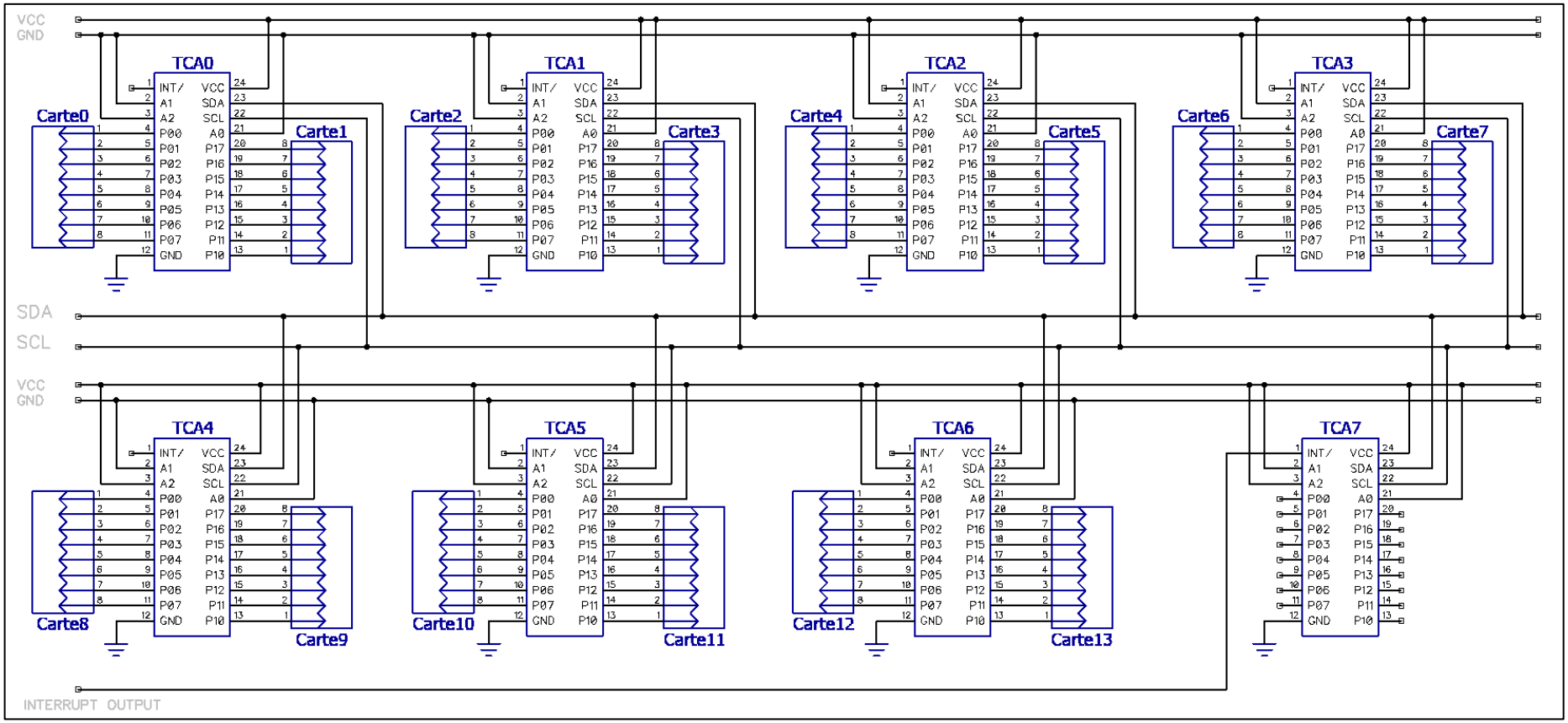

Figure 20. Solution 1: 8 TCA9555 Chip Implementation with interruption line

6.2.2 Solution 2 – 6 TCA9555 and 2 TCA6424A combination – Until 18 modules on the motherboard

The TCA6424A component also manufactured by Texas Instruments presents similar characteristics as the TCA9555 that's the principal reason why we propose to make a combined structure to have two more devices at the same bus.

- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- I2C to Parallel Port Expander supply.
- Low Standby Current Consumption of 1 μ
- 400-kHz Fast I2C Bus
- 24-bit I/O expander for the two-line bidirectional I2C (Texas Instruments, 2014).

This component can drive 3 cards considering that each one will use a port of 8 bits, however it allows only 2 address selection by connecting the ADDR pin to Vcc or GND, so a maximum of two TCA6424A chips can be in the same I2C Bus (Figure 21).

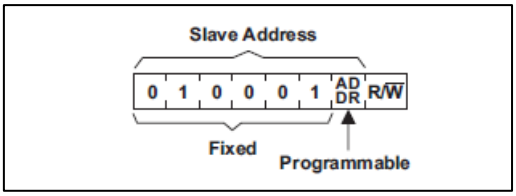

Figure 21. TCA6424A Address
(Texas Instruments, 2014)

But it is the manufacturer who has imposed the same address for both devices, therefore we propose to replace the TCA9555 with address 0x22 and 0x23 for TCQ6424A chips (Table 15), in this way we can increment the number of cards by 2, so a total of 18 cards can be handled in the bus.

Table 15. Address Reference

ADDR	I^2C BUS SLAVE ADDRESS
L	34 (decimal), 22 (hexadecimal)
H	35 (decimal), 23 (hexadecimal)

(Texas Instruments, 2014)

Figure 22 illustrates the implementation of this configuration, we can notice that for the TCQ6424A address selection only one pin is required. A device can also be reserved for fault detection signals if required since all have output interruption $\overline{INT}$ pins.

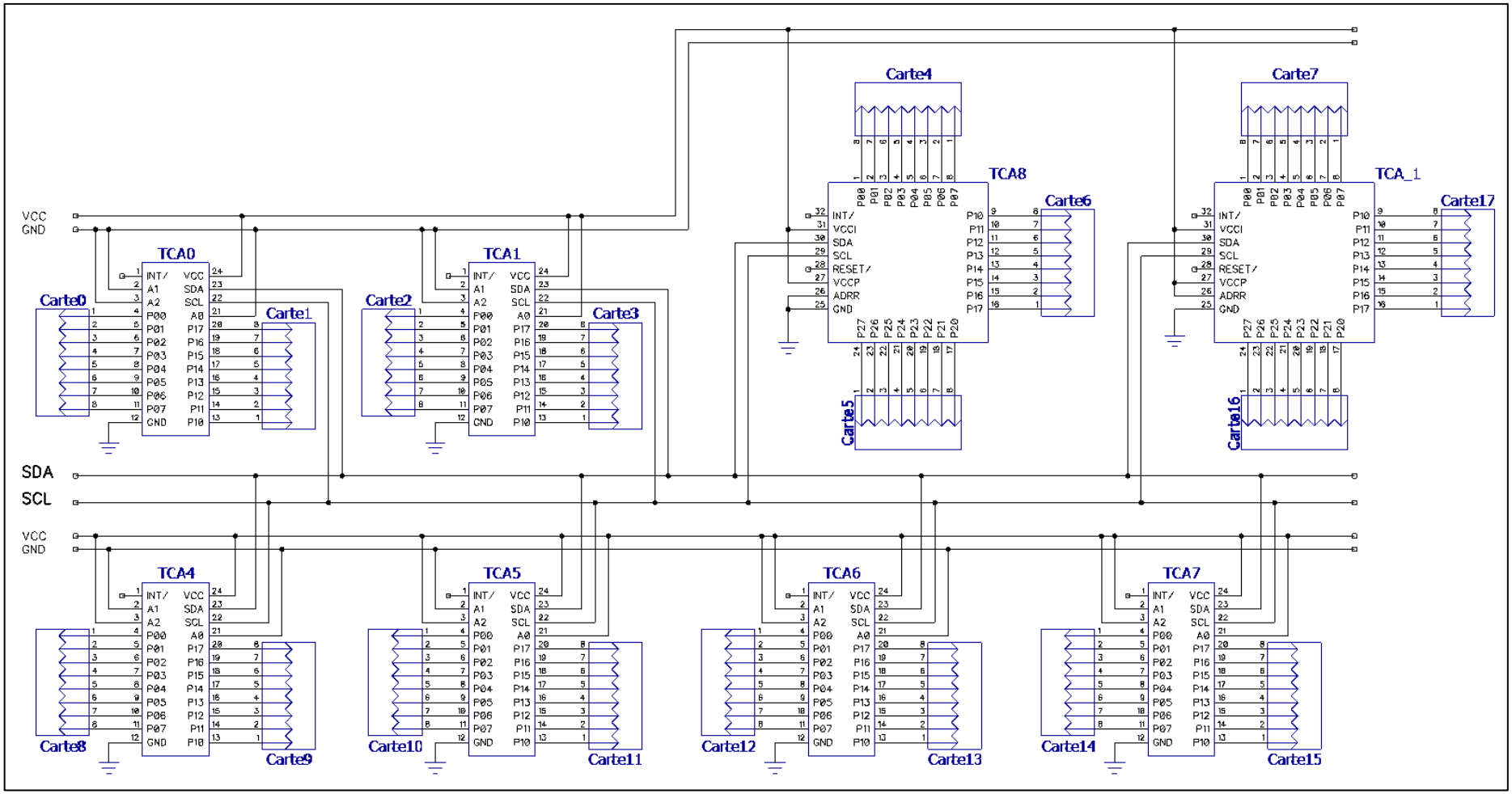

Figure 22. Solution 2 – 6 TCA9555 and 2 TCA6424A combination.

6.2.3 Solution 3 – MAXIM7311 2-Wire-Interfaced 16-Bit I/O Port Expander – Until 64 modules on the motherboard

To face the limited number of cards and the imposed address set by the manufacturer, after a carefully research, two IC that can handle more devices were identified, the PCA9655EE from ON Semiconductor and the MAXIM7311 from Maxim Integrated Products (Figure 23). The key feature of this last component is the capability to have 64 slave ID addresses available, this characteristic matches evidently with one of the objectives of BINMOV that is to recognize as many cards as possible allowing a large range for cards with different characteristics.

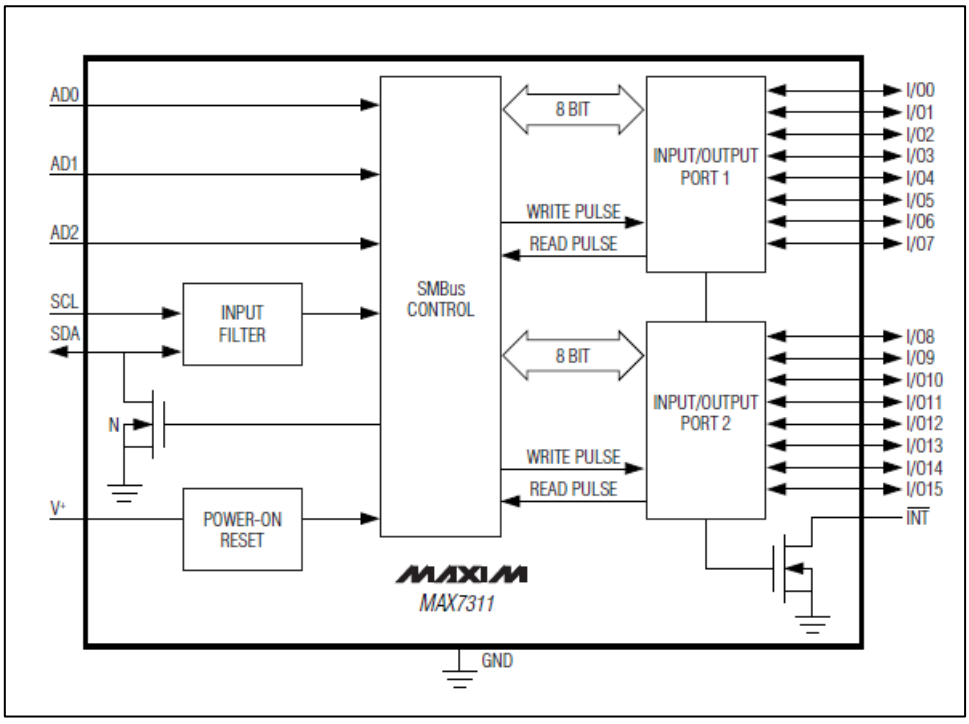

Figure 23. MAX7311 Block Diagram
(Maxim Integrated Products, 2005)

Therefore, a third solution is proposed to deal with card identification employing the MAX7311 expander. Its main characteristics are following stated.

- 400kbps I2C-Compatible Serial Interface
- 2V to 5.5V Operation
- 16 I/O Pins that Default to Inputs on Power-Up

- 64 Slave ID Addresses Available
- Low Standby Current (2.9µA typ)
- Open-Drain Interrupt Output (Maxim Integrated Products, 2005).

As show in Figure 24 the MAX7311 has a 7-bit-long programmable slave address trough 3 dedicated pins AD2 AD1 and AD0, these pins can not only be connected to Vcc or GND but also to SDA and CLK lines directly, that is the difference with the other presented components, and it is this difference which allows to handle 64 ID slave devices.

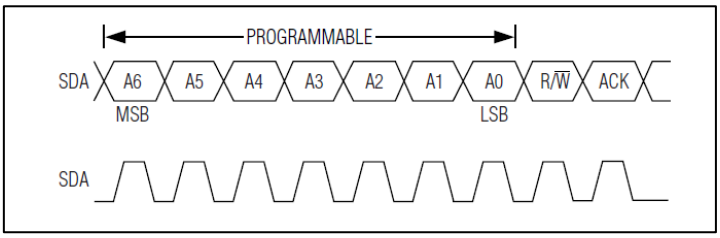

Figure 24. Slave Address
(Maxim Integrated Products, 2005)

An extrait of the address map is presented in Table 16 where we can notice that even we can attach pin A2, AD1 and AD0 directly to the clock signal CLK to assign the 0xB0 address to the device.

Table 16. Extrait MAX7311 Address Map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	ADDRESS (HEX)
SCL	**SCL**	**GND**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0xA0**
SCL	SCL	V+	1	0	1	0	0	0	1	0xA2
SCL	SDA	GND	1	0	1	0	0	1	0	0xA4
SCL	SDA	V+	1	0	1	0	0	1	1	0xA6
SDA	SCL	GND	1	0	1	0	1	0	0	0xA8
SDA	SCL	V+	1	0	1	0	1	0	1	0xAA
SDA	SDA	GND	1	0	1	0	1	1	0	0xAC
SDA	SDA	V+	1	0	1	0	1	1	1	0xAE
SCL	**SCL**	**SCL**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0xB0**

(Maxim Integrated Products, 2005)

The third digital proposal due to the large device handling and recognition capability was selected to be used for the card's identification in BINMOV project.

7. READ/WRITE 64 SELECTABLE DIFFERENT ADDRESSES TEST MODULE

To characterize the MAX3711 chip and to test the design functionality, and overall, the capacity to switch between 64 different addresses, a card with two main functionalities has been developed.

The first is the reading capability, using one the MAX3711 chip and a series of switch and resistors we will be able to read the state of the two port input lines through the I2C interface. This part of the test module also includes 3 different switches which allows the user select between the 64 different addresses by connecting V+, GND, SDA or SCL to the chip addresses pins A2, A1, and A0.

The second is the writing capability, another MAX3711 chip configured in writing mode will take the information from the I2C bus and set its output pins high or low according to the bits received.

7.1 Design

The general structure of the card is shown in the block diagram (Figure 25). The bottom part, the read module, employs a MAX3711 chip connected to the I2C bus lines and a series of manual switches that can be manipulated by the user to change the values of the address pins A2, A1, A0 so that the user can set one of the 64 available addresses to the device.

The write module also employs a MAX3711 chip with a fix address that will be used to control two multiplexers, one dedicated to modify the gain of the differential input signal and the second one dedicated to change the cutoff frequency of this differential signal.

The design suite used to design the schematic, to route and define components and patterns used in PCB layout is Dip Trace, a software employed for electronics projects in NOVATEM.

More detail about the circuit configuration and components used in these structures is presented in next sections.

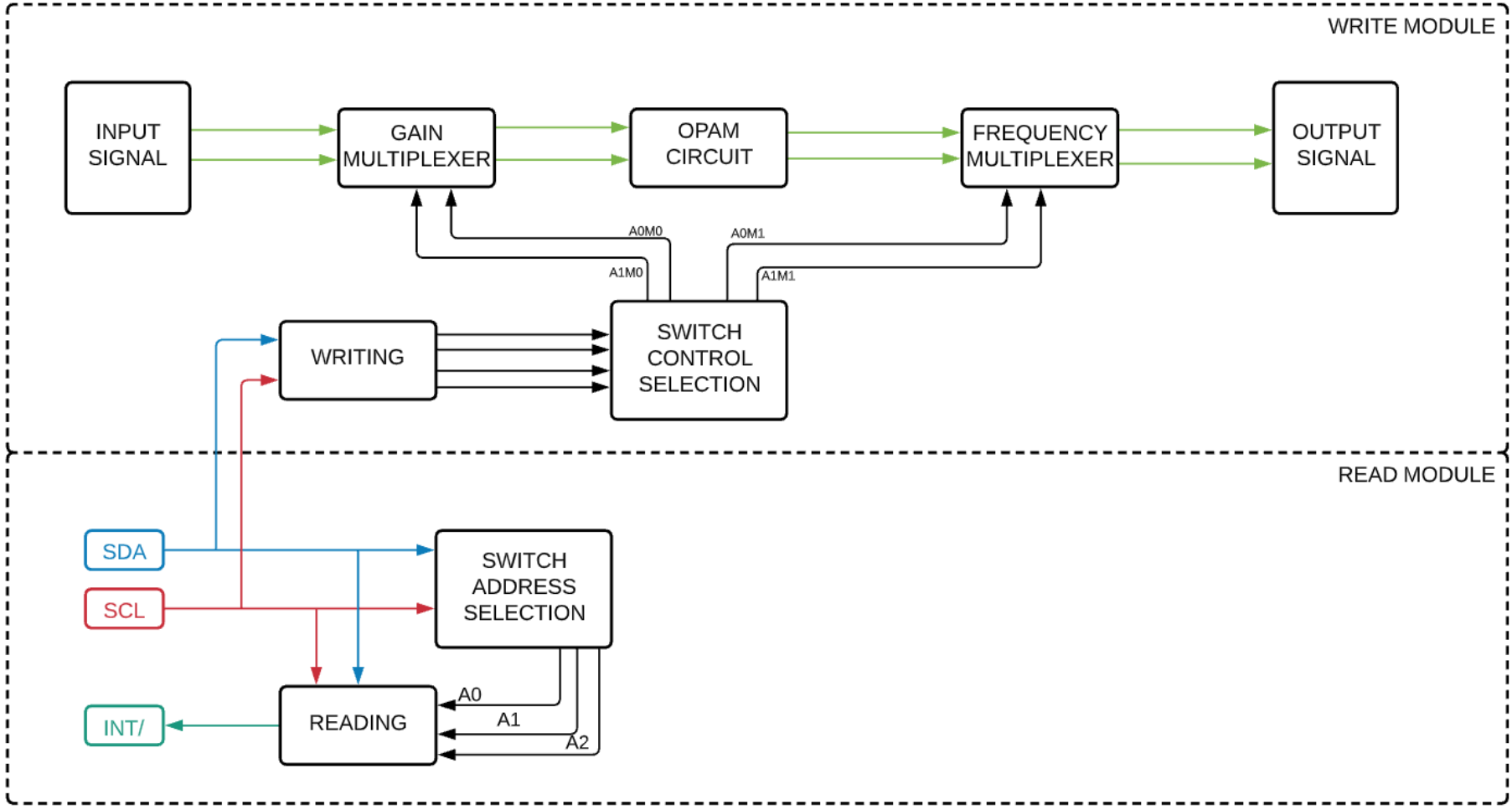

Figure 25. Test Module Block Diagram

7.1.1 Read Module

The electronics composing this module are showed in Figure 26. We can distinguish a MAX7311 as the main component in the module. The main purpose if this module is to test the reading capacity of the IC trough the I2C bus and to test the 64 different address assignations.

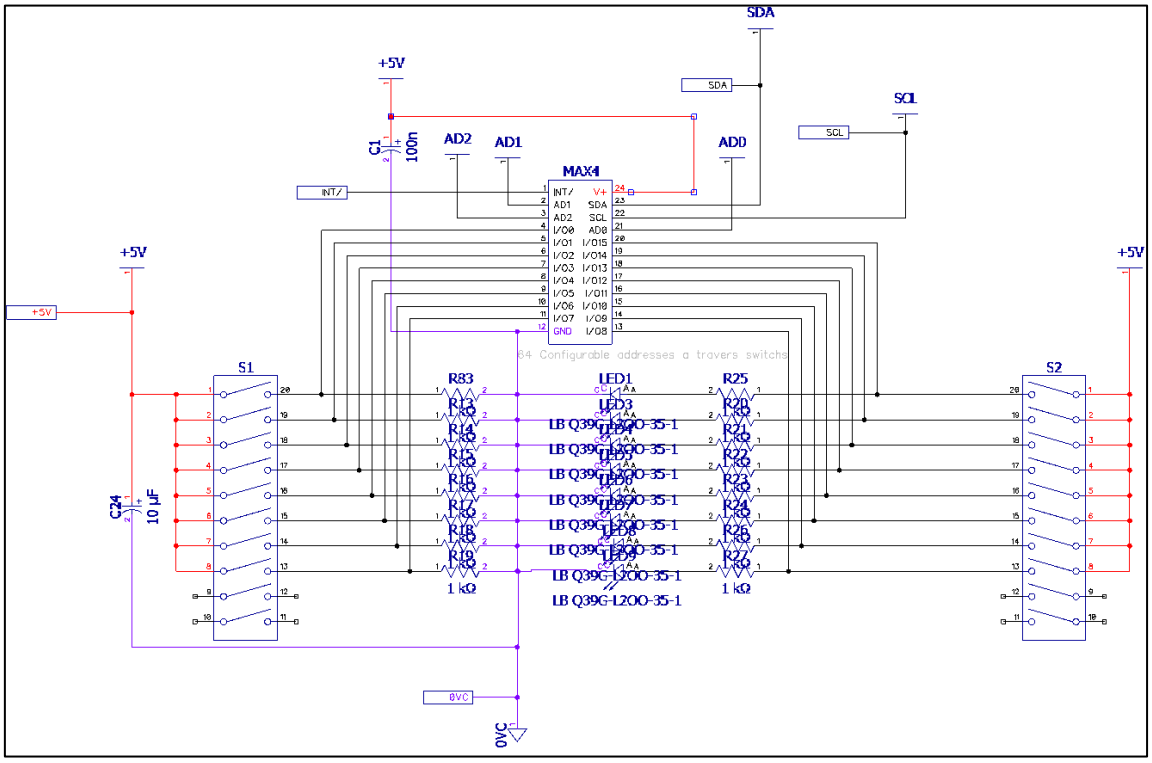

Figure 26. Read Module - MAX7311

The 2 bytes that this IC can read are generated by 16 pull-down resistors that are connected to each one of the MAX7311 input ports, then when switching S1 or S2 we can modify the input voltage level '+5V' or '0V' at the ports and evidently the byte that is going to be sent to Speedgoat through the I2C interface.

In the left port, there are also LED diodes used to indicate the state of the left input port, and they could show the state of the same port when configured as output, therefore the left port is used also to test the MAX7311 write capability.

The address selection is achieved by connecting A2, A1 and A0 pins to +5V, 0V, SDA or SCL lines, to do that, three switches are connected between the address pins and the lines (Figure 27), so by selecting one and only one line for each switch the address is assigned.

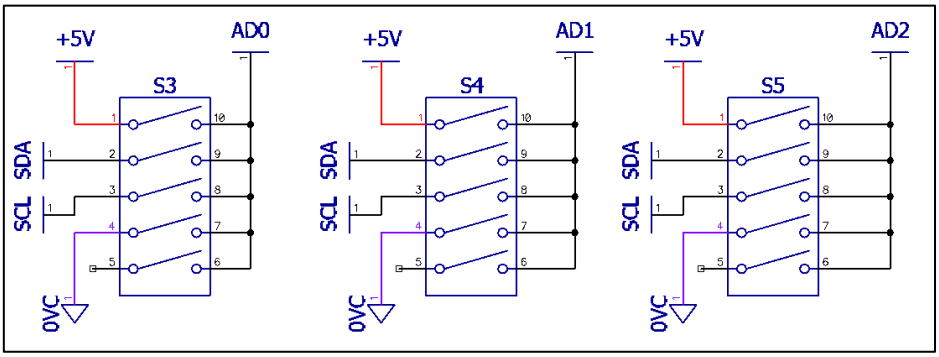

Figure 27. Read Module - Switch address selection

7.1.2 Write Module

This part consists of a MAX7311 with a fixed address whose 4 output pins are used to control two multiplexers charged to select the gain and the cutoff frequency of a differential input signal.

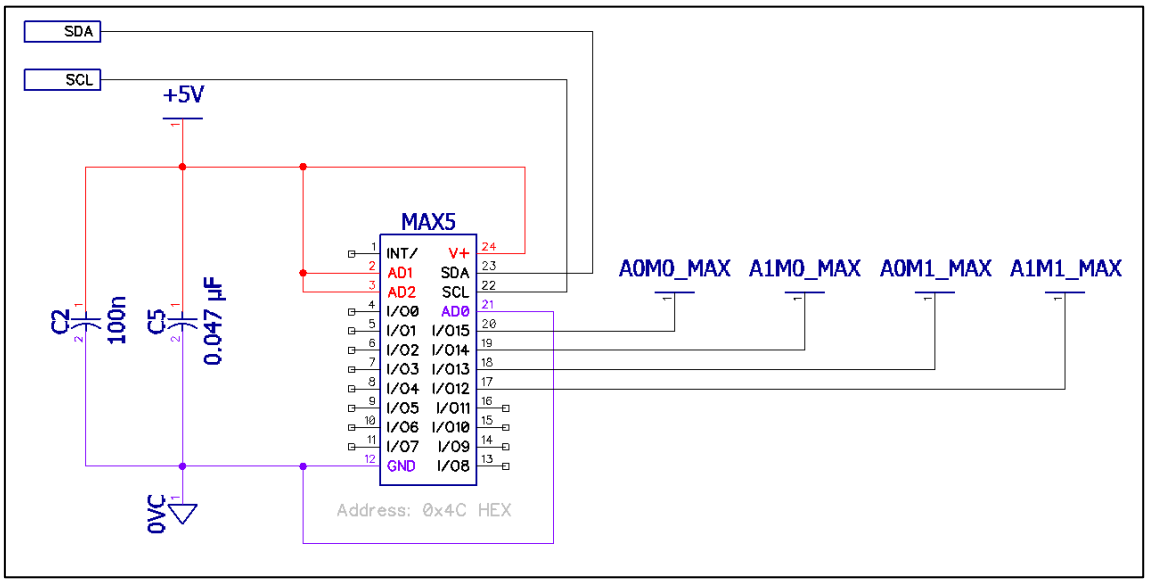

Figure 28. Write Module - MAX7311 MUX outputs

Parallelly to the progress of this internship, another was developed. To summarize briefly, its main contribution was the conceptualization of a generic filter function which allows filter any differential signal from the sensor outputs (Figure 29). This montage fully differential permits changer the cutoff frequency and the gain thanks to a series of resistors connected to a manual switch which are activated by the user according to the sensor characteristics as showed in Table 17.

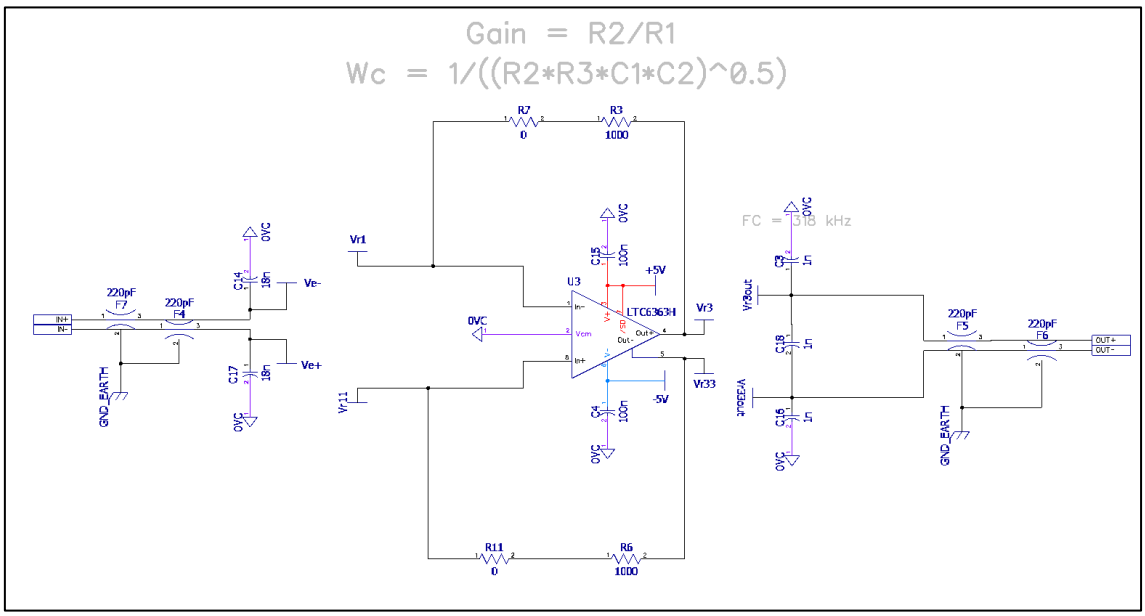

Figure 29. Second order Rauch structure

Table 17. Gain and cutoff frequency values

Gain	Resistance	S	A1	A0
1	1000	1	0	0
5	200	2	0	1
7	140	3	1	0
10	100	4	1	1

Fc	Resistance	S	A1	A0
300 kHz	180	1	0	0
50 kHz	1100	2	0	1
10 kHz	5100	3	1	0
1 kHz	51000	4	1	1

For the actual internship development this circuit is considered as a black box. So, what it was required was to integrate a solution that will allow select the different gain and cutoff frequency by controlling all the way through the Speedgoat.

The proposed solution was to introduce multiplexer to create programmable gain amplifier (PGA) structure (Figure 30). PGAs are most useful when an input sensor

signal needs to vary across different gain values to then be amplified to carry the signal into the next system component. A multiplexer allows for this switching between the different gain values thereby changing the level of amplifications

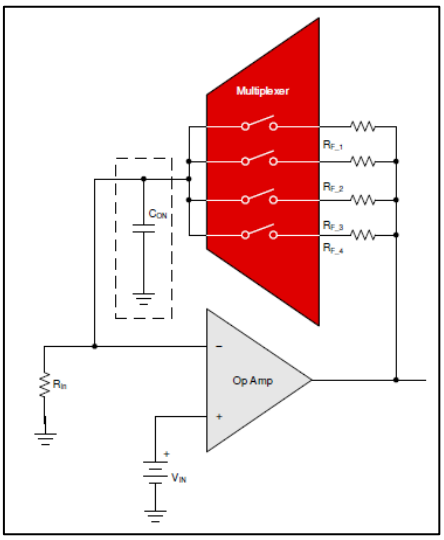

Figure 30. Circuit Model of Basic Discrete PGA
(Texas Instruments, 2020)

Therefore, the analog multiplexer ADG1409 from Analog Devices was selected to perform this task thanks to the 4.7 Ω maximum on resistance and the capability to drive four differential channels. The ADG1409 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1 (Analog Devices, 2016).

For instance, Figure 31 shows the multiplexer dedicated to select the gain, therefore just 2 bits are necessary two choose one of the 4 resistors, these bits come from

the MAX7311 when configured as an output device. A similar structure comprises the one used to select the cutoff frequency

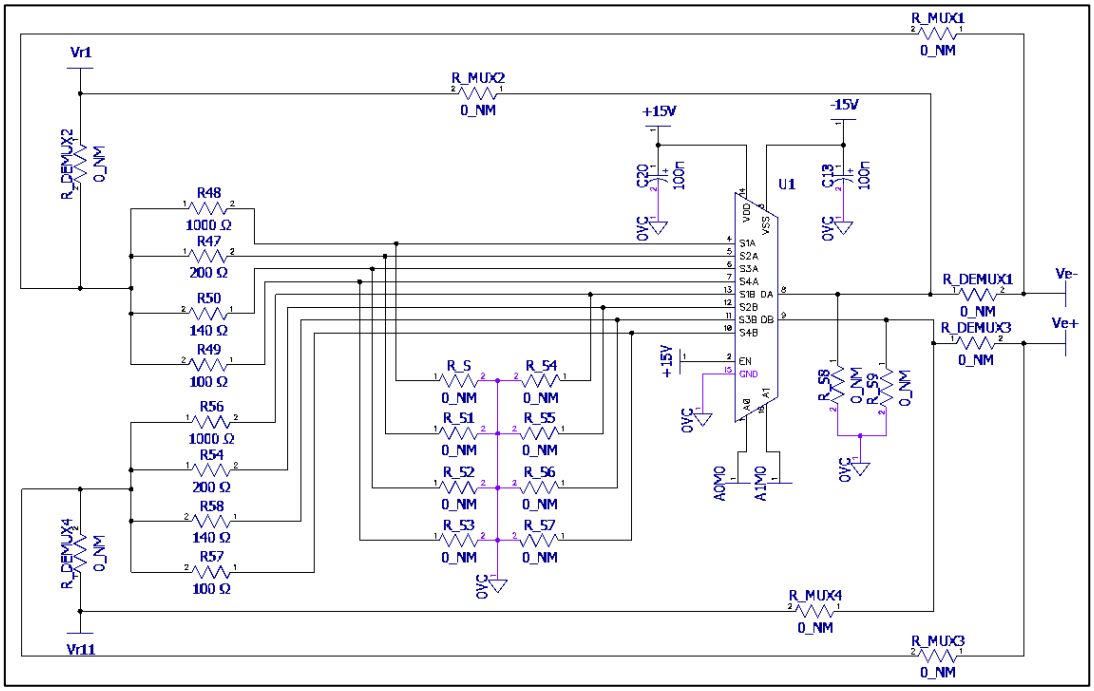

Figure 31. ADG 1409 implementation for gain selection.

The structure developed counts also with a series of switches that permits to debug the OPAM functionality just in case communications problems are detected, so these switches select the manual control or the Speedgoat control.

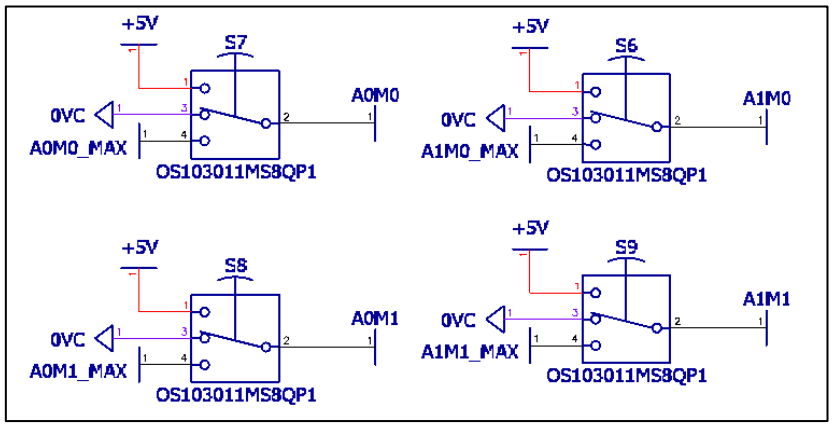

Figure 32. Selection control mode switches

7.2 PCB Creation

A prototype of the module was built to test the functionality. First it was necessary to develop the PCB routing before send the module to fabrication.

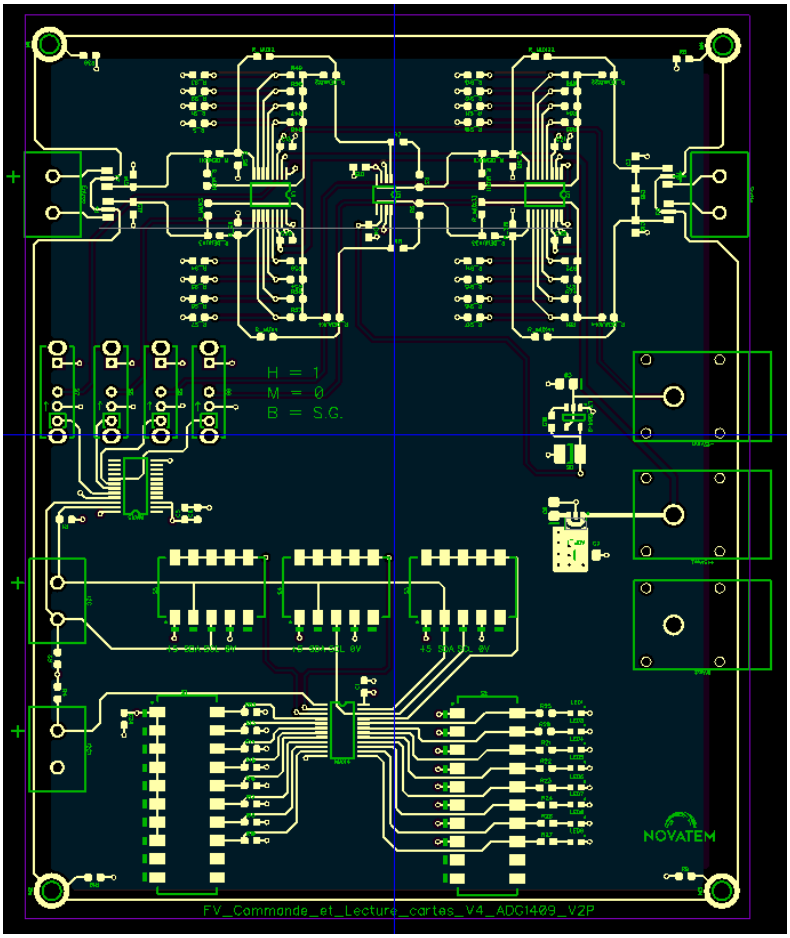

Figure 33. PCB Top view

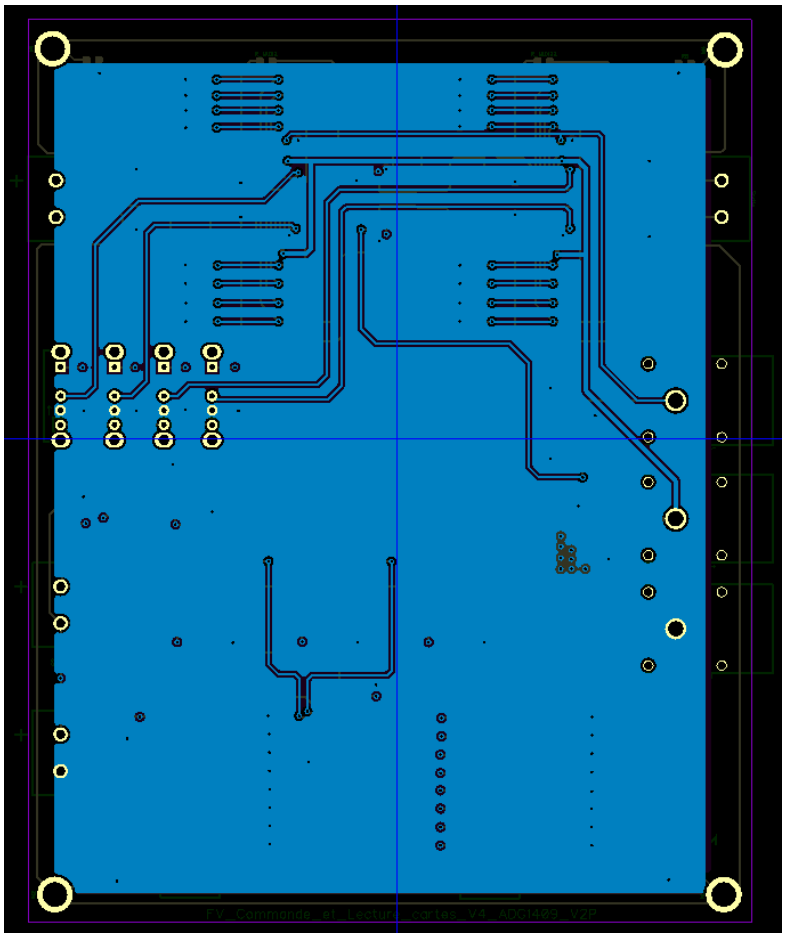

Figure 34. PCB Bottom view

Once the design checked it was sent to the foundry to be built, after one week approximately the PCB card looked like this.

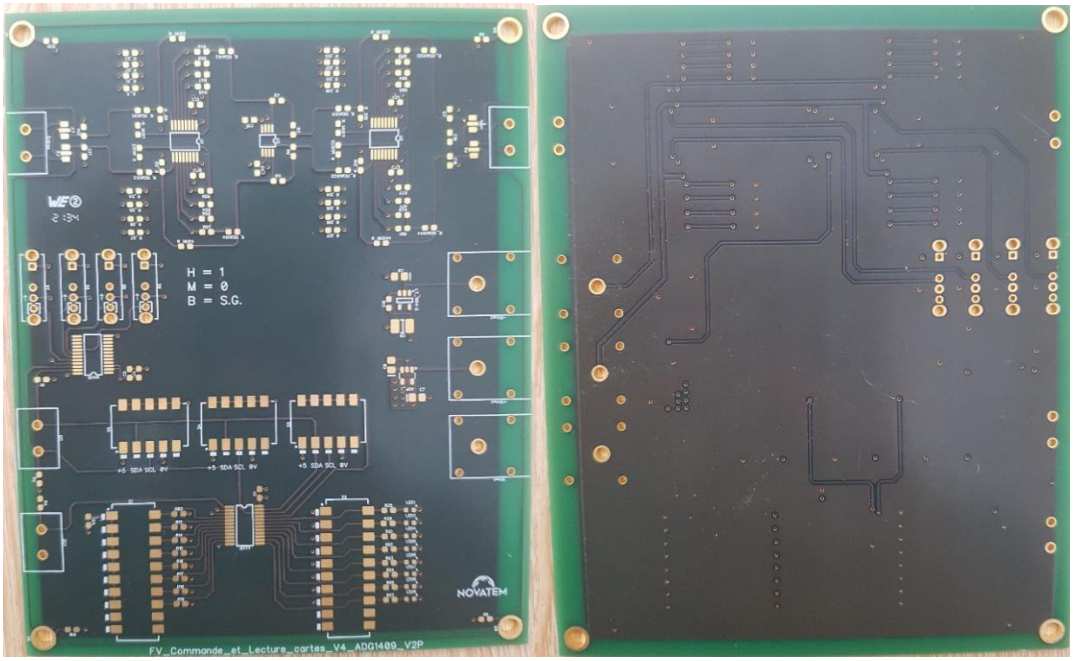

Figure 35. Real PCB

So, the work at NOVATEM was to prepare the welding and the components placement. First the silk screen machine TECPRINT 500 was employed to fill the traces

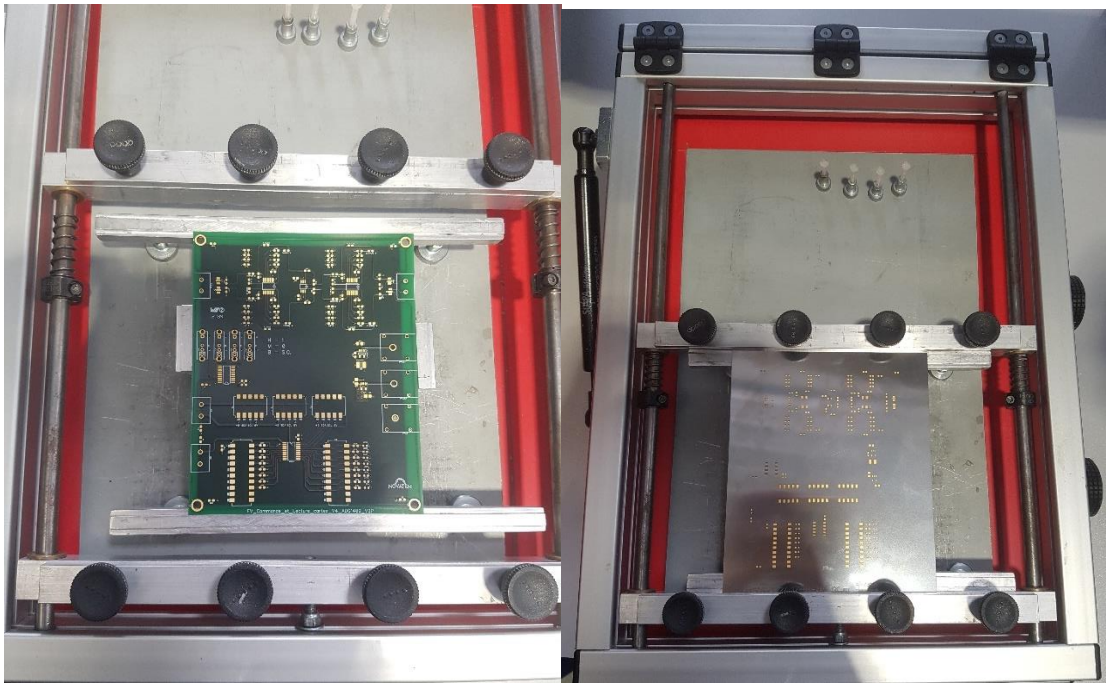

Figure 36. TECPRINT 500

Then, all components where placed thanks to EASYPLACER machine

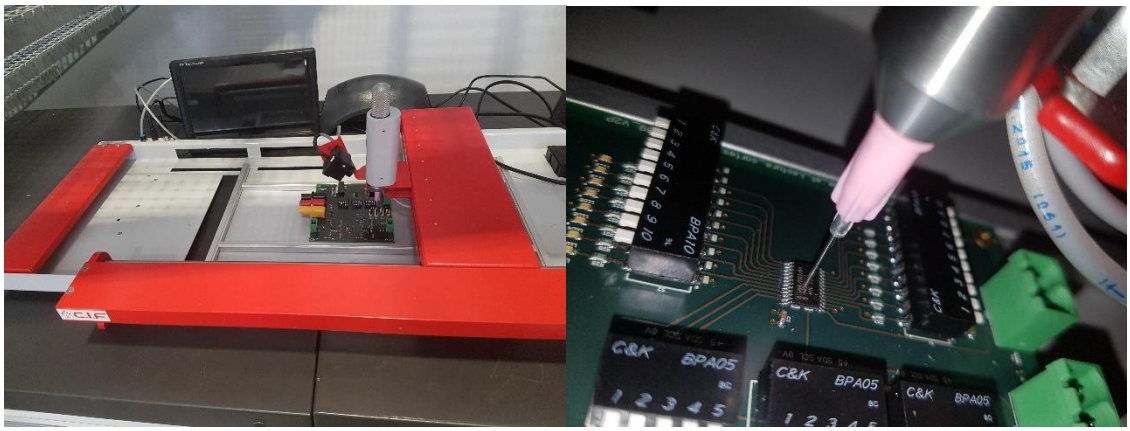

Figure 37. Components Placement

Then the PCB was sent inside an oven to complete the reflow soldering

Figure 38. Reflow oven

Finally, the rest of the components such as connectors, switches, alimentation pins were placed manually. Therefore, it is ready to begin the test phase.

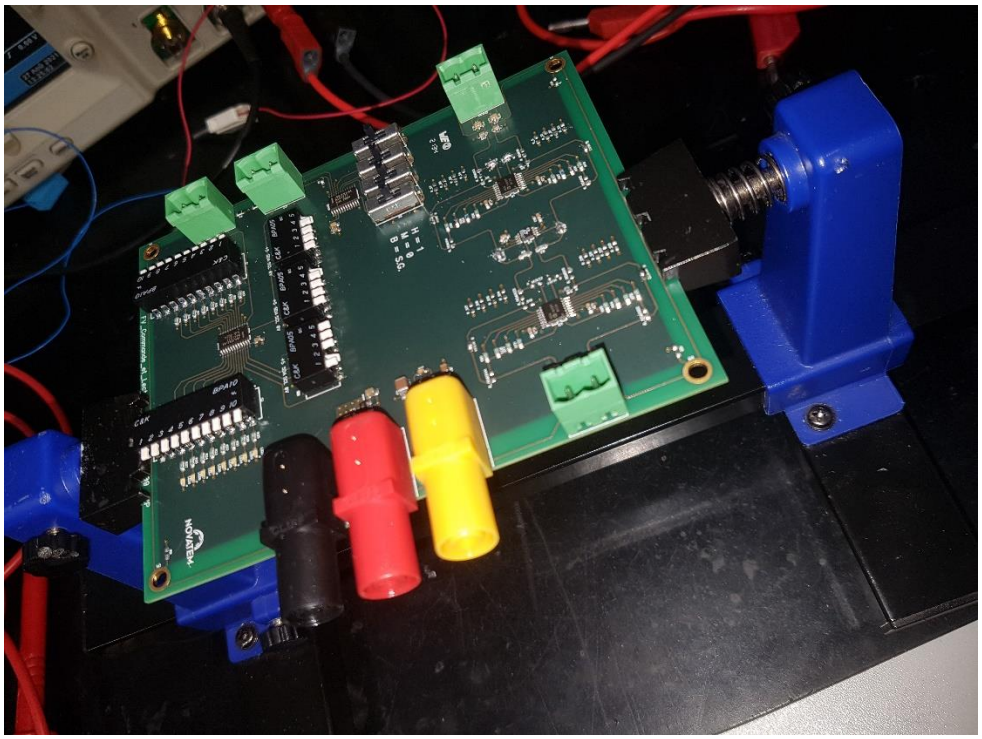

Figure 39. Final PCB module

8. DATA ANALYSIS

8.1 Testing

During the testing phase, two test were made, the first dedicated to validate the integration of the multiplexer stage to the OPAM circuit. This test will determine if the output signal changes according to the gain and cutoff frequency values selected.

The second test is used to check the communication trough the I2C bus between Speedgoat and the MAX7311 by reading the input ports of this last component.

8.2 Multiplexer Testing

The available equipment used in test were a function generator which sends the differential input signal to the card, a voltage source to feed all components and to control the power consumption and finally an oscilloscope with a differential proof used to look at the output signal

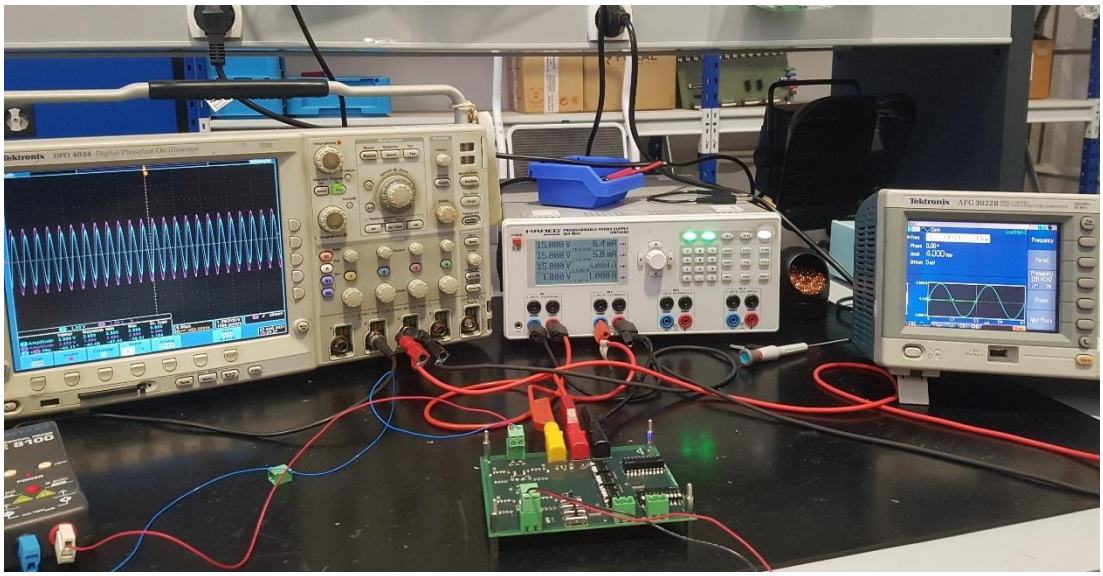

Figure 40. Multiplexer testing equipment

The test consisted of determining the phase and attenuation values for all gain and for all cutoff frequencies. The value selection is done by manipulating the switches according to Table 17

For a given gain at the cut off frequency the phase should reach as close as possible to -45° and the attenuation should be as close as possible to -3dB.

Gain	Frequency [kHz]	Phase [°]	Attenuation
1	300	-43.86	-2.38
	50	-43.59	-2.95
	10	-42.64	-3.085
$Vin_{PK-Pk} = 4\ [V]$	1	-44.87	-3.477

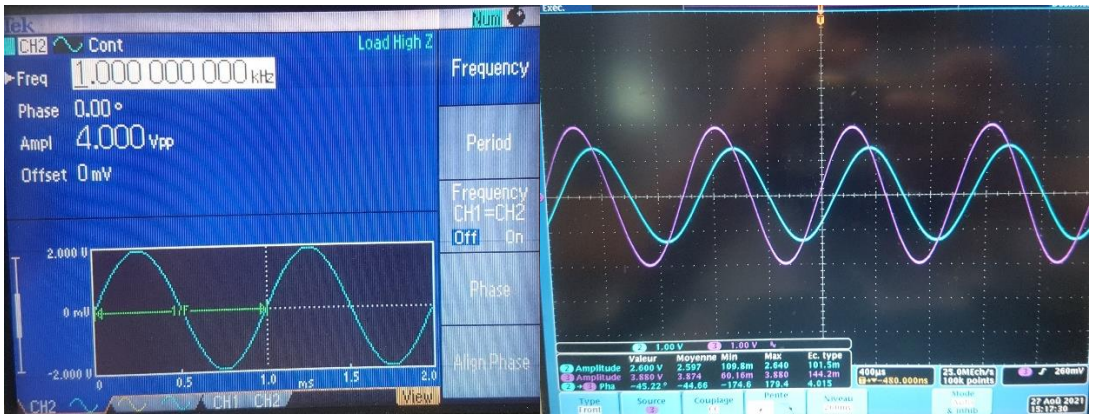

Figure 41. Waveforms for input and output signal when Vin pk-pk=4[V] at f=1 [kHz].

Gain	Frequency [kHz]	Phase [°]	Attenuation
5	300	-48.78	-1.82
	50	-43.74	-2.47
	10	-41.60	-2.69
$Vin_{PK-Pk} = 1\ [V]$	1	-44.42	-3.42

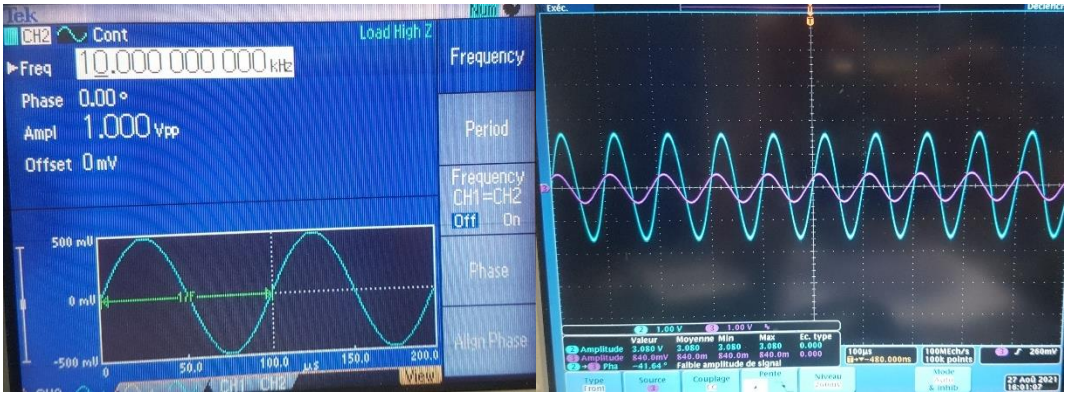

Figure 42. Waveforms for input and output signal when Vin pk-pk=1[V] at f=10 [kHz].

Gain	Frequency [kHz]	Phase [°]	Attenuation
7 $Vin_{PK-Pk} = 0.7\ [V]$	300	-45.19	-3.458
	50	-44.96	-3.53
	10	-42.74	-3.32
	1	-44.61	-3.25

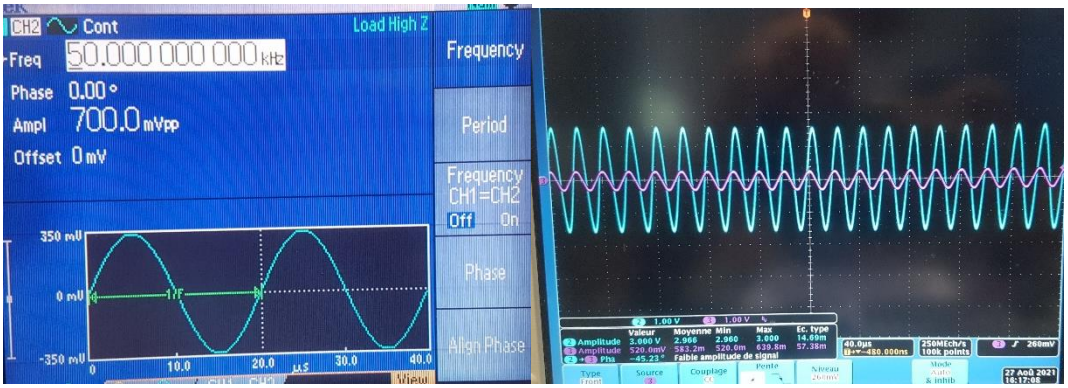

Figure 43. Waveforms for input and output signal when Vin pk-pk=0.7[V] at f=50 [kHz].

Gain	Frequency [kHz]	Phase [°]	Attenuation
10 $Vin_{PK-Pk} = 0.5\ [V]$	300	-46.56	-2.79
	50	-42.84	-4.36
	10	-39.88	-4.59
	1	-43.76	-4.03

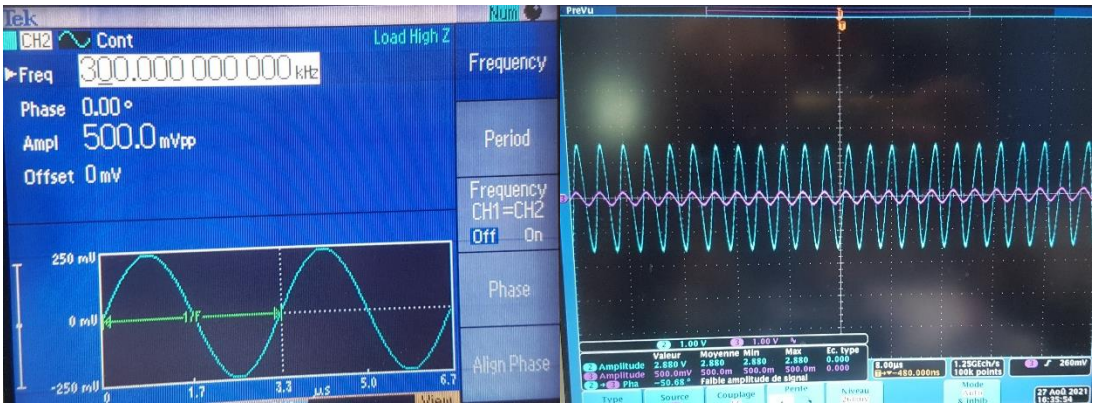

Figure 44. Waveforms for input and output signal when Vin pk-pk=0.5[V] at f=300 [kHz].

Looking at the retrieved values we can conclude that the multiplexer function works as expected, the values are not exact -3 dB or -45° but are close to them. These values are enough for the kind of signals that BINMOV's sensor will be handling.

One constraint found was that the input signal port is reversed, for next versions this consideration must be taken into account and corrected in the PCB routing, for the moment it was enough to invert the terminals of the input signal to resolve this problem.

8.3 I2C Testing

A protocol dedicated to stablish the message data frame was developed to test the I2C communication.

Adresse				Switchs Entrées																Resultat attendu														Clear register to enable port as output				Ecriture			
A2	A1	A0	HEX	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15	Slave Adress	R/W	Command Byte		Slave Adress	R/W	Command Byte	Data Port 1	Data Port 2
GND	GND	GND	0x40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0100000	0	00000111	00000000	0100000	0	00000011	00000000	00000000
GND	GND	GND	0x40	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	1	1	1	1	1	1	1	1	0100000	0	00000111	00000000	0100000	0	00000011	00000000	11111111
V+	V+	V+	0x4E	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0100111	0	00000111	00000000	0100111	0	00000011	00000000	00001111
V+	V+	V+	0x4E	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	0100111	0	00000111	00000000	0100111	0	00000011	00000000	11110000
V+	V+	GND	0x4C	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	X	X	X	X	X	X	X	X	1	0	1	0	1	0	1	0	0100110	0	00000111	00000000	0100110	0	00000011	00000000	10101010
V+	V+	GND	0x4C	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	X	X	X	X	X	X	X	X	0	1	0	1	0	1	0	1	0100110	0	00000111	00000000	0100110	0	00000011	00000000	01010101
V+	SCL	GND	0x28	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0010100	0	00000111	00000000	0010100	0	00000011	00000000	00001111
V+	SDA	GND	0x2C	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	0010110	0	00000111	00000000	0010110	0	00000011	00000000	11110000
V+	SCL	SCL	0x38	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0011100	0	00000111	00000000	0011100	0	00000011	00000000	00001111
V+	SDA	SDA	0x3E	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	0011111	0	00000111	00000000	0011111	0	00000011	00000000	11110000
GND	SCL	SCL	0x30	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	0011000	0	00000111	00000000	0011000	0	00000011	00000000	00001111
GND	SDA	SDA	0x36	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	0011011	0	00000111	00000000	0011011	0	00000011	00000000	11110000
SCL	SCL	SCL	0xB0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	1011000	0	00000111	00000000	1011000	0	00000011	00000000	00001111
SDA	SDA	SDA	0xBE	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	1011111	0	00000111	00000000	1011111	0	00000011	00000000	11110000
SCL	SDA	SCL	0xB4	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1	1011010	0	00000111	00000000	1011010	0	00000011	00000000	00001111
SDA	SCL	SDA	0xBA	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	0	1011101	0	00000111	00000000	1011101	0	00000011	00000000	11110000

Figure 45. Test protocol extrait

In this way it will be enough to connect the SDA, SCL lines and the GND from Speedgoat to the lines of the module card and then fill the preconfigured blocks in Simulink with the information above

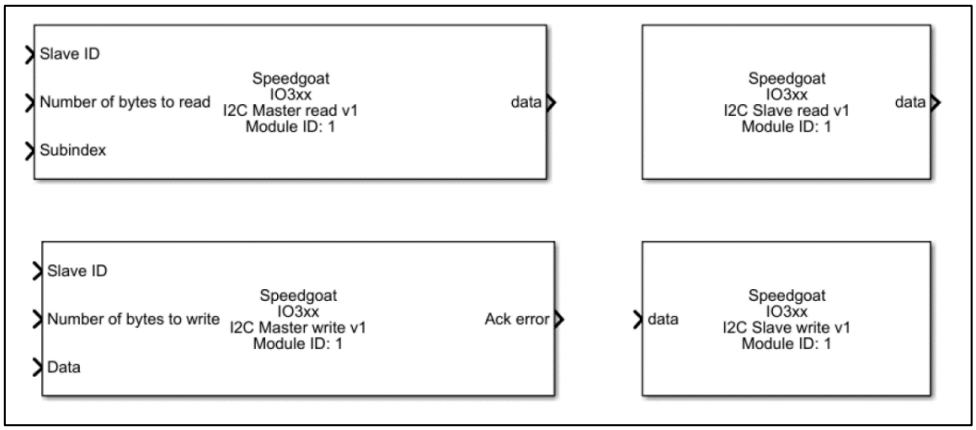

Figure 46. I2C Speedgoat Simulink Blocks

Once the connections stablished and the blocks programmed, the compiled program was running in Speedgoat however, there was neither clock SCL signal output nor data SDA output from Speedgoat. It was suspected that there was a problem with the

configuration modules or pin assignation in Speedgoat modules, since at the moment to run the default testing routine given by the fabricant, there was no signal return in the host PC

This test was performed in the last days of the internship development, unfortunately the I2C communication function could not be tested due to the detected technical problems.

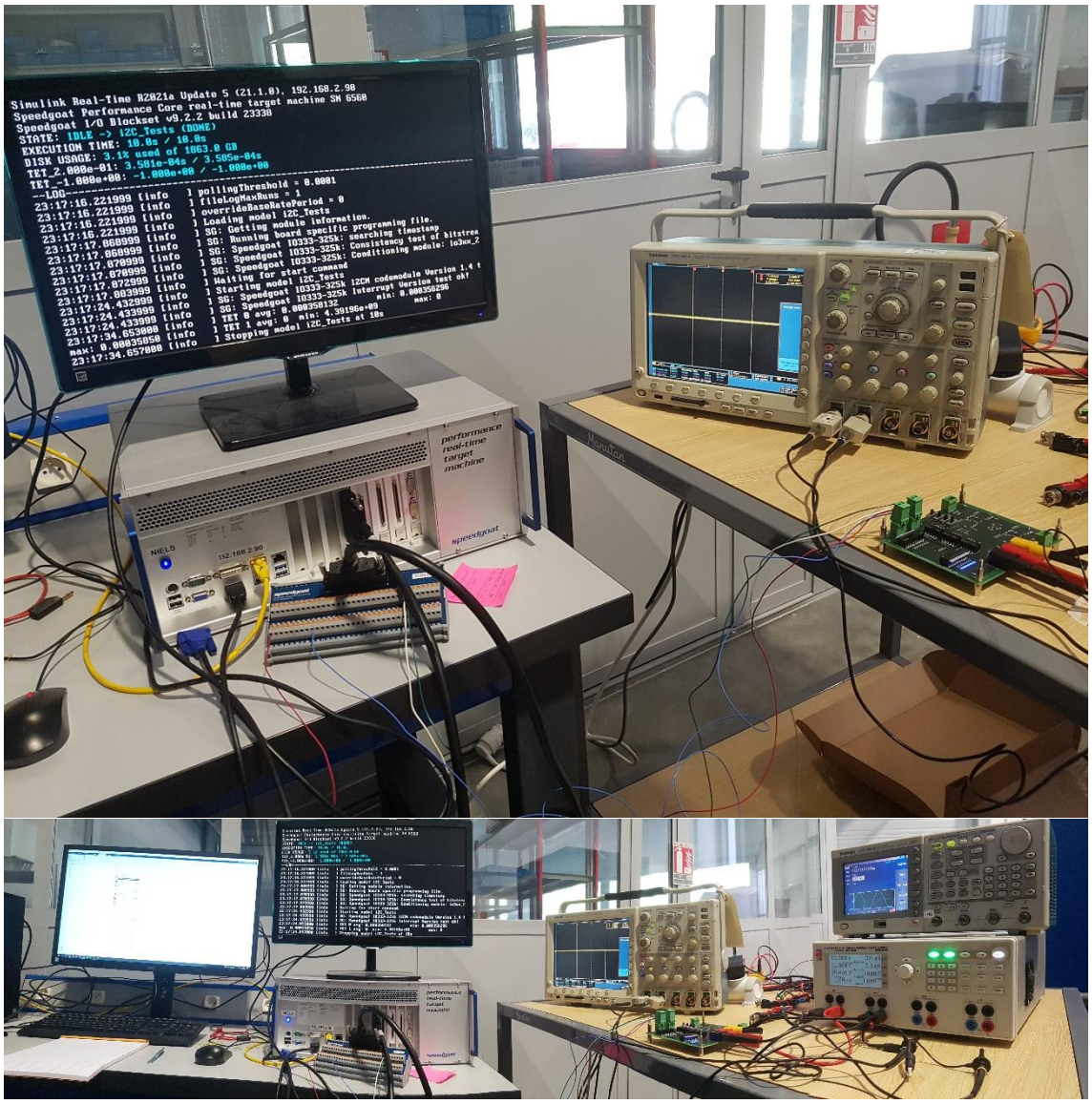

Figure 47. I2C Testing assembly

9. ACQUIRED COMPETENCES – AUTO EVALUATION

In the 6-month internship duration spent in NOVATEM I integrated a dynamic team of engineers and designers; this experience was very enriching for the development of my competences as engineer and the discovering of new ones. I could experiment what designing a real project feels like, knowing that each decision that I take will impact the work and the strategy of the design teams closest to me charged to develop next stages of the system design.

The key skills that I could develop also include the capacity to adapt myself to last minute changes, sometimes all work of a week should be replaced with a complete new one, this led me to develop my creativity by facing the same problem but this time with another point of view and creating a new strategy.

I could experiment how a real project is managed and divided in several teams, I learnt best to organize the assigned task development so that the results could be ready to be use by another design team.

NOVATEM is a full french-speaking environment, so I could learn a lot of vocabulary related to engineering, also I had the opportunity to write several reports in french which allowed me to develop my competences in this langue.

10. GENERAL CONCLUSION

BINMOV is an ambitious project that pretends simplify the testing stage of the developed new devices, during its conception I have participated in the creation of the core module that allows the communication between the Testing machine – Speedgoat and the final mechatronics devices under test. This stage involves having a global vision of what the system is required to do to develop all necessary electronics that will provide BINMOV all desired features. Each decision taken impacts directly on how the control and monitoring signals are going to be transmitted and collected and this, in turn, affects the whole structure of the system.

Participating in the development of BINMOV has given me the opportunity to face real world applications, I could apply all knowledge I learnt during my engineering formation and also the new skills learnt during the second year of master ESECA. I could design and conceive real solutions to real problems; this let me acquire more experience and overall gives me more confidence on my competences as engineer.

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12. ANNEXES INDEX

ANNEX 1 – CIRCUIT DIAGRAMS