# UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

**Colegio de Ciencias e Ingenierías**


## Design of a memristor-based Content Addressable Memory (CAM) using Verilog-A models

.


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**Ingeniería Electrónica y Automatización**


Trabajo de fin de carrera presentado como requisito
para la obtención del título de
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**HOJA DE CALIFICACIÓN**
**DE TRABAJO DE FIN DE CARRERA**

## Design of a memristor-based Content Addressable Memory (CAM) using Verilog-A models

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## RESUMEN

Las ReRAM son un tipo de componente de almacenamiento no volátil que funciona cambiando su impedancia según la corriente aplicada en sus terminales. Por lo tanto, al configurarlo en un estado de baja resistencia (LRS) o un estado de alta resistencia (HRS), es posible almacenar información en un circuito que utiliza su impedancia para dictar la corriente y el voltaje de salida. Por esta razón, las ReRAM se pueden utilizar en circuitos lógicos de memoria, como la memoria direccionable por contenido (CAM). Dado que las memorias modernas utilizan transistores para almacenar información y los transistores son componentes volátiles, el consumo de energía es alto en el día a día. Sin embargo, si la información se almacena en una ReRAM, que se implementa en una CAM, entonces el consumo de energía para mantener la información almacenada disminuirá. Para hacer esto, se creó un modelo de memristor en Verilog-A para simular mejor el comportamiento analógico de una CAM basada en ReRAM. Este modelo se calibró con datos experimentales de una ReRAM de 85 nm con óxido de grafio, utilizando como base un modelo en LT-SPICE. Con esta tesis se diseño y simulo una TCAM simple de 2-palabras con 2-bits, las cuales utilizan tecnología ReRAM, con lo cual se demuestra que la tecnología ReRAM de 85 nm es viable en la creación de memorias TCAM.

**Palabras clave:** ReRAM, CAM, Verilog-A, memristor, CMOS, transistores

## ABSTRACT

ReRAMs are a type of non-volatile storage component that operates by changing its impedance according to the applied current in its terminals. Therefore, by setting it in a Low Resistance State (LRS) or High Resistance State (HRS) it is possible to store information in a circuit that uses its impedance to dictate output current and voltage. For this reason, ReRAMs can be used in memory logic circuits such as a Content Addressable Memory (CAM). Since modern memories utilize transistors to store information, and transistors are volatile component, the power consumption is high in a day to day basis. However, if information is stored in a ReRAM, which is implemented in a CAM, then the power consumption to maintain the stored information will decrease. To do this, a memristor model was made in Verilog-A to better simulate the analog behaviour of a ReRAM based CAM. This model was calibrated using Hf-based ReRAM experimental data from a previously calibrated LT-SPICE model of 85nm ReRAM technology. In this thesis a simple 2-bit 2-word TCAM using ReRAM technology was made and shown to work, proving 85nm ReRAM technology can be used to make TCAM memories.

**Key Words:** ReRAM, CAM, Verilog-A, memristor, CMOS, transistors

# TABLE OF CONTENT

**FIGURES INDEX**

# INTRODUCCIÓN

Content-Addressable Memory (CAM) is a kind of memory which contains stored information in a word-array (a word is a set of bits which form stored data). The CAM will compare the input data against the stored words in the memory, and return the address in which the data is stored, all in a single clock cycle [8]. This is unlike most common memories, such as Random-Access-Memory (RAM), Fist-In-First-Out (FIFO) and Last-In-Last-Out (LIFO), which uses an input address to return information stored in said address. This allows for CAMs to be highly effective in data-intensive applications that involve the searching and matching of large amounts of data, which in turn makes it one of the most used memory types in storing information in multimedia processing, big data analytics and the internet [12].

Most modern CAMs are fabricated using Complementary Metal-Oxide-Semiconductor (CMOS) based technology, which has a high-density and low-cost in the chips produced. However, with the quick downscaling of CMOS technology, this has led to various challenges in large storage circuits such as CAMs. The most critical of these challenges is the CMOS memories leakage in the nanometric scale [9]. Alongside leakage currents, CMOS technology is a volatile, which means that unless it is “refreshed” periodically, the information stored in it will be lost [1]. Common CAMs are made using Static Random-Access Memories (SRAMs), which are made of around 16 transistors only to make a single CAM cell. This in turn increases the area of a CAM cell and its power consumption [12]. Since SRAM cells are used for storage of information, which means the search and return functions of the CAM are done using a different chip from the SRAM, adding more power consumption and area to the final chip [9].

A variant to the usual CAM cell is the ternary content addressable memory (TCAM) cell.

Unlike the CAM cell which only saves a one or zero bit, the TCAM also saves a don't care (X) state [3]. The TCAM cell has two operations, a writing operation and a reading or searching operation, though as the TCAM is mainly used for storage it rarely uses the writing operation [8].Resistive Random-Access Memories (ReRAMs), also known as memristors or memdiodes [7], are one of the new emerging technologies used to overcome these limitations. TheReRAM is capable of storing information in a nonvolatile waythrough its hysteric switching behavior between two stable states, the High Resistive State (HRS) and Low Resistive State(LRS) [2,6]. This is done through two processes known as SETand RESET. When going through the SET process the ReRAMwill change to a LRS, while the RESET process will changeit to a HRS [4]. Furthermore, ReRAM technology has high endurance and high retention time aspect, making it possible to downsize it to the nanometer scale [2].

Resistive Random-Access Memories (ReRAMs), also known as memristors or memdiodes [7], are one of the new emerging technologies used to overcome these limitations. The ReRAM is capable of storing information in a nonvolatile way through its hysteric switching behavior between two stable states, the High Resistive State (HRS) and Low Resistive State (LRS) [2,6]. This is done through two processes known as SET and RESET. When going through the SET process the ReRAM will change to a LRS, while the RESET process will change it to a HRS [4]. Furthermore, ReRAM technology has high endurance and high retention time aspect, making it possible to downsize it to the nanometer scale [2].

A common topology used when working with memristors is the one-transistor-one-resistor (1T1R). With this topology the transistor is used to control the resistive-state changes [1]. This topology is used for its decreased error rate, provided by the transistor controlling the current flow of the memristor, but at the cost of a of additional area and

power consumption [1,11]. To make a Ternary Content Addressable Memory (TCAM) cell, a 2T2R topology is used, which is the combination of two 1T1R cells that share a common source. This way, it is possible to store and read a bit and its complementary-bit easily [3,11].

## MODEL AND METHODS

### Review of ReRAM memristors

The SPICE model used in this thesis was originally made by Enrique Miranda [6]. His model was made considering the equivalent circuit of two anti-parallel diodes with hysteric properties with a resistance in series with this connection (see Fig. 1) [6]. The variable impedance of the memristor is determined by the applied voltage to either of the poles. Then, if the voltage reaches its threshold for either SET or RESET, the impedance of the ReRAM will change to LRS or HRS respectively [4,6,9].

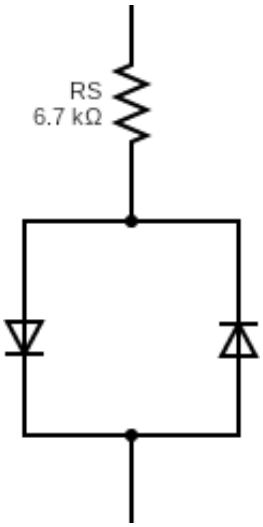


Fig. 1. Equivalent circuit using anti-parallel diodes to represent a memristor

Considering Miranda's model, in order to correctly model the ReRAM model, the only equation needed is that of two diodes in parallel, and this equation in turn is affected by the memory state equation based in a hysteresis operator [6].

$$I = \mathrm{sgn}(V_D) \cdot ((\alpha R_S)^{[} - 1]W\,(\alpha R_S I_0(\lambda)\exp(\alpha\,\mathrm{abs}(V_D) + R_S I_0(\lambda)) - I_0(\lambda)) \quad (1)$$

In equation 1 the current for the parallel diodes is shown, where (sgn) is a sign function and (W) is a Lambert function. The variables α is a constant, while $R_S$ is the internal series resistance. Furthermore, VD is the voltage drop in the memdiode and (I) is the diode current amplitude.

$$\lambda(VD) = \min(\Gamma^{-}(VD), \max(\lambda(VD\leftarrow), \Gamma^{+}(VD))) \quad (2)$$

In equation 2, λ is a control parameter that runs between 0 and 1 to determine the state of the memristor. For this a minimum, maximum and ridge functions are required to function properly [6]. This model is then calibrated with experimental data for an 85 [nm] ReRAM presented in [7] (see Fig. 2).

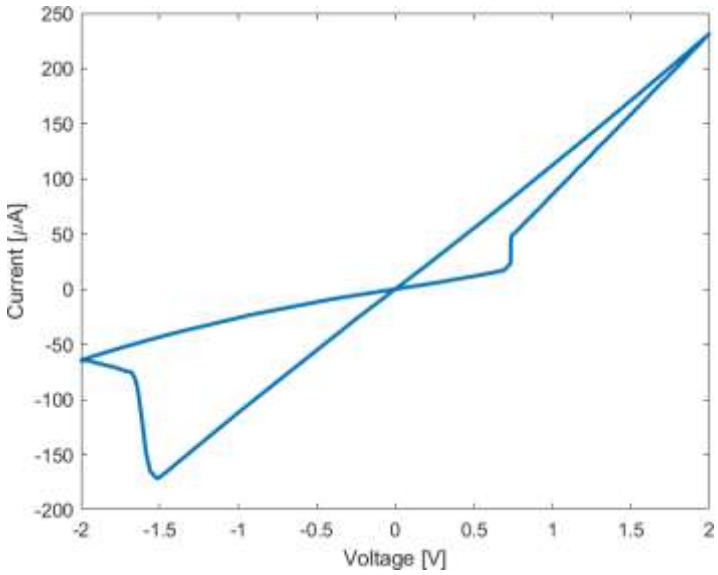


Fig. 2. Verilog-A simulated ReRAM memristor of 85 [nm] technology. The model shows the characteristic IV curve for an HF-based ReRAM

**Verilog-A Modeling**

While SPICE models are useful and widely used in many programs, Verilog-A is the standard when it comes to analog simulations. This language is used for both behavioural with a high level of abstraction as well as detailed models for semiconductor devices. While using Verilog-A it is important to consider it is based in the (C) programming language, meaning it will execute its modules and instructions in a top-down order [10].

In Figure 3 the Verilog-A code for the memristor calibrated with 85 [nm] data is shown. In this model the memristor has two poles, (plus) and (minus), which work both as an input and output port, therefore having the (inout) label. The (H) and (out) port are the ports to measure the memory state and inside current respectively of the memristor. However, this are used solely to help calibrate and test the ReRAM, and therefore are only (output) ports.

Considering Verilog-A simulates the behaviour of the analog circuit, in this case the memristor model, some functions will not work exactly as in the SPICE model presented in [6]. In this case, the sign (sgn) function does not change directly between the possible values of (-1), (0) and (1), and instead uses an exponential function to change between these values. Also, in Figure 3 both equations 1 and 2 are presented as the variables BH and BF respectively. The rest of equations are part of the model presented in [6].

The results of the calibration of the Verilog-A model can be seen in Fig. 2, where both the SET and RESET have been calibrated according to experimental values [7]. To do so, it is necessary to calibrate it using a simple circuit as seen in Fig 3, which uses an external resistance to better simulate the series resistance of the memristor [6].

```
`include "constants.vams"
`include "disciplines.vams"

module ReRAM_PRUEBA2 (plus, minus, H, out);
        inout plus;
        inout minus;
        output H, out;
        electrical plus, minus, H, out;

        parameter real ion = 6e-4, aon = 2, ron = 1;
        parameter real ioff = 0.5e-6, aoff = 0.56, roff = 1;
        parameter real vset = 0.62,  vres = -0.35;
        parameter real nset = 18, nres = 3.3;
        parameter real ISB = 2.31e-5, VT = 0.45;
        parameter real kset = -1, kres = 1;
        parameter real H0 = 0, RSS = 1;
        parameter real RPP = 1e10, CH0 = 1e-3;

        //Internal Variables
        real y = 0, R = 0, S = 0;
        real BH = 0, CH = 0, sgn = 0;
        real result0 = 0, result1 = 0, result2 = 0;
        real result3 = 0, x = 0, BF = 0;

    analog begin

        if(BF <= ISB) begin
                y = vset;
        end
        else begin
                y = VT;
        end
        R = 1/(1+limexp(1.702*ln(1-kres*nres*(V(plus,out)-vres))/kres));
        S = 1/(1+limexp(1.702*ln(1-kset*nset*(V(plus,out)-y))/kset));
        BH = min(R, max(S,V(H))); //0 - H
        CH = CH0 * ddt(V(H)); //H - 0
        V(H) <+ (BH - CH) * 1;

        sgn = 2 * (1/(1+exp(-100*V(plus,out)))) - 1;
        result0 = aon * V(H) + aoff * (1-V(H)); //a(V(H))
        result1 = ron * V(H) + roff * (1-V(H)); //RS(V(H))
        result2 = ion * V(H) + ioff * (1-V(H)); //I0(V(H))
        x = result0 * result1 * result2 * limexp(result0 * (abs(V(plus,out))+result1*result2));
        result3 = abs(ln(1+x)*(1-(ln(1+ln(1+x)))/(2+ln(1+x))));

        BF = sgn * (1/(result0 * result1) * result3 - result2);
        I(plus,out) <+ BF;
        V(out,minus) <+ BF*RSS;


    end
endmodule
```

Fig. 3. Verilog-A simulated ReRAM memristor of 85 [nm] technology. The model shows the characteristic IV curve for an HF-based ReRAM

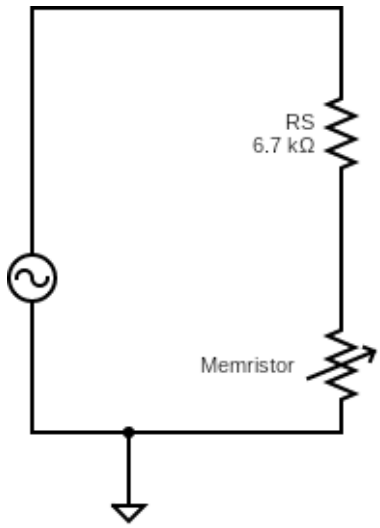


Fig. 4. Schematic for the calibration of the memristor using a single series resistance and a sinusoidal input voltage source.

**Proposed TCAM Cell Design**

Any TCAM cell should be capable of two basic operations. The first is the writing operation, though rarely used it is convenient in order to simplify the installation process of the memory by preventing the need of pre-charged memristors (meaning they are already set in their resistive state). This will be done through both the SET and RESET process. The second operation is that of reading/searching the saved bits. In this case the impedance will not be changed, but will be displayed if the ReRAM is in HRS or LRS [3,8,11].

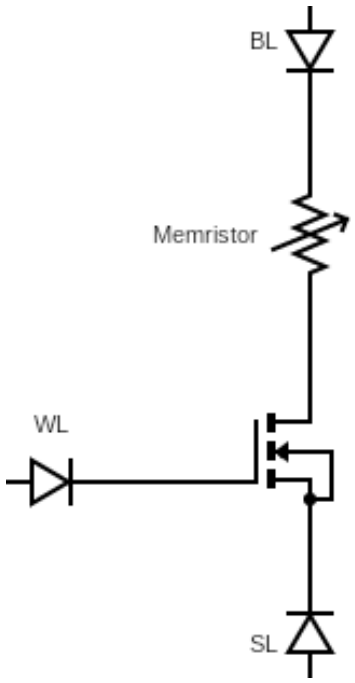


Fig. 5. Basic 1T1R cell used to further construct the TCAM cell [1,3]

In case of the TCAM using ReRAM technology, the first component of its cell is the 1T1R topology (see Fig. 5). While technically a memristor should be capable of storing the information by itself, the possibility of sneak currentsor disturbances in its operations mean that the state of the ReRAM could change unnecessarily [1]. The 1T1R architecture itself gives a higher reliability to the usage of ReRAM technology when mixing it with CMOS technology. By usinga transistor to control the current and voltage in one of the memristors' terminal it is harder for a disturbance or sneak current to change its resistive state by accident [3]. However, this is offset by an increase in area for each memristor used, which in turn increases the power consumption of the circuitas a whole [11].

The 1T1R topology (see Fig. 5) is capable by itself of doing both of the TCAM basic operations. In Figure 5 three lines are connected to the 1T1R. This are the Bit-Line (BL), Word-Line (WL) and Source-Line (SL) [3,11]. To be capable of either reading or writing in the 1T1R topology, the WL must have a voltage high enough to turn-on the NMOS. To write an LRS through the SET process, the BL should have the appropriate voltage while the SL should be grounded. Similarly, to write an HRS though RESET the BL should be

grounded while the WL and SL have their appropriate voltage. Finally, for the read operation the SL should be grounded, while the WL and BL should use lower voltages to prevent the switching of the resistive state of the ReRAM [1,3,5].

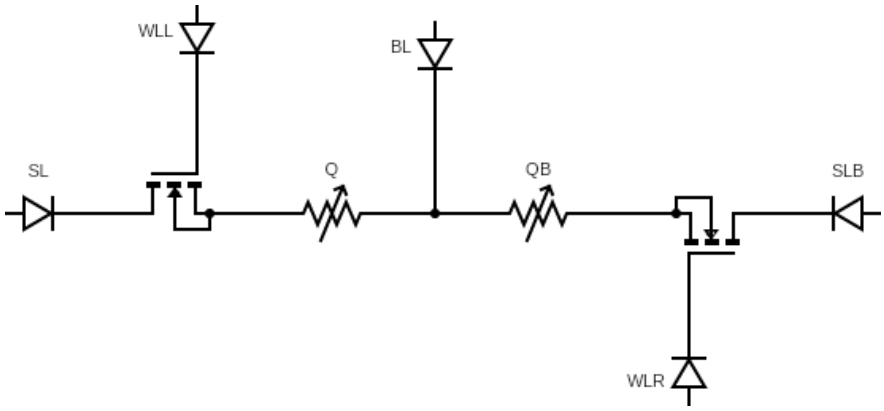


Fig. 6. 2T2R bit-cell used as basis of TCAM cell [3, 11]

By using two 1T1R together, it is possible to make a 2T2R topology that can work as a TCAM cell as well. By sharing a common BL, the 1T1R cells will become complementary to one another (see Fig. 5). Therefore, by changing the resistive states of each memristor it is possible to save and later read the logic state of the cell as a whole [3]. In Figure 6, the 2T2R bit-cell has both a Q and QB memristor. The Q memristor is the bit which the memory is holding. However, to better safeguard the information a complementary-bit is saved in memristor QB. Therefore, by activating the WL and SL of each memristor individually (as well as the shared BL) it is possible to place either of the ReRAM in HRS or LRS by going through multiple cycles in the writing process [3,11].

The 2T2R bit-cell can store a zero logical state, a one logical state or a don’t care logical state. This is done by considering that when a ReRAM is in HRS, the memristor is storing a one logical state. Therefore, for a 2T2R bit-cell to be storing a zero logical state its (Q, QB) memristors should be in a (LRS, HRS) resistive states respectively. Therefore, a one logical state has its (Q, QB) memristors in a (HRS, LRS) resistive states respectively and a don’t care state would have both ReRAM in HRS [3].

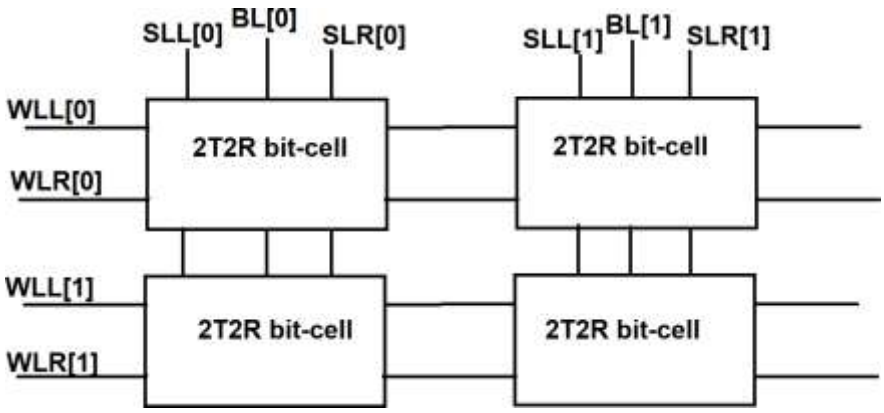


Fig. 7. 2T2R array for 2-bit 2-word TCAM memory[3, 11]

Once the 2T2R bit-cell is made, it is possible to make the TCAM by combining various 2T2R bit-cells. This is done by making an array of 2T2R bit-cells, in which the rows can be Once the 2T2R bit-cell is made, it is possible to make the TCAM by combining various 2T2R bit-cells. This is done by making an array of 2T2R bit-cells, in which the rows can be considered the bit number, while the column would be the word saved in the TCAM. In Figure 7 a 2-bit 2-word TCAM memory is shown, where each word shares a BL and the SL of both its memristors; while each bit shares the WL of their memristors.

## RESULTS AND DISCUSSION

The TCAM simulations made in this thesis are made with 85 [nm] ReRAM technology calibrated with experimental data [7]. In order to keep it similar in scaling to its complementary CMOS technology 90 [nm] NMOS transistors were used as well. However, this in turn opens up the optimization of both energy consumption and speed of the TCAM. Therefore, it is necessary to consider the optimal SL, WL and BL voltages, as well as the sizing of the NMOS used for each 2T2R cell.

All simulations made for this thesis are made in a 2-bit 2-word TCAM memory, with a

frequency of 100 [Hz]. The reason for this is to make sure the reading and writing process can be seen clearly in the results. However, in the information presented in [7] it can be seen that higher frequencies can be used for 85 [nm] ReRAM technology (of around 1 [kHz]).

In case of the SL and BL used in the writing operation to make the RESET and SET operations respectively, the voltage used to make sure the HRS and LRS are clear is of 1.2 [V]. Also, the reading voltage for the BL should be limited, as it is possible for HRS memristors to change to LRS if the voltage is high enough. In case this case voltages above 0.4 [V] tend to cause the reading of HRS memristors to cause a SET process. Therefore, the reading voltage of BL was changed to 0.3 [V] to ensure no changes to impedance are made in the reading process. This was simulated with a 1.0 [V] WL reading voltage, which is lower than the usual 1.8 [V] used for 90 [nm] NMOS technology, also to ensure no changes in the memristor state during reading.

For the case of the writing operation for the 2T2R cells, it is necessary to consider the delayed switching in memristors. This can be done by measuring the time it takes for a signal to change the impedance from HRS to LRS and vice- versa [13,14]. Since memristors need to enlarge or shrink its filament through its metal oxide during the SET and RESET process respectively, this takes a set amount of time [4,5,6]. In case of the 85 [nm] model used for this thesis, the RESET process is the one which usually takes a longer time to happen. Therefore, the writing voltages for WL, BL and SL are chosen with this in mind. Also, the width of the NMOS used for each memristor is important, as it will determine the current flowing through the ReRAM. However, the length of the NMOS was kept constant at 0.11 [um], as that is a common length for 90 [nm] CMOS technology.

Therefore, the writing voltage for the WL was kept at 1.8 [V], considering it's the highest voltage the 90 [nm] NMOS model used was capable of using. The width of the NMOS for

the simulations was of 0.41 [um], as it optimizes the delayed switching time for the RESET process as well as improving the ratio of LRS to HRS to 13:1.

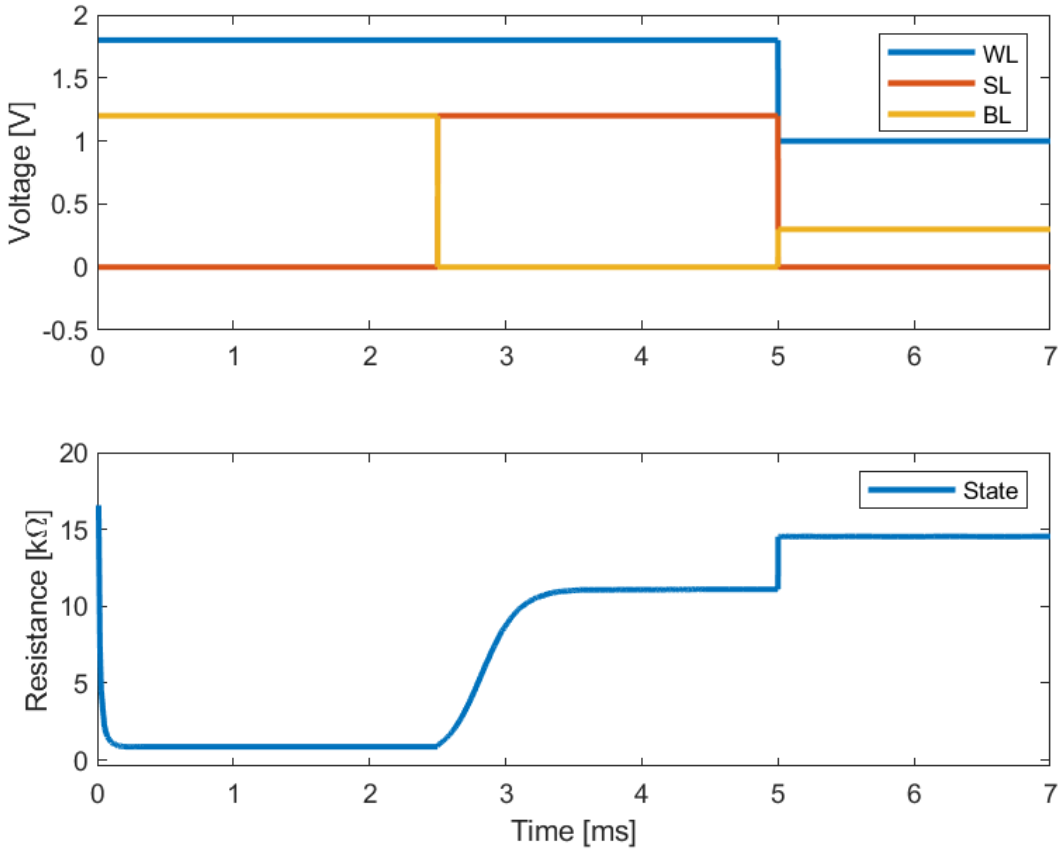


Fig. 8. Simulation results of a 1T1R cell using calibrated Verilog-A ReRAM model, showing the forming, RESET, SET and read operations, with a logical 1 being read

In Figure 8 the results in a 1T1R cell are shown with the previous specifications of the simulation. In this case the figure shows a writing operation starting with a SET, then a RESET and finally a reading operation. In this 1T1R simulation the LRS impedance of the memristor is of 855 [Ω], while its HRS impedance is of 11.1 [kΩ]. At the moment of reading the saved bit when reading an HRS memristor the impedance is of 14.5 [kΩ], while in LRS the memristor only reads 1.17 [kΩ]. These results are the same in 2T2R cells, as the 2T2R cell is simply composed of 1T1R cells.

The delayed switching time for the SET process was of 1.36 [ms], while it was 6.22 [ms] for the RESET process. As mentioned before, the frequency at which it is possible to work with 85 [nm] technology will be determined by this constrain, as any frequency that does not give enough time for the RESET process will have not have reached a HRS properly.

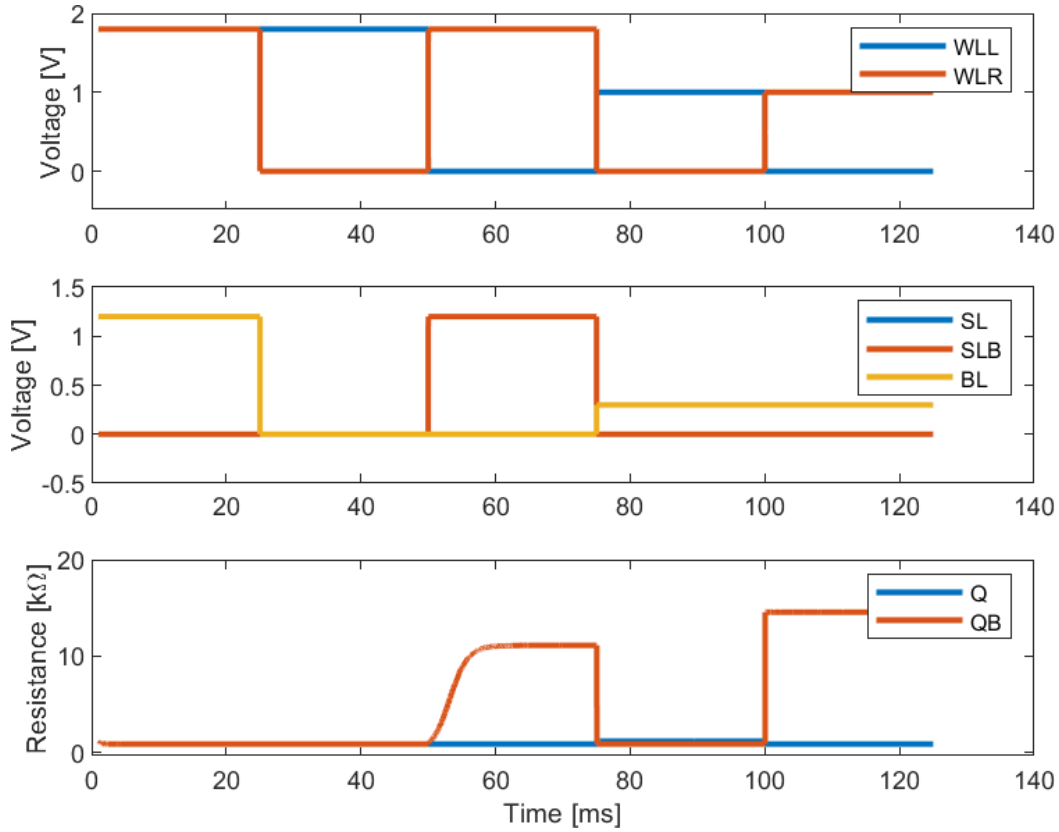


Fig. 9. Simulation results of 2T2R cell with forming operation for both memristors. The TCAM cell is storing a logical 0.

Figure 9 shows the writing and reading process of a 2T2R cell, in which both memristors go first through a SET and then the complementary ReRAM (QB) goes through a RESET. Since the main bit (Q) is in LRS, the stores information in the 2T2R cell of the TCAM is considered a logical zero.

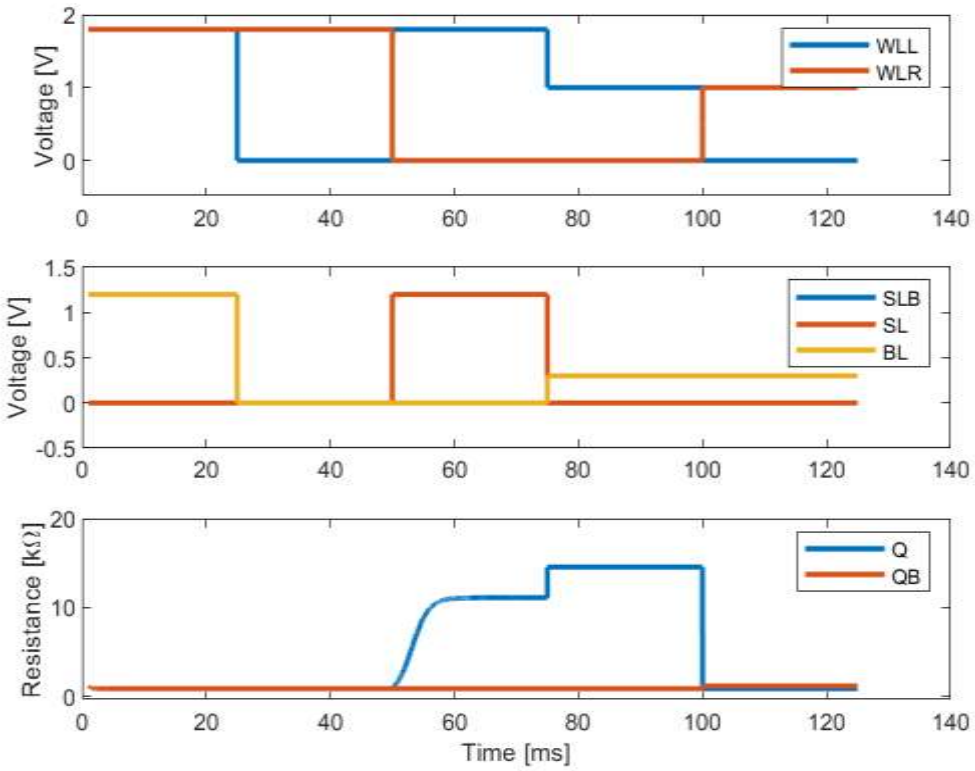


Fig. 10. Simulation results of 2T2R cell with forming operation for both memristors. The TCAM cell is storing a logical 1.

Figure 10 shows a similar process to Figure 9. However, the difference is that the (Q) memristor is the one that goes through the RESET process, which result with it being in a HRS resistive state. Therefore, the stored word in this cell of the TCAM would be of a logical 1.

When reading a TCAM it is possible to either have a match or mismatch. A mismatch is when the read bit of the 2T2R cell is in an LRS resistive state, while a match is when the 2T2R cell is in an HRS resistive state. The reason for this is because it is possible to read either the (Q) or (QB) memristor (see Fig. 6) when searching for information in the TCAM. Therefore, it is important to see the difference between a match and a mismatch. In Figure 11 the matching impedance is of 14.5 [kΩ], while the mismatching one is of 1.17 [kΩ].

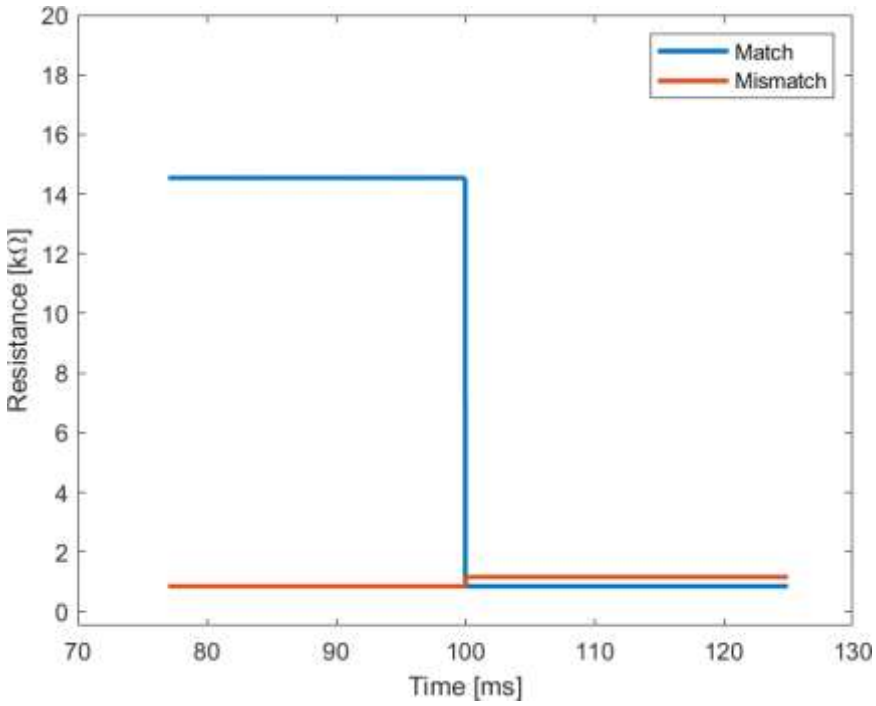


Fig. 11. Simulation result of a memristor reading a match (HRS) and mismatch (LRS)

## CONCLUSIONS

In this thesis the TCAM structure proposed by Yuzong Chen and their team [3,11] was explored with the use of a ReRAM calibrated with experimental data [7]. With the use of a Verilog-A model made for the ReRAM it was possibleto make a simple 1T1R and 2T2R cells of 85 [nm] technology, which are the fundamental cells and one-bit cells for a ReRAM-CMOS combined memory. With the simulations,it was possible to determine the theoretical viability of 85[nm] ReRAM technology in TCAM memories. However, by the delayed switching times have proven that the 85 [nm] memristor is significantly lower than what TCAMs usually need to be. A TCAM needs to be capable of working at frequencies in the scale of the Giga-Hertz [3,11]. However, with the delayed switching of the 85 [nm] ReRAM the possible frequencies in which it can work is only in the Hertz.

However, this does not mean that ReRAM technology isnot capable of being used in TCAM technology. There are already TCAMs in the 65 [nm] and below range, which can be calibrated with the Verilog-A model presented in this thesis. By modeling and testing through simulations smaller ReRAM technologies it is possible to find the optimal size in which ReRAM becomes viable as a component for TCAMs. Furthermore, the results of this thesis lacked variability which was presented in [7]. By improving the Verilog-A model madeit is possible to include variability in future simulations and better represent a real TCAM using memristors. This can be further improved by increasing the number of words and bits in the simulated TCAM, as usually TCAM store much more information than that simulated in this thesis. Therefore, whilethis thesis shows that TCAMs can be made with ReRAM technology alongside CMOS technology, there is still room ofimprovement in the simulation being made with experimental data models of memristors.

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