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Threshold Voltage Instability in SiC and GaN Power Devices

Tesis en torno a una hipótesis o problema de investigación y su constrastación

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Threshold Voltage Instability in SiC and GaN Power Devices

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Dedicatoria

Gracias a mi familia y a las personas que han apoyado.

Abstract

This thesis investigates the properties of power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) based on Silicon Carbide (SiC) and Gallium Nitride (GaN), which are emerging as superior alternatives to traditional silicon-based devices in power electronics. Both SiC and GaN offer significant advantages such as higher breakdown voltages, faster switching speeds, and better thermal performance. This study emphasizes the challenges and improvements in the short-term reliability of these devices under various stress conditions. Indeed, it provides a comparative analysis of SiC- and GaN-based power MOSFETs, focusing on their threshold voltage instability and charge trapping/detrapping phenomena over time by means of hysteresis, positive gate bias stress and zero or negative gate bias recovery measurements. The findings highlight the potential of SiC and GaN materials to enhance the efficiency and reliability of power electronic systems in applications ranging from renewable energy to electric vehicles.

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Chapter 1

Introduction

Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) represent a technology of high relevance in modern electronics and power management systems due to their numerous advantages and wide-ranging applications. They have been advancing with a rich history rooted in the advancements of semiconductor technology. Their development spans several decades and has seen significant evolution since their origin.

This study aims to explore the threshold voltage instability in emerging silicon carbide (SiC) and gallium nitride (GaN) power devices to gain insight into the mechanisms responsible for this phenomenon. These devices are currently of significant interest due to their distinctive bandgap characteristics and threshold voltage behavior for different temperature and stress conditions.

The MOSFET development started in the 1950s with the invention of the MOS (Metal-Oxide-Semiconductor) structure. Engineers like Mohamed Atalla and Dawon Kahng at Bell Labs made pioneering contributions to this technology. In the late 1950s and early 1960s, the MOSFET began to take shape with

significant research and advancements in its fabrication processs and advantages over other technologies. The innovation of the insulated-gate structure (IGFET) contributed as a basis for the practical implementation of MOSFETs addressing certain key challenges and enabling improved performance characteristics such as reducing the gate leakage, improving the threshold voltage control, and enhancing the scaling. Years later, the development of the MOSFET coincided with the "Silicon Revolution". Indeed, the silicon emerged as the preferred semiconductor material due to its abundance, stability, and superior electrical properties. Continuous improvements in semiconductor manufacturing techniques and the development of integrated circuits (ICs) led to the commercialization of MOSFETs. In particular, the integration of multiple transistors, resistors, and capacitors on a single chip marked a significant departure from discrete components, leading to smaller, more efficient, and cost-effective electronic devices from computers to power supplies and beyond [14].

In the last decades, MOSFETs have become an integral part of modern electronics, especially in power electronics due to their high efficiency and switching capabilities. Continuous advancements in semiconductor technology have allowed for the development of smaller and even more efficient MOSFETs. Today, MOSFETs are fundamental components in various applications, including power supplies, motor control, amplifiers, and microprocessors. The constant research and development in semiconductor technology nowadays continues to enhance MOSFETs, making them more efficient, compact, and powerful.

Power MOSFETs technology has reached an advanced state, continually

evolving to meet the demands of various industries that rely on efficient power management and high-performance electronics. The power MOSFETs state of the art can be described in terms of performance improvements in parameters like on-state resistance ($R_{ds(on)}$), switching speed, and efficiency. Advancements in semiconductor materials, device structures, and fabrication techniques contributed to these improvements. In particular, the wide bandgap (WBG) materials such as SiC and GaN have become even more attractive in power electronics. These materials offer superior properties, including higher breakdown voltages, faster switching speeds, and better temperature performance compared to traditional silicon-based MOSFETs.

MOSFETs capable of handling higher voltage and current ratings are being developed, catering to applications in electric vehicles (EVs), renewable energy systems, industrial automation, and high-power electronics. Also, reducing package sizes and advancements in thermal management techniques is aiming to reduce power losses and improve heat dissipation. This allows higher power densities and more compact designs in various applications.

Power MOSFETs are being integrated into intelligent systems with advanced features such as integrated gate drivers, overcurrent protection, and enhanced control circuitry. These innovations aim to optimize system-level efficiency and reliability giving way to emerging technologies like innovative energy systems (solar, wind), data centers, and high-frequency power supplies, thus contributing to the overall efficiency and performance of these systems.

In order to continue developing new devices and technologies, the evolution of the materials also must advance incorporating both traditional and new ma-

terials. The traditional MOSFETs were primarily silicon-based, offering good performance, reliability, and cost-effectiveness along with insulating layers that were commonly silicon dioxide, providing gate insulation. In this regard, new approaches search for combinations of new materials such as Silicon Carbide (SiC) which has emerged as a leading wide bandgap material. This material offers superior characteristics like higher breakdown voltages, and better temperature handling, ideal for high-power and high-frequency applications.

On the other hand, Gallium Nitride (GaN), which this thesis is mostly focused on, is a wide bandgap semiconductor material that has gained significant interest in the electronics industry due to its exceptional properties and potential applications in various fields. Some key aspects of GaN are that it possesses a wider bandgap compared to silicon, enabling it to operate at higher voltages and frequencies while maintaining efficiency, it has a high electron mobility allowing for faster switching speeds and improved performance in high-frequency applications, and it has good thermal conductivity helping in efficient heat dissipation and allowing devices to operate at higher temperatures [12]. While GaN offers superior performance, its manufacturing costs have historically been higher than silicon-based counterparts. Ongoing research focuses on cost reduction and scalability. Further advancements are aimed at improving the reliability and integration of GaN devices into various electronic systems.

The insulating materials beyond silicon dioxide, like high-k dielectrics, are being explored for enhanced gate control and reduced leakage in advanced MOSFETs. Among these materials, we can find Hafnium-based, Zirconium-

based, Aluminium oxide, and rare earth oxides. These materials have gained importance for several reasons such as: allowing thicker gate insulating layers while maintaining effective gate control over the transistor and without compromising performance, facilitating continued miniaturization, lower leakage, their compatibility with advanced materials such as SiC and GaN.

Hybrid composites represent another approach to solve the challenges concerning old technologies and materials. Combinations of materials like SiC with silicon or other materials are often used in device designs to exploit the advantages of different materials for the customization of specific characteristics, like power handling capabilities, breakdown voltages, or reliability, by strategically integrating different materials.

Power MOSFETs find applications in a wide range of industries and electronic systems due to their ability to efficiently manage and control electrical power. They play a critical role in modern electronics and power systems, enabling efficient power management, precise control, and reliable operation across a broad spectrum of applications that people use day by day. Some of their general applications are power conversion and switching power supplies used in AC-DC and DC-DC converters for efficient voltage regulation and power distribution in various electronic devices. They are also used in motor control employed in motor drives for precise control of speed and torque in industrial automation, appliances, robotics, and automotive systems.

As electric vehicles and hybrid electric vehicles are gaining popularity, power MOSFETs play a vital role in EV/HEV powertrains, battery management systems, and charging units, contributing to improved efficiency and performance.

Likewise, the renewal energy systems depend completely on this kind of transistors such as the solar inverters, used in photovoltaic systems, which exploit these MOSFETs to convert DC power generated by solar panels into AC power for the grid. The wind power converters use wind turbine systems for converting variable wind-generated power into usable electricity also through power MOSFETs.

They are also widely used in high-voltage power transmission and distribution systems for grid control and management and industrial automation which is applied in various industrial equipment and machinery for control and automation processes that need a great quantity of power and cannot be managed with conventional MOSFET transistors.

The special characteristics of power MOSFETs are efficiency because they have low on-state resistance (Rds(on)), thus leading to minimal power losses and ensuring high system efficiency. The fast-switching capability also facilitates a rapid control of electrical power for various purposes. In addition, the compactness allows for compact and lightweight designs due to their high-power density and small form factor.

This thesis is focused on the study of Silicon Carbide (SiC) and especially Gallium Nitride (GaN) power MOSFETs since these topologies have shown a lot of improved characteristics like a better response over a prolonged time stress voltage, regarding the trapping and detrapping phenomena. All these characteristics directly affect the circuit performance since the current flow in the drain channel depends on them.

Chapter 2

SiC and GaN

2.1 Silicon Carbide

Silicon carbide holds significance as a crucial non-oxide ceramic with a wide range of industrial uses. It is seldom found in nature, and its synthesis as a compound material comprising silicon and carbon was initially accomplished by Berzelius in 1824. This exotic material has gained much importance in the last decades due to their unique properties whose rivaled with the silicon material that is present in most of the electronic devices. Nevertheless, its production and treatment has been improved because it brings many advantages for the electronics industry such as the ones that was mentioned before.

Nowadays, silicon carbide is encountering similar challenges to those faced by silicon in the 1950s and 1960s, when it was considered a substitute for germanium by physicists and engineers. Despite being relatively recent and more costly compared to silicon, SiC has already proven to offer distinct advantages over alternative materials. As an increasing number of these devices enter the market and their capabilities grow, they have the potential to initiate their

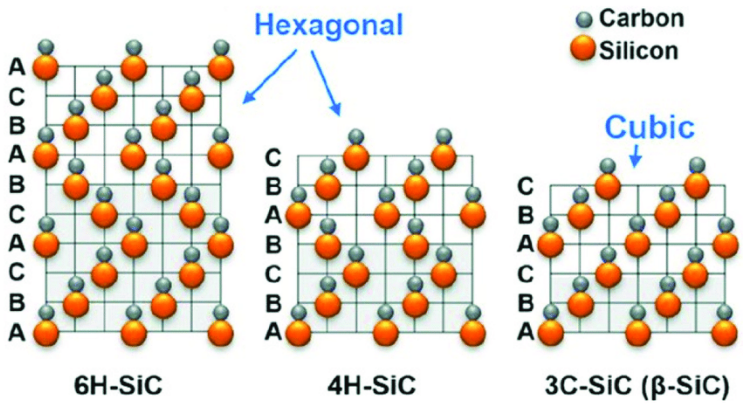

Figure 2.1: The staking sequences of SiC polytypes: 4H-SiC, 6H-SiC, and 3C-SiC [10]

own revolution.

Silicon carbide stands out as a crucial non-oxide ceramic due to its distinctive properties, including exceptional hardness, strength, chemical and thermal stability, elevated melting point, resistance to oxidation and erosion, position it ideally for applications requiring high power and temperature electronic devices, as well as tasks involving abrasion and cutting.

These characteristics are contingent upon the polytype, or different structural configurations of silicon carbide employed (Fig. 2.1). Silicon carbide distinguishes itself in this aspect, as over 250 polymorphs of SiC have been identified, some of which exhibit lattice constants as long as 301.5 nm, approximately one thousand times the usual SiC lattice spacings. A catalog of the most prevalent polytypes includes 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H, 15R, 19R, 2OH, 21H, and 24R, where (C), (H), and (R) represent the three fundamental cubic, hexagonal, and rhombohedral crystallographic categories, respectively [9].

Among these, there are two hexagonal structures (4H-SiC and 6H-SiC) cur-

rently dominating the electronic market, while other new emerging technologies are based on the cubic form 3C-SiC. The material properties, such as high breakdown field ranging from 2 [MV/cm] to 4 [MV/cm] and a high band gap between 2.3 [eV] to 3.2 [eV], remain superior compared to silicon.

Table 2.1: Different properties of the 3 most important SiC polytypes for electronics [5]

Table 1 Select physical properties of the 3C, 4H and 6H polytypes of SiC at room temperature

Properties/polytype	*3C-SiC*	*4H-SiC*	*6H-SiC*
Lattice parameters (Å)	a=4.3596	a=3.0798 c=10.0820	a=3.0805 c=15.1151
Density (g cm^{-3})	3.21	3.21	3.21
Young's Modulus (GPa)	350–650	350–650	350–650
Poisson's ratio	0.21	0.21	0.21
Specific heat capacity (J g^{-1} K^{-1})	0.69	0.69	0.69
Thermal Conductivity (W cm^{-1} K^{-1})	3.3–4.9	3.3–4.9	3.3–4.9
Bandgap (eV)	2.36	3.26	3.02
Electron mobility (undoped) (cm^2 V^{-1} s^{-1})			
⊥ c-axis	1000	1020	450
∥ c-axis	1000	1200	100
Hole mobility (undoped) (cm^2 V^{-1} s^{-1})	100	120	100
Electron saturated drift velocity (undoped) (cm s^{-1})	$\sim 2 \times 10^7$	2.2×10^7	1.9×10^7
Hole saturated drift velocity (undoped) (cm s^{-1})	$\sim 1.3 \times 10^7$	$\sim 1.3 \times 10^7$	$\sim 1.3 \times 10^7$
Critical (breakdown) electric field strength ($\sim 10^{15}$ electrons cm^{-3}) (MV cm^{-1})			
⊥ c-axis	1.4	2.2	1.7
∥ c-axis	1.4	2.8	3.0
Relative dielectric constant (100 kHz–1 MHz)			
⊥ c-axis	9.72	9.76	9.66
∥ c-axis	9.72	10.32	10.03

From Table (2.1), we can see other important properties for the 3 different polytypes described before. The table there also reports other characteristics to understand better the behaviour of this material when it is used as a semiconductor.

Considering all these properties, semiconductor devices based on wide-bandgap materials like silicon carbide offer numerous advantages for power electronic designers.

These materials exhibit superior physical properties compared to silicon, including lower intrinsic carrier concentration (by 10^{-35} orders of magnitude),

higher electric breakdown field (4–20 times), greater thermal conductivity (3–13 times), and larger saturated electron drift velocity (2–2.5 times) (refer to Table (2.2)). Over the past 15 years, silicon carbide has garnered significant attention from research groups and companies. Its wide bandgap energy, ranging from 2.2 to 3.3 eV, surpasses silicon's 1.1 eV bandgap. Furthermore, silicon carbide boasts a higher electric breakdown field of 3 x 10^6 V/cm, i.e., an order of magnitude greater than that of silicon. This higher breakdown field permits a tenfold reduction in drift layer thickness, thereby reducing minority carrier charge storage and significantly enhancing the switching frequency of bipolar devices.

Additionally, silicon carbide's high carrier saturation velocity of 2 x 10^7 cm/s is an order of magnitude greater than that of silicon. Its notable thermal conductivity of 4.9 $\frac{W}{cmK}$ facilitates efficient heat dissipation, coupled with the wide bandgap energy, enabling power-efficient high-temperature operation up to 350 °C [7].

Among other advantages, for a 5000-V power device, the required drift layer thickness is significantly reduced to only 40–50 μm, compared to nearly 500 μm for silicon. This smaller drift layer results in lower drift resistance, leading to reduced forward voltage drop and conduction losses. With a thermal conductivity of around 5 $\frac{W}{cmK}$, silicon carbide enables high-temperature operation of junctions and effective thermal management. Another crucial factor is the carrier lifetime. While silicon carbide, like silicon, is an indirect bandgap semiconductor, gallium nitride (GaN), like gallium arsenide (GaAs), is a direct bandgap semiconductor. Consequently, silicon carbide exhibits much longer

minority carrier lifetimes compared to GaN. Experimental studies have shown recombination lifetimes up to 1 second in 4H–SiC. [7]

Table 2.2: Main properties comparison between different materials [7]

Material	E_g (eV)	n_i (cm^{-3})	ε_r	μ_n ($cm^2/V \cdot s$)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ ($W/cm \cdot K$)	*Direct/ Indirect*
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim 10^{3}$	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	**2.2**	**6.9**	**9.6**	**900**	**1.2**	**2.0**	**4.5**	**I**
4H-SiC	**3.26**	**8.2×10^{-9}**	**10**	**720^a 650^c**	**2.0**	**2.0**	**4.5**	**I**
6H-SiC	**3.0**	**2.3×10^{-6}**	**9.7**	**370^a 50^c**	**2.4**	**2.0**	**4.5**	**I**
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0*	13	I
AlN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: *a* — mobility along a-axis, *c* — mobility along c axis, *— estimate.

Despite these numerous advantages, challenges related to material processing, the existence of crystal defects like micropipes and dislocations, costs related to its extraction and fabrication, and limited availability of wafer suppliers have hindered rapid advancements in commercializing SiC power devices and their widespread adoption within the power electronics community.

SiC devices also present some challenges for high voltage applications due to their significantly higher electric fields in the junction termination area, which has much smaller dimensions in terms of both width and depth compared to traditional junction terminations. Despite the associated higher costs, SiC manufacturers can leverage the WBG properties to reduce the size of the junction termination area, thereby maximizing the usable active area.

While SiC can achieve high blocking capabilities with such designs, the

impact of the elevated fields outside the semiconductor bulk (such as in passivation layers and package filling materials) will be more pronounced than in silicon. Additionally, the absence of dopant diffusion in SiC means that the high electric fields are positioned very close to the surface. However, the higher doping levels in SiC compared to silicon in the termination region offer reduced sensitivity to surface charge variations, which could otherwise alter the electric field locally and lead to device failure [16].

This material is widely recognized for its multitude of advantages across various fields, including biomedicine. However, the full potential of this material remains untapped across a broad spectrum, largely due to the prevalence of a high degree of defects. Despite possessing a wide bandgap, high thermal conductivity, and high breakdown electric field, SiC performance in conventional power device applications falls short of desired standards at elevated temperatures due to these defects. Among the most common defects, there are screw dislocations with various Burgers vectors, stacking faults, low angle grain boundaries, basal plane dislocations, threading edge dislocations, and the interaction of these defects often leads to the formation of additional device-detrimental defects, further compromising device performance [21].

The SiC material applications have a wide spectrum due to their better properties and advantages compared with the traditional Si devices. Thanks to innovative characteristics, new technologies can be developed and improved over the time. The following segment examines recent and noteworthy advancements in SiC device technology within key and emerging industrial sectors, including solar energy, uninterruptible power supplies (UPS), traction

systems, electric vehicles (EVs), and induction heating (IH) [18]:

- SiC Solar Inverter: Recent advancements in SiC solar inverters have focused on improving efficiency, density, and cost-effectiveness. Studies have investigated SiC Schottky diode-based solar microinverters, resulting in reduced reverse recovery losses and enhanced efficiency. Addressing the need for high weight density in rooftop applications, SiC MOSFET-based photovoltaic string inverters have been developed.

- Uninterrupted Power Supply: Innovation in UPS systems is primarily driven by the need for high efficiency, power quality, and power density, particularly in online double-conversion UPS setups. These systems benefit significantly from efficient SiC converters due to the higher cost of electrical losses at the user end compared to the generation end. SiC converters offer increased efficiency, resulting in reduced electricity usage and cooling requirements, thus lowering the total cost of ownership. UPS installations are often in environments where space is limited, such as office buildings, factories, or data centers, making compact, high-power-density solutions highly desirable.

- Railway Traction Inverter: Railway traction applications prioritize characteristics such as low power loss, light weight, high voltage rating, and high temperature resistance to enhance efficiency and performance. The reduction in weight and size of traction systems not only improves overall system efficiency but also maximizes space utilization within railway vehicles for passengers. Traditionally, three-level traction inverters were preferred due to limitations in the switching frequency capability of Si

IGBTs. However, recent advancements have led to the development of two-level traction drive systems that incorporate Si IGBTs and SiC JBS diodes. These advancements have resulted in significant reductions in total losses, system weight, and volume.

- Electric Vehicles: SiC devices play a crucial role in achieving high power density, i.e., a key requirement for power electronics circuits in electric vehicles (EVs). The importance of power density is almost on par with cost considerations. Initiatives like the EV Everywhere Challenge, introduced in 2013, call for significant reductions in size, weight, and losses in EV components, goals that can be met through the adoption of SiC power devices. As the cost of SiC devices decreases, more EV manufacturers are expected to integrate them into their vehicles.

2.2 Gallium Nitride

Gallium nitride (GaN) has garnered significant attention in the power industry due to its impressive performance and size benefits compared to silicon. As a compound of gallium and nitrogen, GaN is characterized by its hardness, thermal robustness, chemical stability, and high-temperature resilience. With a wider energy gap of 3.4 electron volts, GaN surpasses silicon's 1.1 eV, a critical factor determining semiconductor electrical conductivity. Moreover, GaN can be produced at a lower cost than conventional semiconductors. The utilization of semiconductors with wide band gaps like GaN in power electronic devices offers numerous advantages, including faster switching, high-conduction capabilities, low resistance, and reduced capacitance, ultimately leading to lower

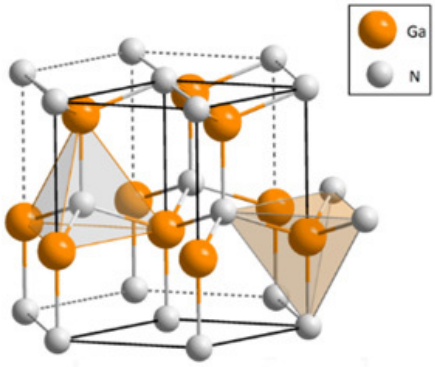

Figure 2.2: The atomic structure of GaN wurtzite crystal

power losses and energy consumption [1].

Gallium nitride features gallium with atomic number 31, belonging to group 13, and nitrogen with atomic number 7, belonging to group 15. In its natural state, GaN occurs in two different structural forms: wurtzite and zinc blende EPC (Fig. 2.2). In both structures, each gallium atom, classified as a group III element, forms bonds with four nitrogen atoms. The structure's pattern is hexagonal. Both structural variations of GaN exhibit notable chemical stability, thereby augmenting GaN piezoelectric characteristics. Typically, GaN is doped to achieve either n-type or p-type conductivity, employing silicon or magnesium dopants, respectively. GaN structural attributes contribute to its high conductivity levels.

Among the properties of GaN (Table 2.3), it possesses a significantly higher band gap energy of 3.39 eV, a little bit higher than the SiC material, and much higher compared to silicon, rendering it well-suited for high-temperature

applications. Due to GaN's elevated wide band gap energy, a higher breakdown voltage (V_{BD}) can be attained. This is because the breakdown voltage of semiconductors is directly linked to the breakdown electric field (E_{BD}) which, at room temperature, is $35*10^5$ V/cm. GaN-based devices are therefore well-suited for high-voltage applications and serve as efficient replacements for less efficient silicon transistors. Additionally, higher breakdown voltages contribute to the reduction in transistor size, leading to smaller resistance for current flow. Consequently, GaN transistors exhibit lower on-state resistance compared to their silicon-based counterparts.

Table 2.3: Properties comparison between GaN, SiC and Si [17]

Property	Symbol	Unit	Value
Silicon band gap energy	$E_{G(Si)}$	eV	1.12
Silicon band gap energy	$E_{G(Si)}$	J	1.793×10^{-19}
Silicon-carbide band gap energy	$E_{G(SiC)}$	eV	3.26
Silicon-carbide band gap energy	$E_{G(SiC)}$	J	5.216×10^{-19}
Gallium-nitride band gap energy	$E_{G(GaN)}$	eV	3.39
Gallium-nitride band gap energy	$E_{G(GaN)}$	J	5.430×10^{-19}
Silicon breakdown electric field	$E_{BD(Si)}$	V/cm	2×10^5
Silicon-carbide breakdown electric field	$E_{BD(SiC)}$	V/cm	22×10^5
Gallium-nitride breakdown electric field	$E_{BD(GaN)}$	V/cm	35×10^5
Silicon relative permittivity	$\epsilon_{r(Si)}$	–	11.7
Silicon-carbide relative permittivity	$\epsilon_{r(SiC)}$	–	9.7
Gallium-nitride relative permittivity	$\epsilon_{r(GaN)}$	–	8.9
Silicon electron mobility at $T = 300$ K	$\mu_{n(Si)}$	$cm^2/V{\cdot}s$	1360
Silicon-carbide electron mobility at $T = 300$ K	$\mu_{n(SiC)}$	$cm^2/V{\cdot}s$	900
Gallium-nitride electron mobility at $T = 300$ K	$\mu_{n(GaN)}$	$cm^2/V{\cdot}s$	2000
Silicon hole mobility at $T = 300$ K	$\mu_{p(Si)}$	$cm^2/V{\cdot}s$	480
Silicon-carbide hole mobility at $T = 300$ K	$\mu_{p(SiC)}$	$cm^2/V{\cdot}s$	120
Gallium-nitride hole mobility at $T = 300$ K	$\mu_{p(GaN)}$	$cm^2/V{\cdot}s$	30
Silicon effective electron mass coefficient	$k_{e(Si)}$	–	0.26
Silicon effective hole mass coefficient	$k_{h(Si)}$	–	0.39
Silicon-carbide effective electron mass coefficient	$k_{e(SiC)}$	–	0.36
Silicon effective hole mass coefficient	$k_{h(SiC)}$	–	1
Gallium-nitride effective electron mass coefficient	$k_{e(GaN)}$	–	0.23
Gallium-nitride effective hole mass coefficient	$k_{h(GaN)}$	–	0.24

Talking about the on-resistance ($R_{DS(on)}$) of the power device, it decreases as the cube of the electrical breakdown and electron mobility, resulting in reduced conduction resistance. Essentially, GaN devices theoretically possess

an on-resistance approximately three times lower than that of Si devices. Due to its properties, there is an increase in on-resistance for different devices with varying breakdown voltages. For silicon transistors, higher breakdown voltages lead to higher on-resistance, reaching a few $k\Omega$ for devices with $V_{BD} \geq 10$ kV. Conversely, SiC and GaN transistors exhibit very low on-resistance at these voltages. Specifically, SiC transistors show an on-resistance of approximately 20 Ω at $V_{BD} = 10$ kV, while GaN devices demonstrate an on-resistance of approximately 0.5 Ω at the same breakdown voltage [17].

Decreasing the on-state resistance while maintaining a fixed breakdown voltage results in a decrease in the overall device size, consequently leading to reduced capacitances. This, in turn, lowers the associated switching losses and allows for higher operation frequencies for switching.

After discussing the main properties of GaN, the advantages of this material can be exposed. A common and commercial GaN FET can endure a maximum voltage stress of 60 V and a maximum current stress of 40 A. It is capable of functioning at frequencies as high as 15 MHz. Its on-state resistance, parasitic capacitance, and turn-off times are minimal, making it an ideal choice for high-voltage, high-frequency power electronic applications.

Incorporating GaN devices into a power converter leads to many significant benefits at the system level, such as: increased operational frequency, lower energy consumption leading to higher efficiency, enhanced power density resulting in a smaller volume. GaN-based devices enable higher switching frequencies, which facilitate a reduction in the size of passive components. This leads to a substantial decrease in weight and volume, thereby lowering the

overall cost of the power system. Depending on the application, GaN devices can improve system efficiency by 3 to 10% [15].

By substituting silicon with GaN, the following improvements can be achieved:

- the efficiency of DC-to-DC conversion can rise from 85% to 95%;
- the efficiency of AC-to-DC conversion can increase from 85% to 90%;
- the efficiency of DC-to-AC conversion can improve from 96% to 99%.

Additionally, the higher efficiency of GaN devices results in less energy being dissipated as heat, leading to reduced cooling needs, smaller heat sinks, and consequently smaller system sizes and lower material costs.

Additionally, GaN has the potential to be much more affordable than SiC because it can be grown on a silicon substrate, enabling its processing to be compatible with standard CMOS fabs. EPC (Efficient Power Conversion) manufactures its devices using silicon wafers with a layer of gallium nitride grown on top. While these wafers are more expensive than plain silicon wafers, gallium nitride devices can be miniaturized due to the higher electric field strength required to break down a gallium nitride crystal compared to silicon. In theory, this allows for more devices to be produced from the same wafer, ultimately reducing costs. However, the actual cost reduction depends on factors such as yield (the number of functional devices produced per wafer) and economies of scale [4].

While GaN-based technologies have shown clear advantages in power electronics applications, their widespread adoption in the market hinges on addressing several challenges that can impact their overall performance and potentially limit the benefits outlined in earlier paragraphs. These challenges

include [15]:

- In depletion-mode operation, also known as normally-on operation, current flows even when there is no bias applied to the gate terminal. This is considered undesirable because it is preferable for zero current to flow in the power system when no voltage is applied to it.

- A low threshold voltage is considered undesirable, as an optimal threshold voltage value to mitigate noise-induced voltage fluctuations and prevent parasitic turn-on of the device at elevated temperatures is above 2 V. However, many GaN technologies currently proposed exhibit a threshold voltage below 2 V, typically ranging from 1.2 to 1.8 V. Despite various efforts to raise the threshold voltage, no technology currently available on the market achieves a threshold voltage much greater than 1.5 V.

- Reliability issues, also referred to as current collapse or dynamic on-resistance, are common concerns in GaN devices. Current collapse refers to a reliability issue observed in GaN devices, where there is a decrease in the output current after subjecting the device to high-voltage stress. This reliability issue has been demonstrated to be both time and voltage-dependent. This thesis is centered on explain and compare this phenomenon between the SiC and GaN technologies. It is generally acknowledged that if the current decreases by 10-15% after repeated high-voltage stress, the device is considered to pass reliability standards.

- Switching oscillations, which occur at high frequencies, can induce oscillations in systems employing GaN devices as power switches. These oscillations, characterized by spikes in currents and voltages, have the po-

tential to cause premature device failure or unintended activation. They can occur during both turn-on and turn-off phases and are not easily regulated solely by the gate drive. However, controlling these oscillations through careful design or selecting an appropriate gate drive is essential.

GaN-based materials and hetero structures find utility across various domains, including optoelectronics, power electronics, and high-frequency devices. The subsequent subsection will provide a brief overview of the primary applications of nitride devices [2]:

1. GaN holds potential for various applications, including large television screens or smaller full-color panels in transportation vehicles like trains or buses. Previously, full-color displays faced limitations due to the insufficient brightness of blue and green LEDs. However, GaN-based LEDs offer significantly improved efficiency, thereby presenting a viable solution for blue and green LEDs in such displays.

2. LEDs consume less energy and have longer lifespans, thus contributing to energy and cost savings. Nitride-based semiconductors, which emit in the ultraviolet (UV) spectrum, can be integrated with phosphor converters to produce white light. However, this capability is currently hindered by the high manufacturing costs of LEDs. Managing the heat generated by LEDs poses significant challenges, particularly with higher power output, despite their increased efficiency, as excessive heat can quickly degrade LED lifespan.

3. Room temperature lasers based on gallium nitride with impressive lifespans have been successfully developed and demonstrated. There exists a

substantial market demand for optical data reading and writing in CD, DVD, and opto-magnetic memory applications.

4. Microwave amplifiers used in wireless communication systems result in improved reception on mobile phones and fewer low-earth satellites and transmitting stations in the environment. The enhanced transmitting power and increased efficiencies offered by GaN materials mean that fewer geostationary satellites can perform the same function as many more low-earth satellites.

5. Aerospace components capable of functioning across a broad temperature spectrum and resilient to radiation. GaN's chemical composition suggests it will likely demonstrate increased resistance to radiation, making it highly anticipated for such applications.

Although GaN holds promise for various technological applications, there are still some fundamental material properties of group III nitride materials that remain incompletely understood. While advancements in growth and fabrication methods can enhance extrinsic effects mentioned earlier, controlling basic properties remains challenging. Thus, further research is necessary to comprehend their role in device operations. While transport measurements and optical characterization have provided some insights, there are still areas requiring further investigation.

2.3 SiC vs GaN

Gallium nitride and silicon carbide FETs are facilitating increased levels of power density and efficiency in contrast to conventional silicon MOSFETS as it has been mentioned before. Despite both being wide bandgap technologies, there are inherent distinctions between GaN and SiC, leading to one being more suitable than the other in specific topologies and applications. This section aims to compare the strengths and weakness of each technology to conclude which one is generally better.

The use of wide-bandgap devices like GaN and SiC has brought about significant changes in the power industry. These devices offer notable advantages over both silicon MOSFETs and IGBTs, characterized by lower gate capacitance that facilitates faster turn-on and turn-off, thereby reducing gate drive losses. For example, GaN boasts a gate charge of less than 1 nC-Ω, compared to silicon's 4 nC-Ω. Additionally, these devices feature markedly lower output capacitance, allowing designers to achieve higher switching frequencies without a corresponding increase in switching losses and enabling the reduction in size and weight of magnetics in the system. A typical GaN device exhibits an output charge of 5 nC-Ω, as opposed to comparable silicon devices at 25 nC-Ω [3].

GaN and SiC cater to distinct power requirements in the market. SiC devices provide voltage levels reaching up to 1,200 V along with robust current-carrying capacities, rendering them suitable for various applications such as automotive and locomotive traction inverters, high-power solar farms, and large three-phase grid converters. In contrast, GaN FETs are commonly 600-V de-

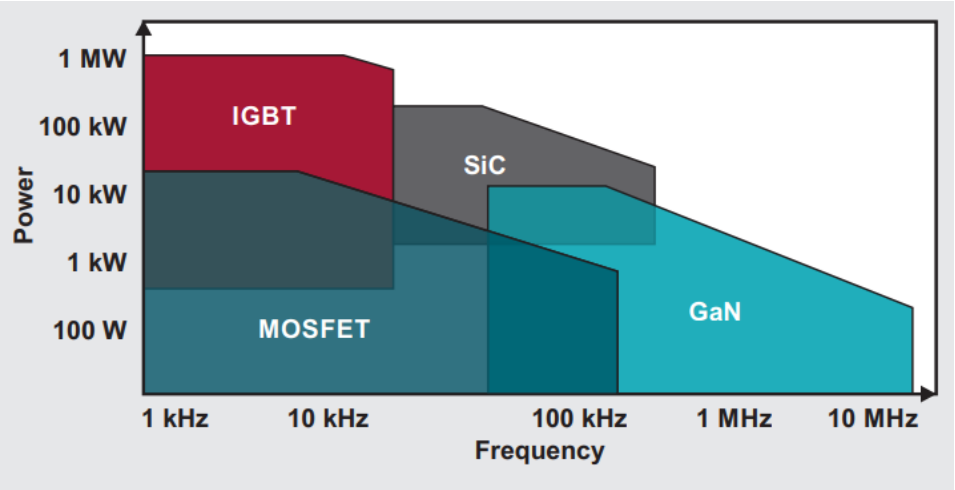

Figure 2.3: High-voltage power device mapping, different technologies capabilities [3]

vices and can facilitate the development of high-density converters spanning 10 kW and beyond. GaN finds applications across various sectors including consumer electronics, server systems, telecommunications, industrial power supplies, servo drives, grid converters, electric vehicle onboard chargers, and DC/DC converters.

Despite these differences, these two technologies do overlap in some applications below 10 kW as can be seen in the Fig. 2.3. In the following, we make a comparison between SiC and GaN technologies considering two specific examples.

Single-phase PFC

Every electrical appliance that draws more than 75 W from the power grid must incorporate power factor correction (PFC). PFC serves as the initial step in converting power from the grid to the system, carrying the entire load regardless of operating conditions. As a result, its efficiency and power density

have a direct impact on the overall size of the system. In applications connected to a single-phase grid, PFC stages are typically engineered to accommodate a universal AC input range (85 VAC to 264 VAC) and can generate output voltages of up to 400 VDC. Designers have employed various topologies with the aim of minimizing size while adhering to industry efficiency standards.

The totem-pole configuration offers a cost-efficient option compared to dual-boost PFC setups by halving the number of power devices and inductors required, as opposed to the dual boost topology commonly used in high-power systems exceeding 1 kW. Additionally, it notably enhances both density and efficiency. Solutions employing either SiC or GaN devices in the totem-pole configuration are readily accessible.

GaN presents several advantages over SiC in this configuration, notably:

- GaN FETs offer zero reverse recovery, as they lack the P-channel N-channel junction found in MOSFETs. Consequently, GaN FETs do not incur reverse-recovery losses associated with body diodes. In contrast, SiC FETs are susceptible to reverse-recovery losses due to the presence of body diodes in their structure.

- GaN demonstrates lower switching energy compared to SiC, with GaN's switching energy being over 50% lower than that of SiC. This reduction directly leads to decreased losses in the PFC stage. Moreover, in certain pivotal totem-pole applications, achieving switching frequencies exceeding 1 MHz is feasible.

- GaN devices offer faster switching speeds, with newer generations featuring integrated gate drivers capable of switching at speeds of up to

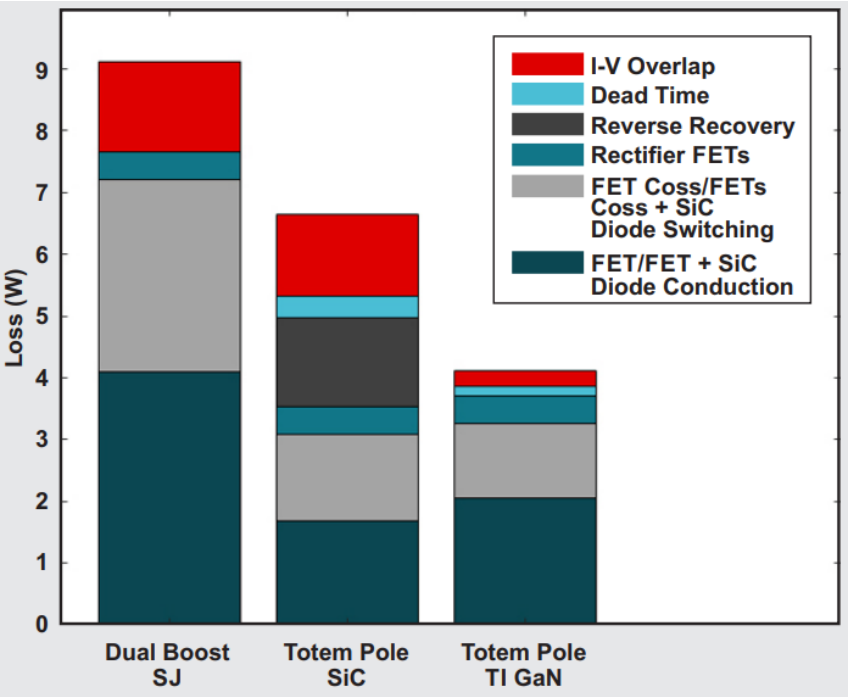

Figure 2.4: Comparison of loss breakdown in a 1-kW PFC between superjunction (SJ), SiC, and GaN [3]

150 V/ns. This results in a significant reduction in losses—up to 82% compared to SiC and 63% compared to discrete GaN FETs.

Fig. 2.4 illustrates a comprehensive breakdown of losses in a dual-boost PFC, a totem pole employing SiC, and a totem pole utilizing GaN. GaN demonstrates the lowest losses and highest efficiency in this scenario. These benefits empower designers to achieve high power density and substantially decrease the cost and size of cooling components like heat sinks and fans.

Three-phase grid converters

In three-phase grid-tied power supply applications, higher AC and DC bus voltage levels are typical, often reaching 480 V line-to-line for AC inputs and potentially exceeding 900 V for DC bus voltage, depending on the specific application. While a two-level converter with 600-V GaN FETs is not feasible,

multilevel topologies employing GaN provide a viable alternative. Multilevel circuits utilize different configurations of stacked lower-voltage devices and control mechanisms to accommodate higher-voltage three-phase grid applications. In comparison to a two-level converter utilizing 1,200-V SiC or IGBT, GaN offers several advantages in multilevel converter setups, such as:

- GaN demonstrates superior switching figures of merit (FOMs) compared to SiC, particularly in reverse recovery, switching energy, speed, and dead-time losses. These advantages become more pronounced when comparing a 600-V GaN FET to a 1,200-V SiC or IGBT.

- Reducing overall expenses, which covers making things cheaper by using surface-mount devices, cutting down on electromagnetic interference stuff, shrinking magnetic filter sizes, and cooling requirements.

- Improved thermal distribution is particularly crucial in applications employing convection cooling, allowing designers to evenly distribute thermal energy across a larger array of power devices.

- Increased system compactness. With the converters operating at higher frequencies, there are considerable reductions in the size of passive components and heat sinks across the system.

The Table 2.4 summarizes in a simple way the most important operation conditions between 3 different technologies, i.e., IGBT, SiC and GaN. From this table, we can see that the GaN topology exhibit better results in terms of general performance.

Table 2.4: Comparing IGBT, SiC and TI GaN devices for multilevel converters [3]

Typical Operating Conditions	IGBT	SiC	TI GaN
Frequency (kHz)	20	100	140
Open-frame power density (W/in^3)	73	170	211
Efficiency (%)	98.3	98.9	99.2

GaN and SiC cost comparison

As previously stated, GaN technology allows for substantial cost reductions at the system level by reducing the need for both active and passive components, enabling the use of smaller and lighter magnetic components, and decreasing cooling requirements. However, the cost savings extend beyond these factors. GaN is moving towards offering the lowest device cost overall. The cost of any semiconductor integrated circuit or field-effect transistor (FET) is determined by various factors, these factors include: substrate cost, chips per wafer and wafer fabrication. To make a comparison, these three variables can be expressed in a simple equation:

$$\text{Device cost} = \frac{\text{substrate cost} + \text{wafer fabrication}}{\text{chips per wafer}} \tag{2.1}$$

The quantity of chips per wafer depends on factors such as the wafer's size, the device's on-resistance, and the thermal resistivity of the technology involved. SiC generally exhibits superior thermal resistivity compared to both GaN and silicon, resulting in a larger number of chips per wafer. Nonetheless, this is just one aspect of the overall cost assessment [3].

The cost of the substrate stands out as a significant distinction between GaN

and SiC. GaN devices are cultivated on common and easily accessible silicon substrates, much like the process used for producing billions of semiconductor integrated circuits annually. Additionally, by utilizing silicon substrates, manufacturers can make use of existing fabrication techniques and equipment, including the transition to 300-mm wafers.

SiC not only has a much higher cost for raw materials, but it also demands specialized manufacturing procedures. A crucial element of the SiC production process involves maintaining temperatures exceeding 2,500°C, leading to considerable energy expenses for manufacturers.

The Table 2.5 shows a normalized comparison between the cost of the 3 technologies, where we can observe that GaN has just a little increase compared to the traditional technologies and is cheaper than the SiC technology.

Table 2.5: Normalized future device costs of power devices [3]

Technology	Normalized Substrate and Fabrication	Normalized Chips per Wafer	Normalized Device Cost
Superjunction (SJ) MOSFET	1.0	1.0	1.0
GaN	3.0	2.4	1.3
SiC	10.3	4.3	2.4

SiC and GaN cater to distinct voltage, power, and application requirements, yet they also intersect in certain end-use scenarios. SiC devices are capable of handling voltage levels up to 1,200 V with robust current capacities, making them suitable for automotive and locomotive traction inverters, high-capacity solar installations, and large-scale three-phase grid converters. Con-

versely, GaN, renowned for its superior switching figures of merit (FOMs), cost-effectiveness in manufacturing, and capability to operate at higher frequencies, has emerged as the preferred option for designers working on applications below 10 kW. Whether it is a USB Type-C adapter, a multi-kilowatt telecom rectifier, an integrated motor drive for robotics, or an electric vehicle onboard charger, designers now possess the tools to select the most suitable technology for creating environmentally friendly, lighter, and economically efficient products.

Chapter 3

Power MOSFETs based on SiC and GaN

3.1 General description of Power MOSFETs

Power MOSFETs find primary application in power switching circuits such as DC/DC or AC/DC converters. By utilizing wide bandgap components, higher transistor switching frequencies become feasible, leading to reduced values of inductive elements and enhanced energy efficiency of power electronic devices. In these applications, where minimizing switch-on resistance (R_{on}) is crucial, the transistor functions as a controlled switch. Additionally, there exists a category of power electronic devices where MOSFETs are employed as controlled resistors, including power amplifiers, electronic current sources, or active electronic loads.

Related to the main topic of this thesis, the dielectric (oxide) of a power MOSFET primarily associates to the properties of the insulating layer, known as the gate oxide, which separates the gate electrode from the semiconductor

channel. This dielectric layer serves as a capacitor, allowing the MOSFET to control the flow of current between the source and drain terminals by modulating the voltage applied to the gate. The dielectric function involves several key aspects: dielectric constant breakdown Voltage (V_{BD}), gate oxide thickness (t_{ox}) and frequency response.

The gate oxide material used in Si, GaN, and SiC MOSFETs is primarily silicon dioxide (SiO_2), although alternatives like AlGaN, MgO and Ga_2O_3 are also employed. However, the degradation of these gate oxide materials are more pronounced in SiC and GaN MOSFETs compared to Si MOSFETs. This difference arises because the electric field experienced by the SiO_2 in SiC material is nearly 2.5 times the breakdown strength of SiC, which is approximately ten times higher than that experienced by the SiO_2 in Si material. Additionally, the gate oxide thickness tends to be smaller in SiC and GaN MOSFETs. Consequently, the gate oxide in SiC MOSFETs may approach its reliability limits more rapidly. Hence, it is crucial to closely monitor the effects of gate oxide degradation in SiC and GaN MOSFETs [6].

The mechanism of gate oxide degradation differs between Si and SiC/GaN MOSFETs structures. In Si MOSFETs, degradation leads to the formation of positive oxide-trapped charges within the gate oxide, resulting in a decrease in precursor magnitude, and negative interface trapped charges at the oxide-silicon interface, leading to an increase in precursor magnitude. These precursors exhibit a simultaneous dip-and-rebound variation pattern over time. In contrast, in SiC/GaN MOSFETs, gate oxide degradation occurs due to the direct tunneling of electrons into preexisting oxygen vacancy defects near the

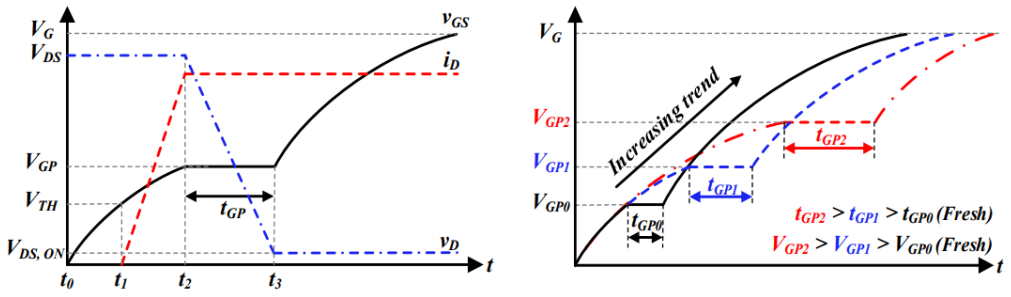

Figure 3.1: Parameters variation due to the trap effects [11]

channel-oxide interface, also known as near-interface oxide traps.

The tunneling of electrons into these traps depends on the bias-stress magnitude and time. Longer bias-stress times or higher magnitudes allow electrons to tunnel deeper into the oxide. Consequently, under positive gate bias stress, the threshold voltage in SiC MOSFETs increases over time. Both the voltage gate plateau (V_{GP}) and the time duration of programming (t_{GP}) have a strong analytical relationship with the near-interface oxide traps through the threshold voltage. Therefore, V_{GP} and t_{GP} are expected to show a simultaneous increasing trend similar to the threshold voltage during the stress time. In consequence, the drain current (I_D) will be reduced due to the effects of the traps generated and the increase of the V_{TH} [11]. The studied effects can be appreciated in Fig. 3.1.

Talking about the channel, its width in a power MOSFET determines the amount of current that the MOSFET can carry when it is turned on. A wider channel width allows more current to flow through the MOSFET, increasing its conductivity and reducing its on-state resistance. This is important for power MOSFETs used in high-current applications, such as power amplifiers or motor control circuits, where low on-state resistance and high current-carrying

capability are essential for efficient operation. Increasing the channel width can improve the performance and efficiency of the power MOSFET in such applications. As can be seen in the equation 3.1, with a wider channel width the $R_{DS_{on}}$ can be improved reducing it.

$$R_{DS_{on}} = \frac{R_{DS}}{W} \tag{3.1}$$

The common channel width sizes for power MOSFETs can vary depending on the specific application requirements and the manufacturing process used. However, typical channel width sizes for power MOSFETs can range from a few micrometers (μm) to several hundred micrometers. In high-power applications, channel widths are often larger to accommodate higher current-carrying capacities and reduce on-state resistance. Conversely, in lower-power applications or integrated circuits, smaller channel widths may be sufficient to meet the performance requirements while conserving space and reducing cost. Ultimately, the choice of channel width depends on factors such as desired current handling capabilities, on-state resistance, and overall system design considerations [8].

The channel length in a power MOSFET determines the distance between the source and drain terminals along the semiconductor material's surface when a voltage is applied to the gate terminal. It plays a crucial role in controlling the MOSFET's on-state resistance $R_{DS_{on}}$ and its ability to conduct current. Specifically, the channel length affects the size of the conductive channel formed between the source and drain terminals. A shorter channel length allows for a shorter and more direct path for current flow, reducing the resistance

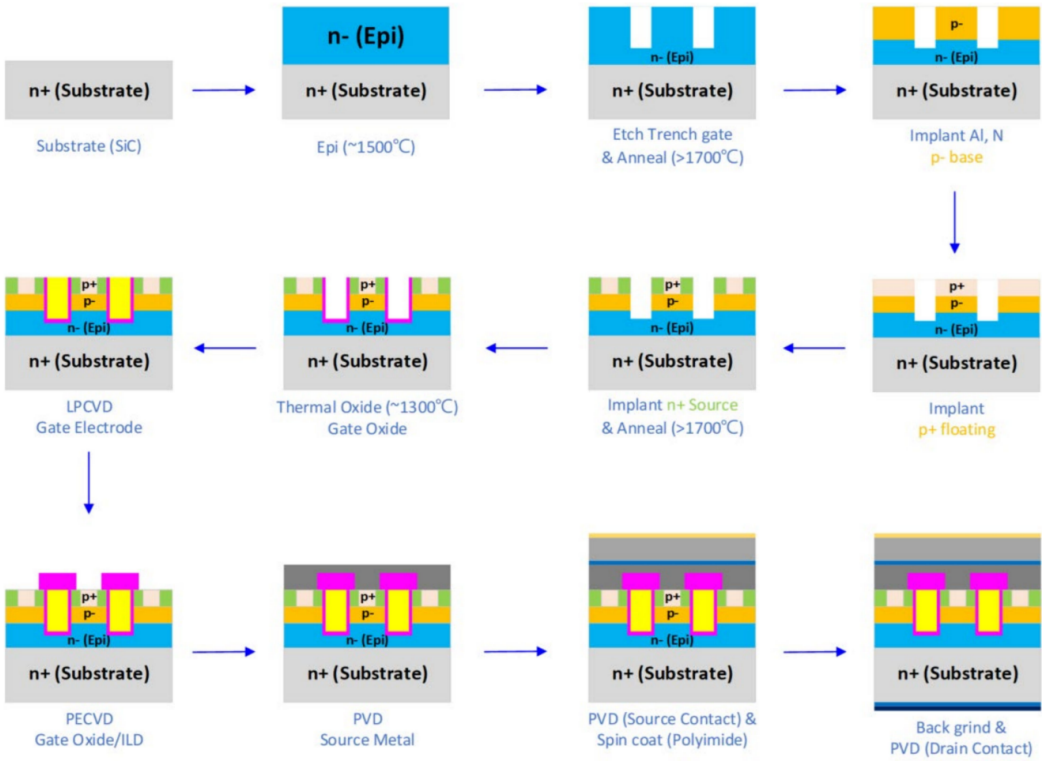

Figure 3.2: General Power MOSFET fabrication process flow [13]

and enabling higher current-carrying capability. Conversely, a longer channel length increases the resistance and decreases the current-carrying capacity of the MOSFET. In power MOSFETs, shorter channel lengths are generally preferred to minimize on-state resistance and improve overall performance, especially in high-power and high-frequency applications where low resistance and efficient power handling are essential. However, the choice of channel length must also consider factors such as breakdown voltage, gate control, and manufacturing constraints.

The fabrication process for power MOSFETs can vary depending on the topologies and materials used but in general it can be generalized as follows (Fig. 3.2): initially, the n-drift region is grown epitaxially on the n^+ substrate. Next, the trenched gate region is formed by trenching the structure using implantation with Al or N to create the p-base region. Following this,

p^+ implantation is conducted to establish the shielding region, succeeded by n^+ implantation to delineate the source and drain regions. Subsequent to the implantation steps, the resulting structure undergoes high-temperature exposure for thermal oxidation to generate gate oxide after annealing. Then, the gate electrode, source metal, and drain metal are deposited. Ultimately, a polyimide layer is applied as a protective passivation coating. Various methods of ion implantation and thermal oxidation processes are employed to enhance device performance by minimizing the number of defects in the SiC substrate and epitaxial layer [13].

3.1.1 SiC-based MOSFETs under test

Part of this thesis was addressed to evaluate n-channel SiC-based power MOSFETs provided by STMicroelectronics. More specifically, automotive-grade SCTH40N120G2V7AG commercial devices (H^2PAK-7 package), whose main electrical characteristics are reported in Fig. 3.3, were investigated. This SiC power MOSFET device is the result of STMicroelectronics advanced and innovative 2nd generation SiC MOSFET technology. It boasts remarkably low on-resistance per unit area and exhibits excellent switching performance. Moreover, the variation of switching loss remains nearly unaffected by changes in junction temperature.

From Fig. 3.3., the SCTH40N120G2V7AG power MOSFET can handle a maximum V_{DS} of 1200 V, a V_{GS} with operational values from -5 V up to 18 V and endure a 33 A I_D at room temperature. This MOSFET can work at temperatures of -55 up to 175 ^{o}C and exhibit a $R_{DS_{on}}$ which can vary from 75

to 105 $m\Omega$ at room temperature and 167 $m\Omega$ at maximum temperature. Also, its V_{TH} can vary from 1.9 V up to 5 V with a typical value of 3.2 V. In Fig. 3.4 we can see its typical output characteristics at T = 25^{o}C.

This chip shows key features such as: minimal switching losses, low power losses even at elevated temperatures, extended operating temperature range, body diode with negligible recovery losses, simple to drive. Also, it has the benefits of a smaller physical footprint and increased power density, a decreased size and cost of passive elements, enhanced overall system efficiency, diminished need for cooling and smaller heat sink dimensions. It can be used in traction inverters, electric vehicle charging stations, solar power systems, industrial automation, electric motor controllers, power supplies for data centers, on-board chargers and DC/DC converters [19].

3.1.2 GaN-based MOSFETs under test

The thesis activity was also addressed to test n-channel GaN-based power MOSFETs provided by STMicroelectronics. More specifically, two different types of commercial devices were investigated, i.e., SGT120R65AL and SGT65R65AL devices (both with PowerFLAT 5x6 HV packag), whose main electrical characteristics are respectively reported in Fig. 3.5 and 3.6.

This chips integrates a 650 V, 15 A and 25 A enhancement-mode (e-mode) PowerGaN transistor with a proven packaging technology. The resulting G-HEMT (Gallium Nitride High Electron Mobility Transistor) device has exceptionally low conduction losses, high current capacity, and extremely fast switching capabilities. These features enable the device to achieve high power

density and unmatched efficiency performance as expected from a GaN device.

From Fig. 3.5, the SGT120R65AL power MOSFET can handle a maximum V_{DS} of 650 V, a V_{GS} with operational values from -10 V up to 6 V and endure a 15 A I_D at room temperature. This MOSFET can work at temperatures of -55 up to 150 ^{o}C and has a $R_{DS_{on}}$ which can vary from 75 to 120 $m\Omega$. Also, its V_{TH} can vary form 1.2 V to 2.6 V with a typical value of 1.8 V. In Fig. 3.7 we can see its typical output characteristics at T = 25 ^{o}C.

From Fig. 3.6, the SGT65R65AL power MOSFET can handle a maximum V_{DS} of 650 V, a V_{GS} with operational values from -10 V up to 7 V and endure a 25 A I_D at room temperature. This MOSFET can work at temperatures of -55 up to 150 ^{o}C and has a $R_{DS_{on}}$ which can vary from 49 to 65 $m\Omega$. Also, its V_{TH} has a typical value of 1.8 V.

These chips have key features such as: enhancement mode normally off transistor, exceptionally high switching speeds, robust power management capabilities, extremely low capacitances, incorporated Kelvin source pad for optimal gate driving, and zero reverse recovery charge, which makes them ideal in applications like adapters for tablets, notebook and AIO, USB type-C PD adapters and quick chargers, and finally wireless chargers [20].

3.2 Short-term reliability testing

The activity carried out within this thesis was addressed to short-term reliability testing of Sic- and GaN-based power transistor. To this aim, hysteresis, positive gate bias stress and zero or negative gate bias recovery measurements

in DC conditions at room temperature were performed on devices under test described in the previous sections.

The electrical characterization of commercial packaged devices was done by using a measurement set-up including the Keithley 4200 Semiconductor Characterization System (4200-SCS) equipped with source-measure-units (SMUs), as shown in Fig. 3.8 and 3.9. In particular, three SMUs were used according to the following scheme: the MOSFET drain terminal was connected to the SMU1, the MOSFET gate terminal was connected to the SMU4, and the MOSFET source terminal was connected to the SMU2.

Referring to the performed measurements, the threshold voltage (V_{TH}) and the maximum transconductance ($g_{m,max}$) of devices under test were initially extracted from the linear region of the measured I_D-V_{GS} characteristics at V_{DS} = 50 mV, as shown in Fig. 3.10.

Then, the following procedure was considered for hysteresis tests:

- An initial stabilization phase was carried out by applying a negative gate-source voltage (i.e., V_{GS} = -5 V for SiC-based devices and V_{GS} = -10 V for GaN-based devices) for 60 s to reset the device characteristics, i.e., to release the trapped charge at the channel/oxide interface or in the bulk oxide.

- I_D-V_{GS} characteristics were measured at V_{DS} = 50 mV by sweeping the V_{GS} from a minimum negative voltage ($V_{GS,min}$) up to a maximum positive voltage ($V_{GS,max}$) and vice versa to evaluate the maximum hysteresis-induced V_{GS} shift ($\Delta V_{GS,hyst}$) by comparing the forward and backward

curves at the current corresponding to $V_{GS} = V_{TH}$ in the forward curve, as shown in Fig. 3.11.

More specifically, the hysteresis in SiC-based devices under test was evaluated by considering in the V_{GS} sweeping a $V_{GS,min}$ = -5 V and different $V_{GS,max}$ values equal to 6 V, 10 V, 14 V, and 18 V, whereas for GaN-based devices a $V_{GS,min}$ = -5 V and $V_{GS,max}$ values equal to 3 V, 4 V, and 5 V were used.

Instead, the following procedure was considered for stress/recovery measurements:

- An initial stabilization phase of 60 s (i.e., V_{GS} = -5 V for SiC-based devices and V_{GS} = -10 V for GaN-based devices) was initially carried out. Such stabilization phase ensures that the device reaches a consistent reference state for subsequent experiments, allowing for fair comparisons among different stress conditions.

- A reference I_D-V_{GS} curve was measured by sweeping the V_{GS} from - 5 V up to 6 V for SiC-based devices and up to 3 V for GaN-based devices at V_{DS} = 50 mV.

- The positive gate bias stress phase was done by applying a positive bias voltage $V_{GS,stress}$ for a stress time t_{stress} = 100 s. To monitor the time evolution of the stress-induced degradation, the stress phase was interrupted at fixed time intervals and the I_D at V_{DS} = 50 mV and $V_{GS,meas}$ equal to 5 V for SiC-based devices and 2 V for GaN-based devices was measured. Such I_D values were used to extrapolate the corresponding stress-induced V_{GS} shift ($\Delta V_{GS,stress}$) from the previously measured reference I_D-V_{GS} curve, as shown in Fig. 3.12.

- After the stress, the recovery phase was performed by applying a zero or negative recovery voltage $V_{GS,recov}$ for a recovery time t_{recov} = 100 s. As in the stress phase, in order to monitor the time evolution of the recovery-induced relaxation, the recovery phase was interrupted at fixed time intervals and the I_D at V_{DS} = 50 mV and $V_{GS,meas}$ equal to 5 V for SiC-based devices and 2 V for GaN-based devices was measured. Such I_D values were again used to extrapolate the corresponding recovery-induced V_{GS} shift ($\Delta V_{GS,recov}$) from the reference I_D-V_{GS} curve measured before the stress.

More specifically, the stress was evaluated by considering different $V_{GS,stress}$ values, i.e., 10 V, 14 V, and 18 V for SiC-based devices, while 2 V, 2.5 V, and 3 V for GaN-based devices. Similarly, the recovery was evaluated by using different $V_{GS,recov}$ values, i.e., 0 V, -2.5 V, and -5 V for both SiC- and GaN-based devices.

Symbol	Parameter [Unit]	Value
$V_{(BR)DSS}$	Drain-source breakdown voltage [V]	1200
V_{GS}	Gate-source voltage [V]	-5 to 18
I_D	Drain current (DC) @25°C [A]	33
$V_{GS(th)}$	Gate threshold voltage @V_{GS} = V_{DS}, I_D = 1 mA [V]	1.9 (min.), 3.2 (typ.), 5 (max.)
$R_{DS(on)}$	Static drain-source on-resistance @V_{GS} = 18 V, I_D = 20 A [mΩ]	75 (typ.), 105 (max.)
C_{iss}	Input capacitance @V_{DS} = 800 V, f = 1 MHz, V_{GS} = 0 V [pF]	1230
T_J	Operating junction temperature range [°C]	-55 to 175

Figure 3.3: Main electrical characteristics of SCTH40N120G2V7AG devices [19]

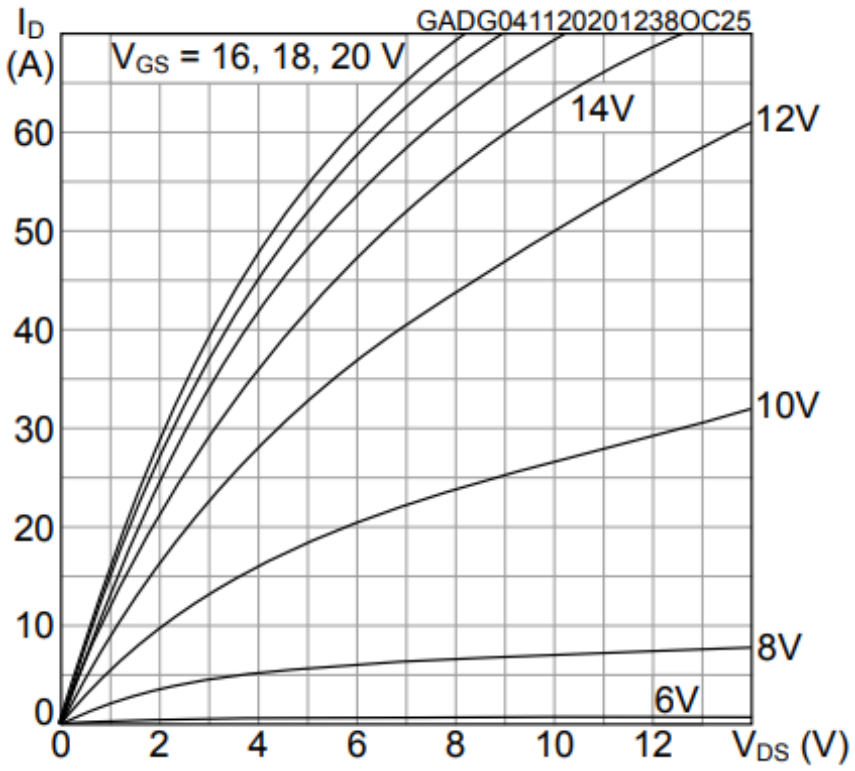

Figure 3.4: SiC Power MOSFET (SCTH40N120G2V7AG) output characteristics at room temperature [19]

Symbol	Parameter [Unit]	Value
$V_{(BR)DSS}$	Drain-source breakdown voltage [V]	650
V_{GS}	Gate-source voltage [V]	-10 to 6
I_D	Drain current (DC) @25°C [A]	15
$V_{GS(th)}$	Gate threshold voltage @V_{DS} = 0.1 V, I_D = 12 mA [V]	1.2 (min.), 1.8 (typ.), 2.6 (max.)
$R_{DS(on)}$	Static drain-source on-resistance @V_{GS} = 6 V, I_D = 5 A [mΩ]	75 (typ.), 120 (max.)
T_J	Operating junction temperature range [°C]	-55 to 150

Figure 3.5: Main electrical characteristics of SGT120R65AL devices [20]

Symbol	Parameter [Unit]	Value
$V_{(BR)DSS}$	Drain-source breakdown voltage [V]	650
V_{GS}	Gate-source voltage [V]	-10 to 7
I_D	Drain current (DC) @25°C [A]	25
$V_{GS(th)}$	Gate threshold voltage @V_{DS} = 0.01 V, I_D = 2.3 mA [V]	1.8 (typ.)
$R_{DS(on)}$	Static drain-source on-resistance @V_{GS} = 6 V, I_D = 15 A [mΩ]	49 (typ.), 65 (max.)
T_J	Operating junction temperature range [°C]	-55 to 150

Figure 3.6: Main electrical characteristics of SGT65R65AL devices

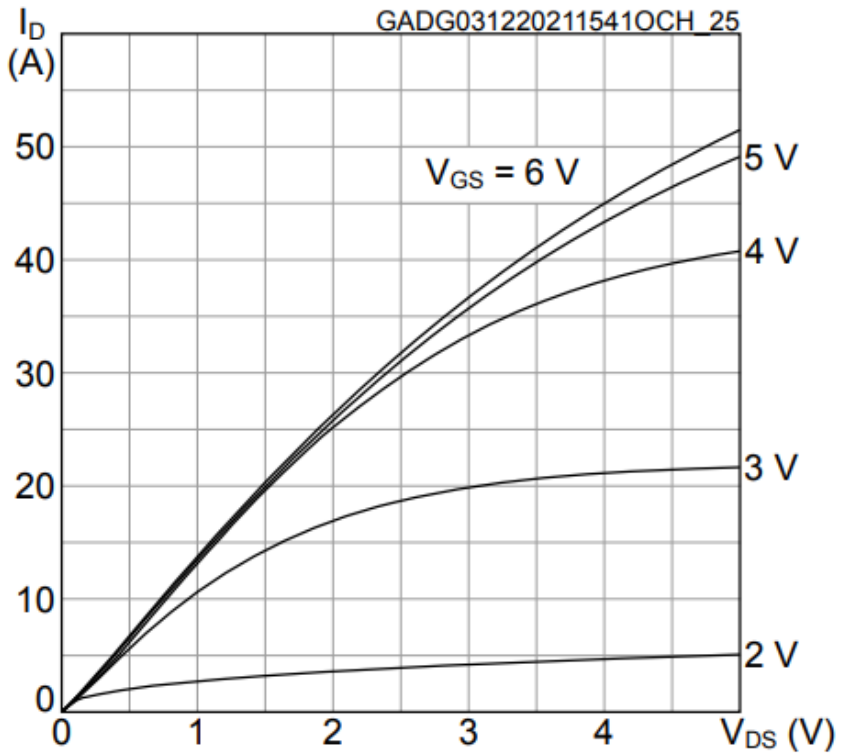

Figure 3.7: GaN Power MOSFET (SGT120R65AL) output characteristics at room temperature [20]

Figure 3.8: 4200-SCS Semiconductor Characterization System

Figure 3.9: 4200-SCS Semiconductor Characterization System' SMUs

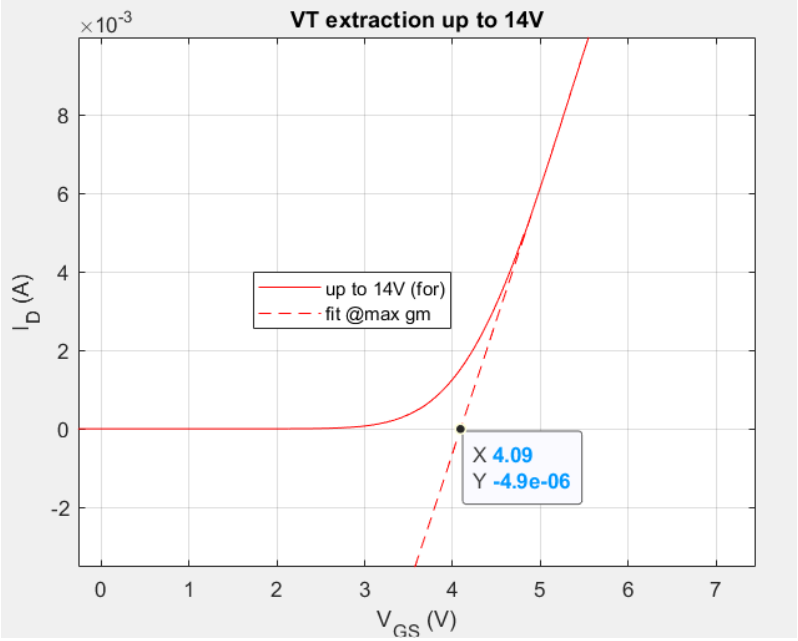

Figure 3.10: Example of V_{TH} extraction in a typical SiC device

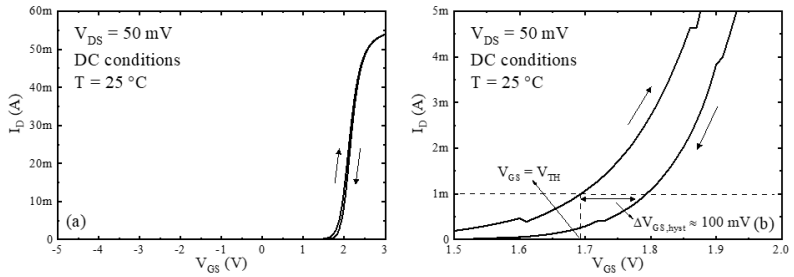

Figure 3.11: Hysteresis measurements for a typical GaN-based device: (a) I_D-V_{GS} characteristics (V_{GS} from -5 V up to 3 V and vice versa) at V_{DS} = 50 mV and room temperature, (b) evaluation of the hysteresis-induced shift ($\Delta V_{GS,hyst}$).

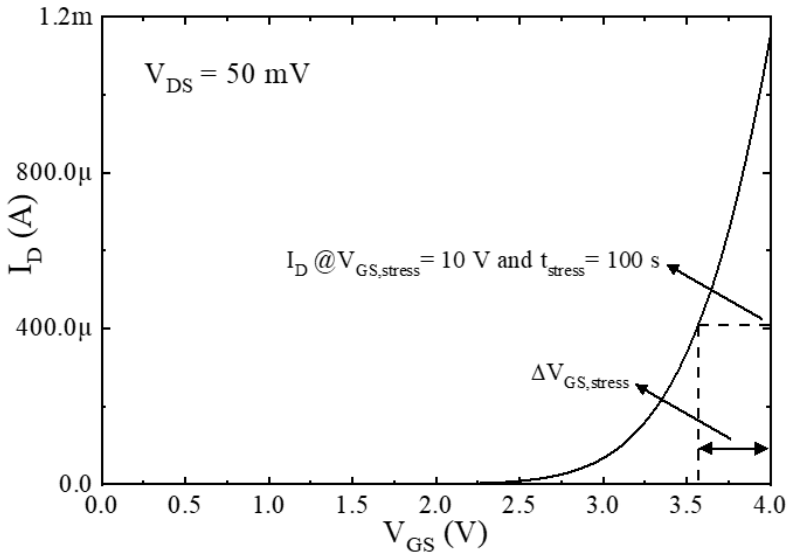

Figure 3.12: Example of reference I_D-V_{GS} characteristics measured at V_{DS} = 50 mV and room temperature for a representative SiC-based device and extrapolation of the stress-induced $\Delta V_{GS,stress}$ shift at $V_{GS,stress}$ = 10 V and t_{stress} = 100 s.

Chapter 4

Measurement results and discussion

4.1 Threshold voltage and maximum transconductance

This section reports and discusses the measured data in terms of V_{TH} and $g_{m,max}$ for all tested devices.

SiC-based SCTH40N120G2V7AG devices

Five samples of the SiC-based SCTH40N120G2V7AG device were evaluated in this thesis. Fig. 4.1 shows the related measurement histograms. From this figure, the measured V_{TH} shows a mean value of 4.09 V and a quite low sample-to-sample variability equal to $\sigma/\mu = 5.5\%$, whereas the $g_{m,max}$ shows a more pronounced $\sigma/\mu = 20.9\%$.

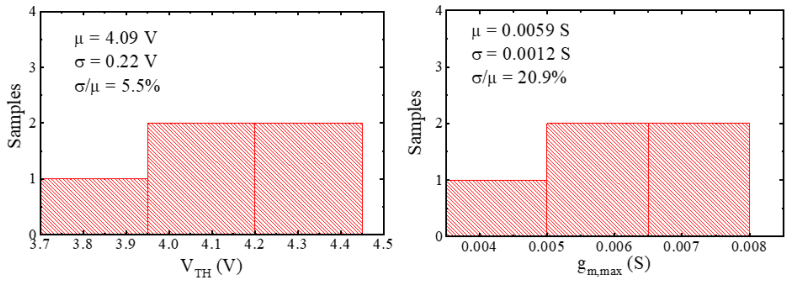

Figure 4.1: Measurement histograms of the V_{TH} and $g_{m,max}$ across five samples of SiC-based SCTH40N120G2V7AG device.

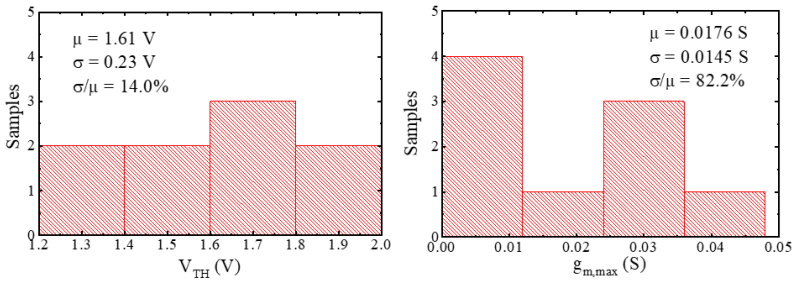

Figure 4.2: Measurement histograms of the V_{TH} and $g_{m,max}$ across nine samples of GaN-based SGT120R65AL device.

GaN-based SGT120R65AL devices

Nine samples of the GaN-based SGT120R65AL device were evaluated, whose statistical results in terms of V_{TH} and $g_{m,max}$ are reported in Fig. 4.2. From this figure, the measured V_{TH} shows a mean value of 1.61 V and a sample-to-sample variability equal to $\sigma/\mu = 14.0\%$, whereas the $g_{m,max}$ shows a very high $\sigma/\mu = 82.2\%$.

GaN-based SGT65R65AL devices

Eight samples of the GaN-based SGT65R65AL device were evaluated, whose V_{TH} and $g_{m,max}$ statistical data are shown in Fig. 4.3. From this figure, the measured V_{TH} shows a mean value of 1.45 V (again lower than the SiC-based

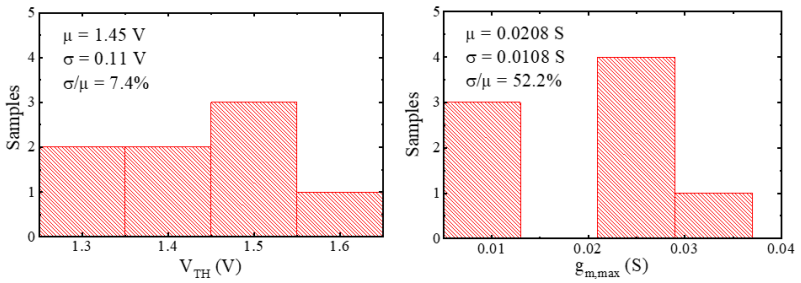

Figure 4.3: Measurement histograms of the V_{TH} and $g_{m,max}$ across eight samples of GaN-based SGT65R65AL device.

devices) and a sample-to-sample variability equal to $\sigma/\mu = 7.4\%$, whereas the $g_{m,max}$ shows a quite high $\sigma/\mu = 52.2\%$.

4.2 Hysteresis

This section reports and discusses the measured hysteresis data in terms of the $\Delta V_{GS,hyst}$ shift for both SiC- and GaN-based tested devices.

SiC-based SCTH40N120G2V7AG devices

Fig. 4.4 shows the $\Delta V_{GS,hyst}$ as a function of the $V_{GS,max}$ for the tested SiC-based devices. From this figure, we can observe a quite significant $\Delta V_{GS,hyst}$ values in the order of hundreds millivolts. This is ascribed to the decrease of the current and hence a corresponding decrease of the threshold voltage in the backward curve due to trapped negative charges (i.e., electrons) as given by the applied positive gate voltage. Consistently across all tested devices, we can also appreciate an increasing trend of the $\Delta V_{GS,hyst}$ shift with increasing $V_{GS,max}$, which translates into filling the traps at higher energy levels. Furthermore, the measured hysteresis exhibits a quite low sample-to-sample variability (i.e.,

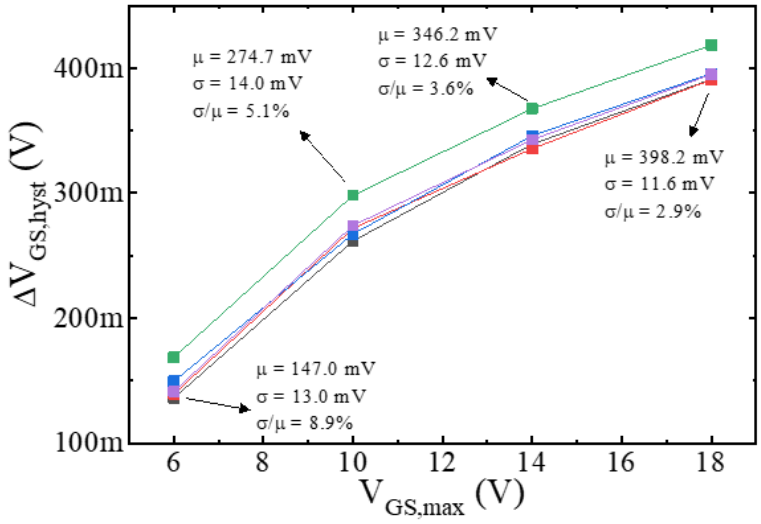

Figure 4.4: $\Delta V_{GS,hyst}$ versus $V_{GS,max}$ across five samples of SiC-based SCTH40N120G2V7AG device.

σ/μ below 10%, coherently with the low variability observed for the V_{TH}), along with a decreasing trend for higher $V_{GS,max}$.

Fig. 4.5 shows the scatter plot of the $\Delta V_{GS,hyst}$ versus the V_{TH}. From this plot, we can observe a clear and strong correlation between the hysteresis-induced shift and the threshold voltage of the device, i.e., the lower V_{TH}, the higher the $\Delta V_{GS,hyst}$. This could be ascribed to the fact that a lower V_{TH} could be associated with more available traps and hence a higher hysteresis-induced shift due to a more significant trapping phenomena.

GaN-based SGT120R65AL devices

Fig. 4.6 shows the $\Delta V_{GS,hyst}$ as a function of the $V_{GS,max}$ for the tested GaN-based SGT120R65AL devices. From this figure, we can observe a mean $\Delta V_{GS,hyst}$ of about 130-140 mV with values ranging from 40 mV up to 200 mV. In all devices, we can note a slight increasing trend of the $\Delta V_{GS,hyst}$ shift when

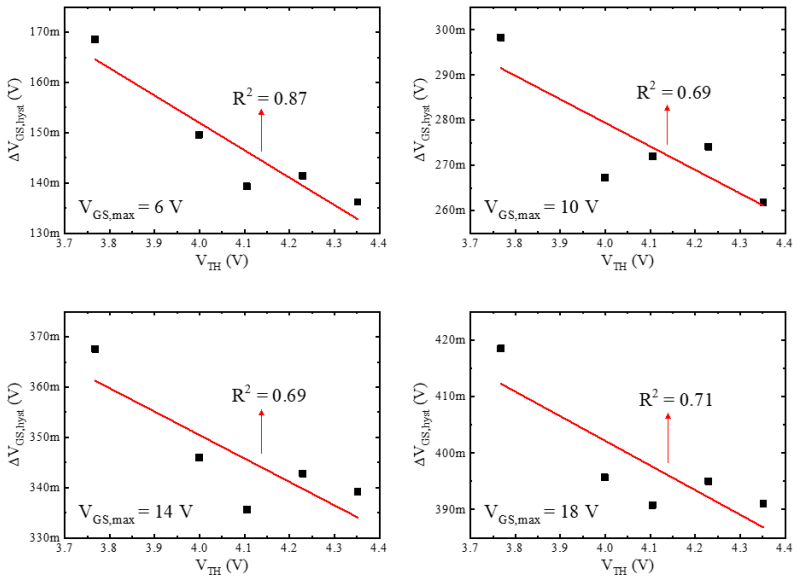

Figure 4.5: $\Delta V_{GS,hyst}$ versus V_{TH} across five samples of SiC-based SCTH40N120G2V7AG device.

passing from $V_{GS,max} = 3$ V to $V_{GS,max} = 4$ V, whereas an anomalous behavior is observed at $V_{GS,max} = 5$ V where the $\Delta V_{GS,hyst}$ shows a decrease. Furthermore, the measured hysteresis exhibits a relevant sample-to-sample variability in the order of 40%.

Fig. 4.7 shows the scatter plot of the $\Delta V_{GS,hyst}$ versus the V_{TH}. From this plot, as in SiC-based devices, we can note a strong correlation with a significant increase of the $\Delta V_{GS,hyst}$ for lower V_{TH}.

GaN-based SGT65R65AL devices

Fig. 4.8 shows the $\Delta V_{GS,hyst}$ as a function of the $V_{GS,max}$ for the tested GaN-based SGT65R65AL devices. From this figure, we can observe a mean $\Delta V_{GS,hyst}$ of about 110-120 mV with values ranging from about 80 mV up to about 160 mV. As in SGT120R65AL devices, we can again observe an anomalous behavior with increasing $V_{GS,max}$. In addition, the tested samples show

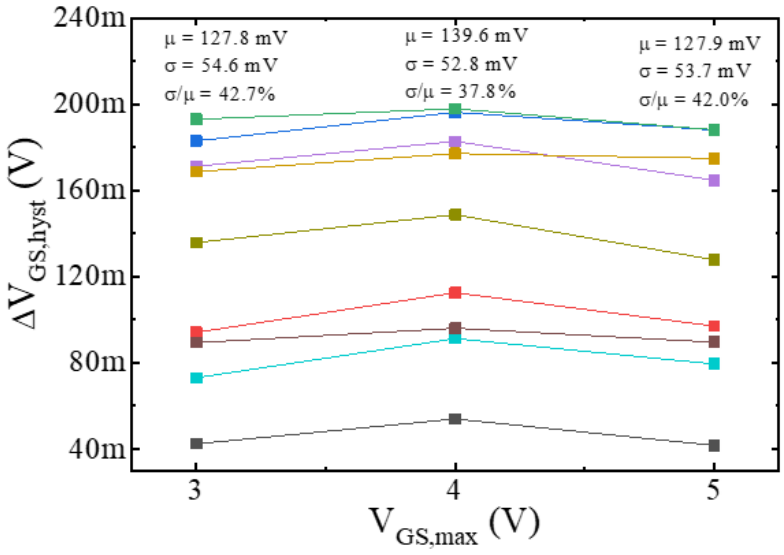

Figure 4.6: $\Delta V_{GS,hyst}$ versus $V_{GS,max}$ across nine samples of GaN-based SGT120R65AL device.

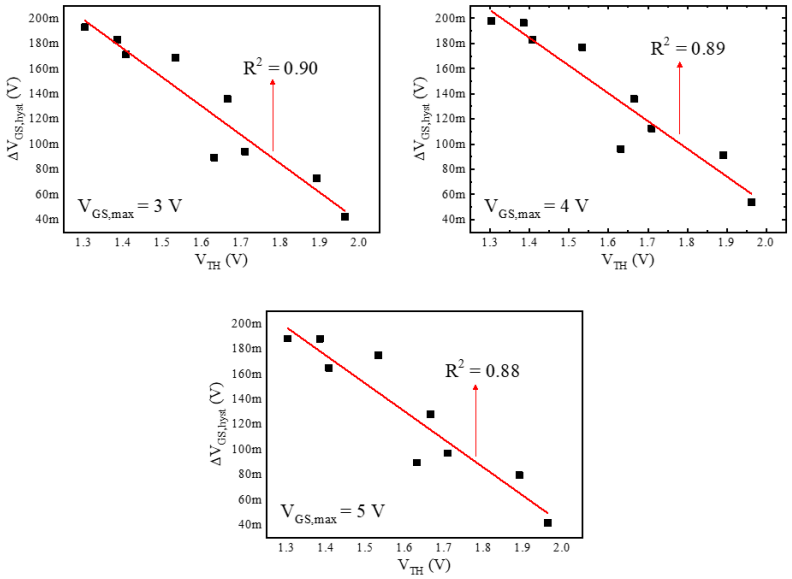

Figure 4.7: $\Delta V_{GS,hyst}$ versus V_{TH} across nine samples of GaN-based SGT120R65AL device.

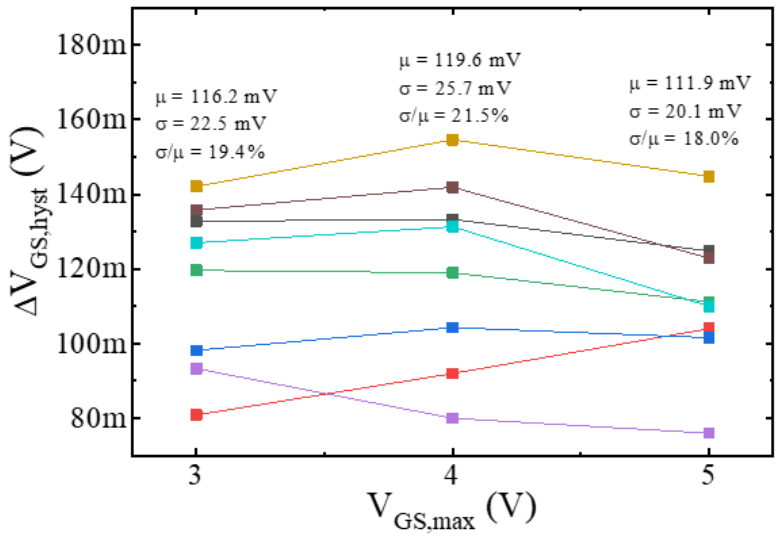

Figure 4.8: $\Delta V_{GS,hyst}$ versus $V_{GS,max}$ across eight samples of GaN-based SGT65R65AL device.

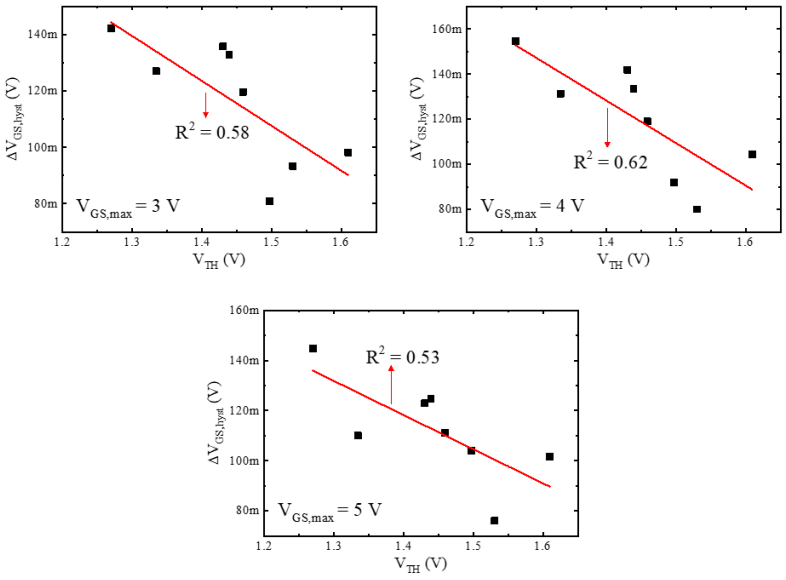

Figure 4.9: $\Delta V_{GS,hyst}$ versus V_{TH} across eight samples of GaN-based SGT65R65AL device.

different trends. Indeed, when moving $V_{GS,max}$ from 3 V to 4 V, some samples exhibit a small increase in $\Delta V_{GS,hyst}$, while others shows a decrease. Moreover, when further increasing the $V_{GS,max}$ up to 5 V, the samples show a decrease in $\Delta V_{GS,hyst}$, with the exception of only one sample. Moreover, the measured hysteresis exhibits a quite relevant sample-to-sample variability of about 20%.

Fig. 4.9 shows the scatter plot of the $\Delta V_{GS,hyst}$ versus the V_{TH}. From this plot, again we can note a quite strong correlation between the two parameters.

4.3 Stress

This section reports and discusses measurements results for all tested devices under positive gate bias stress.

SiC-based SCTH40N120G2V7AG devices

Fig. 4.10 shows the time evolution of the $\Delta V_{GS,stress}$ shift in a log-log plot obtained at different $V_{GS,stress}$ across tested SiC-based samples. The observed positive drift in the order of hundreds millivolts corresponds to an increase of the threshold voltage during the stress phase, which results into a reduction of the drain current. This can be ascribed to the electron trapping from the channel into SiC/oxide interface traps or into bulk oxide traps. From Fig. 4.10, the $\Delta V_{GS,stress}$ expectedly increases when increasing the applied $V_{GS,stress}$, which translates into filling the traps at higher energy levels. We can also note that the measured $\Delta V_{GS,stress}$ in SiC-based devices exhibits a quite low sample-to-sample variability ranging from 1.1% up to 2.8%.

Fig. 4.11 shows the time evolution of the trapping rate parameter defined as

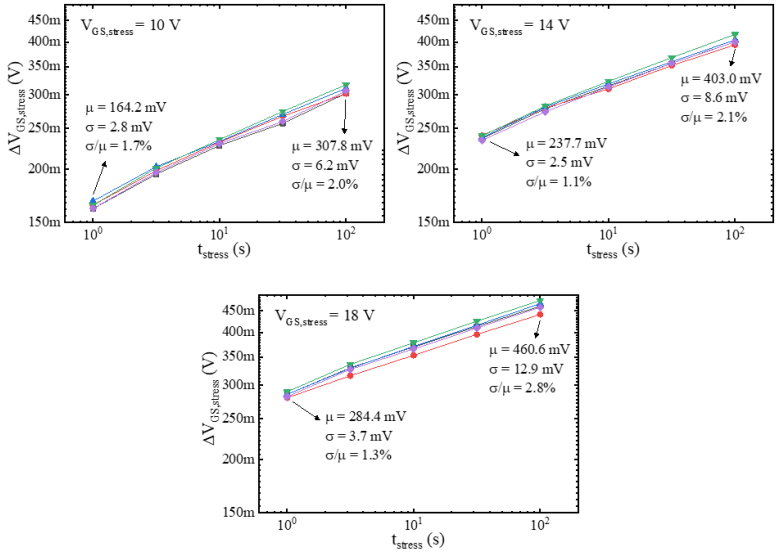

Figure 4.10: Time evolution of the $\Delta V_{GS,stress}$ at different $V_{GS,stress}$ across five samples of SiC-based SCTH40N120G2V7AG device.

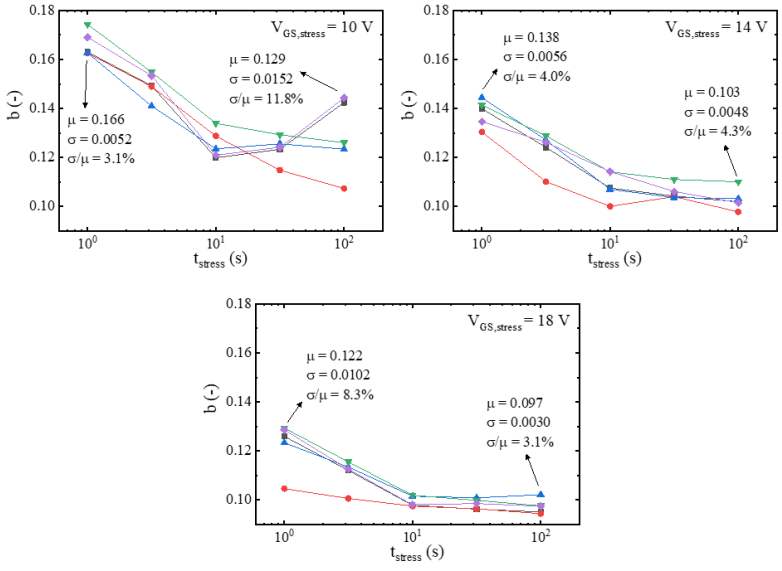

Figure 4.11: Time evolution of the trapping rate parameter b at different $V_{GS,stress}$ across five samples of SiC-based SCTH40N120G2V7AG device.

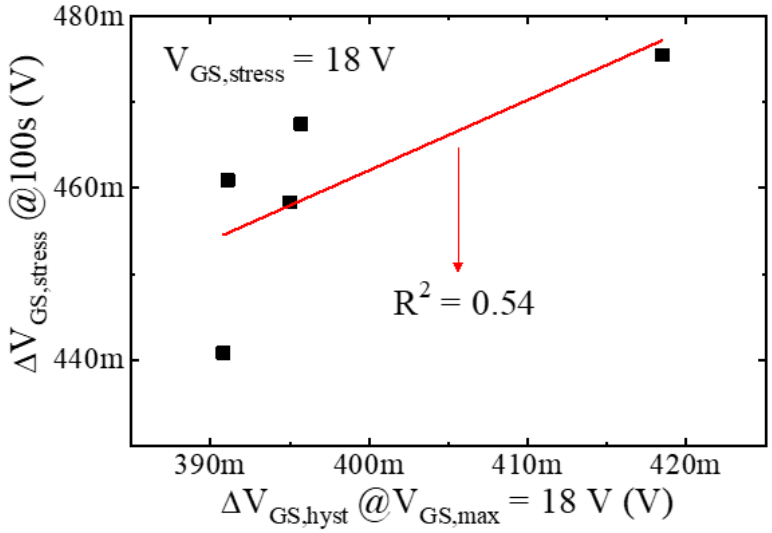

Figure 4.12: $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 18 V versus $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 18 V across five samples of SiC-based SCTH40N120G2V7AG device.

b = d(log($\Delta V_{GS,stress}$))/d(log(t_{stress})), i.e., the slope of the log-log $\Delta V_{GS,stress}$-time curves, at different $V_{GS,stress}$ across tested SiC-based samples. Here, we can observe values ranging from 0.09 up to about 0.17 along with a general decreasing trend over the time, thus indicating that the $\Delta V_{GS,stress}$ shows a tendency towards the saturation for longer stress times rather than following the classical power law evolution. This is the result of filling the existing traps, whereas almost no new traps are created by the applied stress. We can also note that the trapping rate tends to decrease for larger $V_{GS,stress}$. This suggest that the effectiveness of charge trapping mainly depends on the number of available empty traps, which reduces when increasing the stress voltage.

Fig. 4.12 shows the scatter plot of the $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 18 V versus the $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 18 V. From this plot, we can observe a clear and strong correlation between

hysteresis and stress, thus proving that both phenomena are related to the same physical mechanism, i.e., charge trapping at the channel/oxide interface and/or in the bulk oxide.

GaN-based SGT120R65AL devices

Fig. 4.13 shows the time evolution of the $\Delta V_{GS,stress}$ shift in a log-log plot obtained at different $V_{GS,stress}$ across tested GaN-based SGT120R65AL devices. The observed positive is in the order of tens millivolts, again corresponding to a reduction of the drain current during the stress. From Fig. 4.13, differently from what observed in SiC-based devices, the $\Delta V_{GS,stress}$ shows a decreasing trend with increasing $V_{GS,stress}$. We can also note that the measured $\Delta V_{GS,stress}$ exhibits a high sample-to-sample variability ranging from about 50% after 1s of stress down to about 15-20% after 100s of stress.

The anomalous behavior of tested GaN-based devices with respect to SiC-based devices can be further appreciated in Fig. 4.14, which reports the time evolution of the trapping rate parameter b. Differently from SiC-based devices where a general decreasing trend was observed over the time, here we can observe samples for which the trapping rate is almost constant or increaseas during the stress. Also, the trapping rate tends to increase for larger $V_{GS,stress}$ and it shows a larger variability, i.e., 30-40% after 1s of stress and 11-14% after 100s of stress, with b values ranging from 0.35 up to 1.6.

Finally, Fig. 4.15 shows the scatter plot of the $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 3 V versus the $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 3 V. From this plot, differently from what observed in SiC-based devices, we

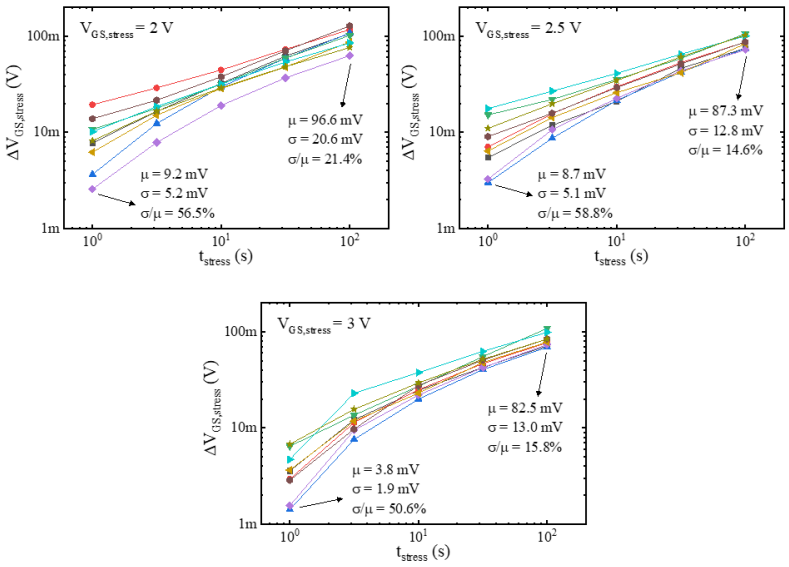

Figure 4.13: Time evolution of the $\Delta V_{GS,stress}$ at different $V_{GS,stress}$ across nine samples of GaN-based SGT120R65AL device.

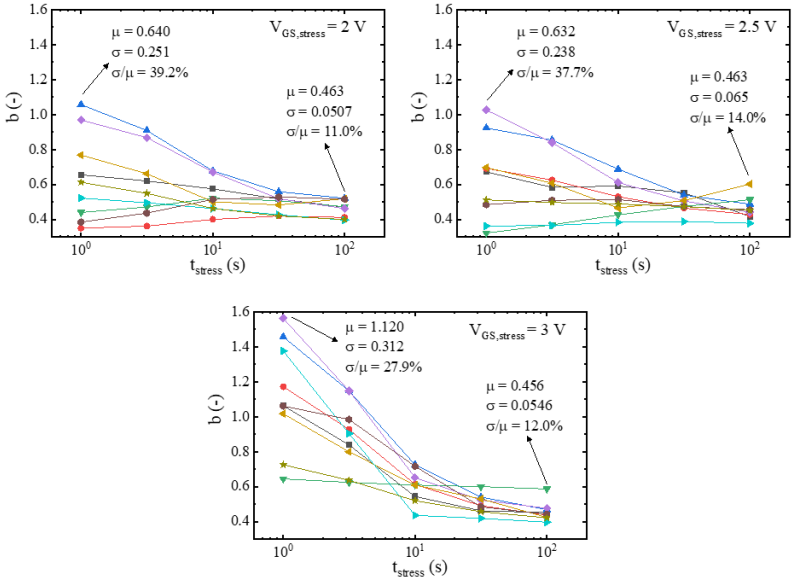

Figure 4.14: Time evolution of the trapping rate parameter b at different $V_{GS,stress}$ across nine samples of GaN-based SGT120R65AL device.

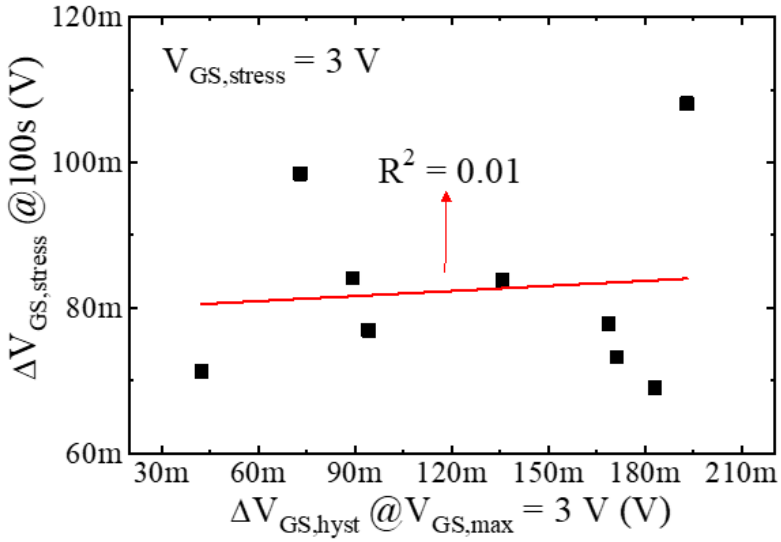

Figure 4.15: $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 3 V versus $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 3 V across nine samples of GaN-based SGT120R65AL device.

can observe no correlation between hysteresis and stress. This likely suggests that in tested GaN-based devices other phenomena besides the charge trapping drive their stress behavior.

GaN-based SGT65R65AL devices

Fig. 4.16 shows the time evolution of the $\Delta V_{GS,stress}$ shift in a log-log plot obtained at different $V_{GS,stress}$ across tested GaN-based SGT65R65AL devices. As in SGT120R65AL devices, the observed positive drift is in the order of tens millivolts, while the $\Delta V_{GS,stress}$ exhibits a slight decreasing trend with increasing $V_{GS,stress}$ and a high sample-to-sample variability ranging from 46-71% after 1s of stress down to about 13-19% after 100s of stress.

Fig. 4.17 reports the time evolution of the trapping rate parameter b. Again, we can observe samples exhibiting an almost constant or increasing b over the

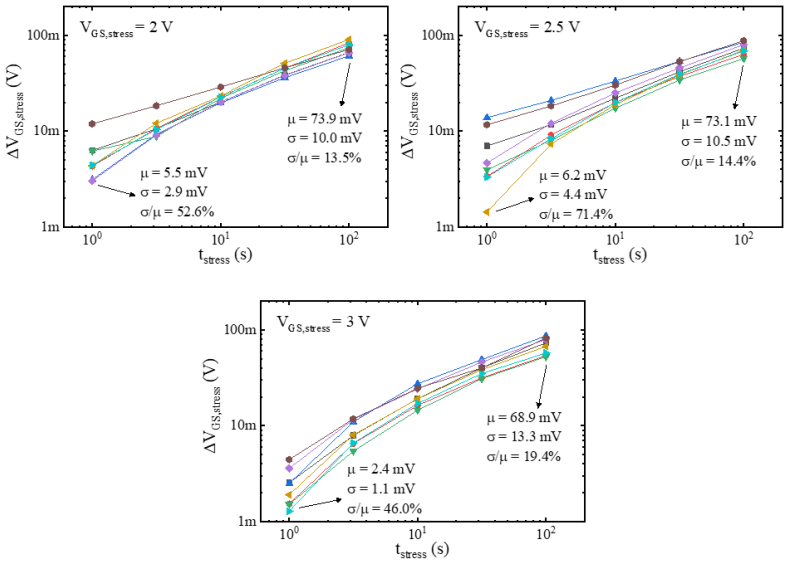

Figure 4.16: Time evolution of the $\Delta V_{GS,stress}$ at different $V_{GS,stress}$ across eight samples of GaN-based SGT165R65AL device.

time, especially at lower $V_{GS,stress}$. As in SGT120R65AL devices, the trapping rate tends to increase for larger $V_{GS,stress}$ and it shows a quite high variability, i.e., 16-50% after 1s of stress and 8-12% after 100s of stress, with b values ranging from 0.3 up to 1.4.

Finally, Fig. 4.18 shows the scatter plot of the $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 3 V versus the $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 3 V. From this plot, similarly to SGT120R65AL devices, no correlation between hysteresis and stress is observed.

4.4 Recovery

This section reports and discusses measurements results for all tested devices under zero or negative gate bias recovery as achieved after the previously performed stress phase.

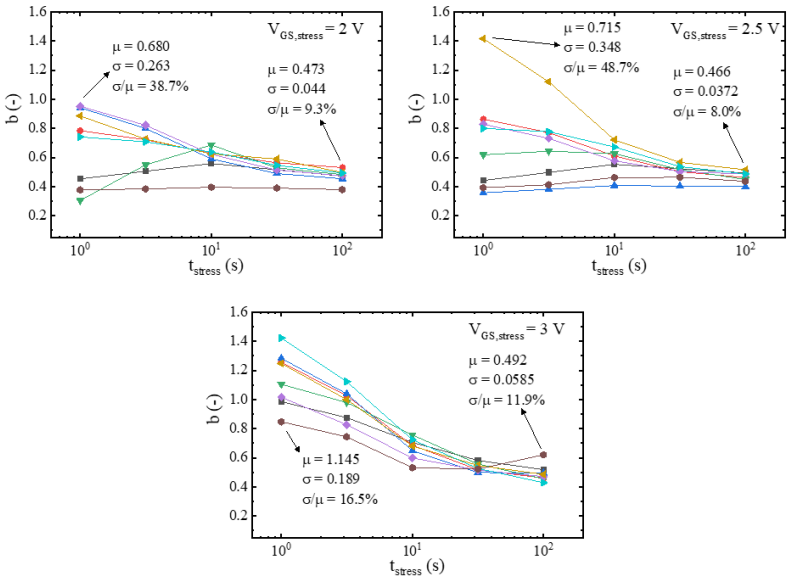

Figure 4.17: Time evolution of the trapping rate parameter b at different $V_{GS,stress}$ across eight samples of GaN-based SGT65R65AL device.

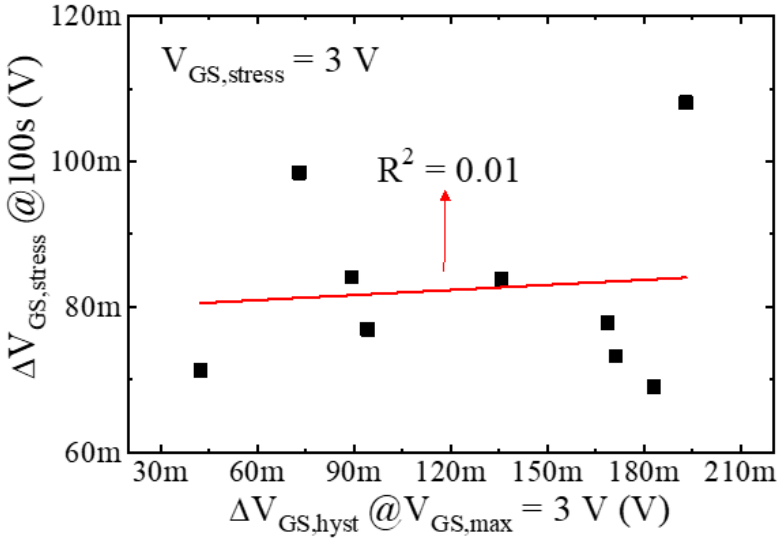

Figure 4.18: $\Delta V_{GS,stress}$ as obtained after 100s of stress at $V_{GS,stress}$ = 3 V versus $\Delta V_{GS,hyst}$ as achieved for $V_{GS,max}$ = 3 V across eight samples of GaN-based SGT65R65AL device.

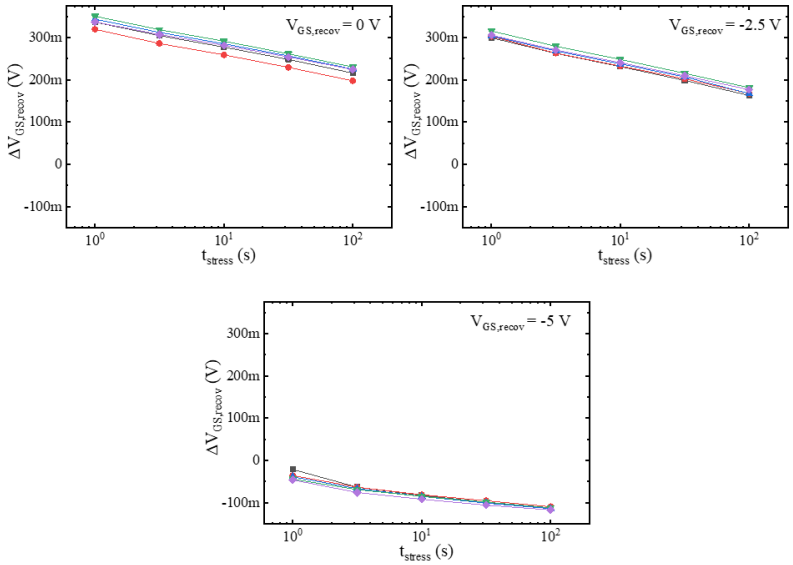

Figure 4.19: Time evolution of the $\Delta V_{GS,recov}$ at different $V_{GS,recov}$ after the stress phase with $V_{GS,stress}$ = 18 V across five samples of SiC-based SCTH40N120G2V7AG device.

SiC-based SCTH40N120G2V7AG devices

Fig. 4.19 shows the time evolution of the $\Delta V_{GS,recov}$ shift in a semilog plot obtained at different $V_{GS,recov}$ across tested SiC-based samples. The observed negative drift corresponds to a decrease of the threshold voltage during the recovery phase, which results into an increase of the drain current. This can be ascribed to the electron detrapping, i.e., the release of the charges prevously trapped during the stress. From Fig. 4.19, such a charge release is faster and more efficient when applying a more negative $V_{GS,recov}$. Overall, experimental data suggests that the stress-induced shift can be fully recovered by applying a proper negative bias voltage, as shown in Fig. 4.19 for a $V_{GS,recov}$ = -5 V leading to a full recovery after only 1 s.

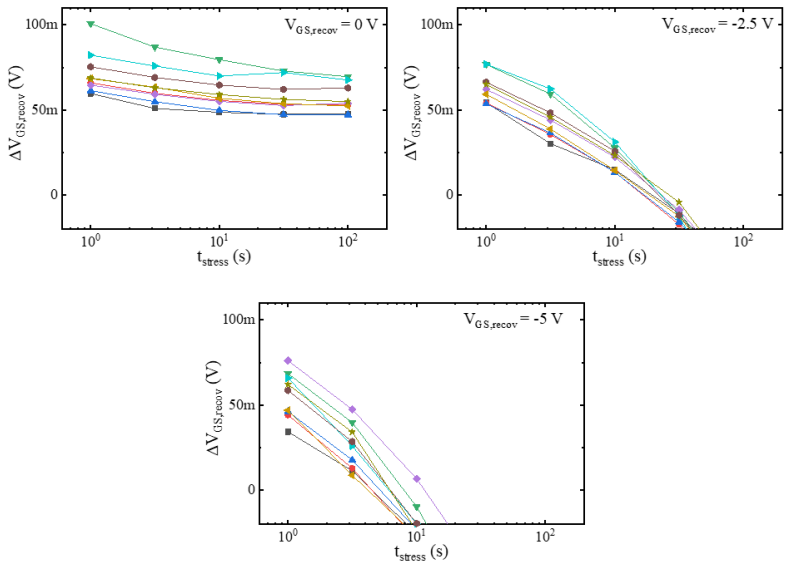

Figure 4.20: Time evolution of the $\Delta V_{GS,recov}$ at different $V_{GS,recov}$ after the stress phase with $V_{GS,stress}$ = 3 V across nine samples of GaN-based SGT120R65AL device.

GaN-based SGT120R65AL devices

Fig. 4.20 shows the time evolution of the $\Delta V_{GS,recov}$ shift in a semilog plot obtained at different $V_{GS,recov}$ across tested GaN-based SGT120R65AL samples. As in SiC-based devices, we can observe a negative drift corresponding to an increase of the drain current and hence a decrease of the threshold voltage during the recovery phase. From Fig. 4.20, the recovery is faster and more efficient when applying a more negative $V_{GS,recov}$. Indeed, while a $V_{GS,recov}$ = 0 V is not sufficient to achieve a full recovery, a $V_{GS,recov}$ = -2.5 V (-5 V) allows for a full recovery within 30 s (15 s) in all tested devices.

GaN-based SGT65R65AL devices

Fig. 4.21 shows the time evolution of the $\Delta V_{GS,recov}$ shift in a semilog plot obtained at different $V_{GS,recov}$ across tested GaN-based SGT65R65AL samples.

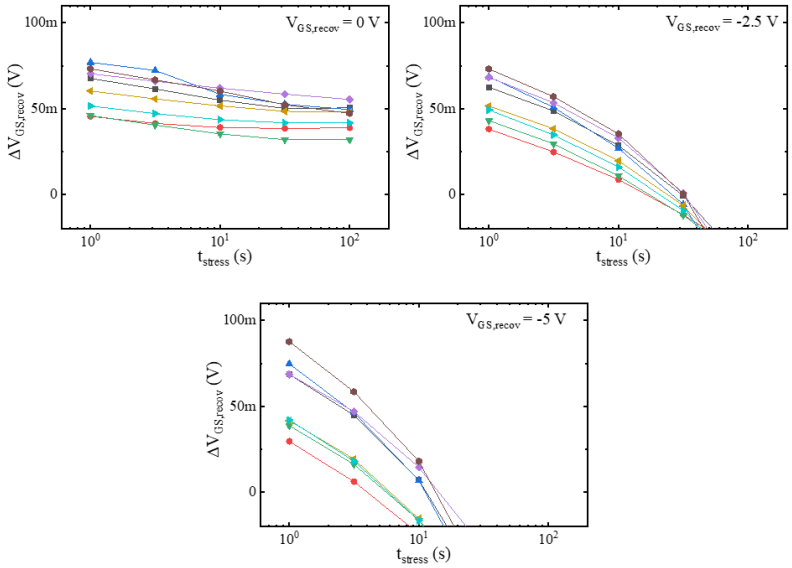

Figure 4.21: Time evolution of the $\Delta V_{GS,recov}$ at different $V_{GS,recov}$ after the stress phase with $V_{GS,stress}$ = 3 V across eight samples of GaN-based SGT65R65AL device.

As in SGT120R65AL devices, we can observe that the recovery is faster and more efficient when applying a more negative $V_{GS,recov}$. Indeed, while a $V_{GS,recov}$ = 0 V is again not sufficient to achieve a full recovery, a $V_{GS,recov}$ = -2.5 V (-5 V) allows for a full recovery within 40 s (20 s) in all tested devices.

Chapter 5

Conclusions

This thesis has explored the properties, performance, and challenges associated with Silicon Carbide (SiC) and Gallium Nitride (GaN) power devices, with a focus on Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). These wide bandgap semiconductors have been shown to offer substantial advantages over traditional silicon-based devices, including higher breakdown voltages, faster switching speeds, and superior thermal performance.

The performed study has provided a comparative analysis of SiC- and GaN-based power MOSFETs in terms of their threshold voltage instability. This was accomplished by performing extensive hysteresis, positive gate bias stress and zero or negative gate bias recovery measurements at room temperature on a set of commercial devices provided by STMicroelectronics.

Experimental results show that both SiC- and GaN-based power devices suffer from hysteresis- and stress-induced shift of the threshold voltage, whose entity depends on the applied stress conditions (i.e., the applied positive gate bias voltage). More specifically, tested SiC-based devices has shown threshold

voltage drifts in the order of hundreds of millivolts, whereas tested GaN-based devices has exhibited drifts in the order of tens of millivolts. Nonetheless, GaN-based devices has shown a quite larger sample-to-sample variability. Furthermore, performed measurements has shown that the stress-induced shift can be fully recovered by applying a proper negative gate bias voltage over the time, thus proving that such a shift is reversible.

While this thesis has provided significant insights into the performance of SiC- and GaN-based power MOSFETs in terms of short-term reliability, there are several areas where further research is needed:

Long-Term Reliability: there is a need for more extensive long-term reliability testing of SiC- and GaN-based devices under various operating conditions. Understanding the mechanisms that lead to device degradation over time is critical for improving their longevity and performance.

Cost Reduction: although the cost of SiC- and GaN-based devices is decreasing, further research into manufacturing processes is necessary to make these devices more economically viable. Advances in material synthesis and device fabrication could lead to significant cost reductions.

Integration with Emerging Technologies: as the demand for high-efficiency power electronics grows, there is an opportunity to integrate SiC- and GaN-based devices with emerging technologies such as other wide bandgap materials and advanced packaging techniques. This integration could lead to even more compact and efficient power systems.

Overall, SiC and GaN MOSFETs represent a significant advancement in the

field of power electronics. Their superior properties, including higher breakdown voltages, faster switching speeds, and better thermal performance, make them ideal candidates for a wide range of applications. While there are some challenges to be addressed, particularly in terms of cost and long-term reliability as discussed above, the potential benefits of these materials are immense. As the technology continues to evolve, it is likely that these materials will play an increasingly important role in the future of power electronics, driving advancements in energy efficiency and system reliability across a variety of industries. The continuous development and integration of SiC and GaN devices will be fundamental for meeting the growing demand for high-performance power systems and supporting the transition to a more sustainable and efficient energy future.

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