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Threshold Voltage Instability in Silicon Carbide Power MOSFET

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Trabajo de titulación de posgrado presentado como requisito para la obtención del título de Magister en Nanoelectrónica.

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Dedication

Dedico a la vida (Dios, Energía del todo, Ciencia o como tu creencia y percepción permitan representar lo inimaginable) que se ha encargado de darme a las personas perfectas en mi camino: mi Mamá Beatriz, mi segunda Mamá Carmen Amelia mi Papá Pedro, mis Hermanos Pedro y Santiago que siempre son un faro en mi viaje de la vida.

RESUMEN

La presente investigación tiene como objetivo comprender la influencia de la tasa de captura de carga en transistores de efecto de campo metal-óxido-semiconductor (MOSFET) de carburo de silicio (SiC), que en la actualidad tienen un interés especial para aplicaciones de alta potencia. Es muy importante el estudio de la confiabilidad de esta nueva generación de dispositivos de alta potencia de acuerdo con las aplicaciones tales como inversores solares, UPS, convertidores CC-CC de alta tensión, fuentes de alimentación de modo de conmutación y controladores de motor, entre otros, donde la alta prioridad es la aplicaciones en las que la vida de los seres humanos tiene una dependencia directa, por ejemplo, la aplicación en el motor del automóvil o del avión. El comportamiento de los MOSFET de SiC muestra una resistencia insuperable por unidad de área, así como un rendimiento de conmutación casi independiente de la temperatura según las hojas de datos de varias compañías de producción, pero esta confiabilidad debe ser verificada por una institución mediadora como la universidad en sus laboratorios respectivos para poder contrastar los resultados proporcionados y asegurar los parámetros de fiabilidad en diferentes entornos. Este estudio universitario ha informado que los MOSFET de alta potencia que se basan en semiconductores de SiC de banda ancha tienen inestabilidad de voltaje de umbral. Las metodologías o métodos que se utilizaron en esta investigación fueron un estudio experimental basado en la histéresis y la inestabilidad de la temperatura de polarización positiva (PBTI). El sistema de medición utilizado, como Probe Station y Temptronic, así como los detalles de conexión en los que dejamos en claro la forma correcta para obtener los datos experimentales, se utilizó el software Keithley en los distintos fines. Las excelentes propiedades térmicas y de cambio de voltaje de umbral presentadas por SiC MOSFET pueden promover muchas mejoras en las capacidades térmicas de la industria en general, lo que significa que es uno de los elementos más importantes en el desarrollo de muchas empresas en todo el mundo y su impacto es muy importante en todos los planos en especial en seguridad, desarrollo y nivel económico.

Palabras clave: BTI, hitéresis, SiC, voltaje umbral.

Abstract

The present research aims to understand the influence of the charge trapping rate in Silicon Carbide (SiC) metal-oxide semiconductor-field-effect-transistors (MOSFETs) which nowadays have special interest for high power applications. It's very important the study of the reliability of this new generation of high power devices according to the applications such as solar inverters, UPS, high voltage DC-DC converters, switch mode power supplies and motor drivers among others, where the high priority are the applications wherein the life of human beings have a directly dependence for instance the application in the car's motor or aircraft' motor. The behavior of SiC MOSFETs shows unsurpassed on-resistance per unit area as well as switching performance almost independent of temperature according to datasheets of various production companies but this reliability has to be verified by a mediating institution like the university in this electronic labs to be able to contrast the results provided and be sure of the parameters of reliability in different environments. This university study has reported that high power MOSFETs which are based on wide bandgap SiC semiconductors have threshold voltage instability. The methodologies or methods which were used in this research were an experimental study based on hysteresis and positive bias temperature instability (PBTI). The measure system used such as the Probe Station and Temptronic as well as the connection details where we made clear about the correct form to obtain the experimental data, the software Keithley was used in the distinct purposes. The outstanding thermal and threshold voltage shift properties presented by SiC MOSFET are able to promote many improvements in the thermal capabilities of the industry in general this means that it's one of most important element in the development of a lot of companies worldwide and its impact are so important at all planes but special in security, developing and economic levels.

Index Terms—BTI, hysteresis, SiC, threshold voltage.

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Chapter 1

Introduction

1.1 Generalities

The present research is according to get the best idea to understand the influence of the charge trapping rate in the new power devices of silicon carbide (SiC) based metal-oxide semiconductor-field-effect-transistors (MOSFETs) which nowadays have special interest due to their bandgap as well as the threshold voltage nature in different temperature and stress environments.

It's very important the study of the reliability of this new generation of high power devices according to the applications such as solar inverters, UPS, high voltage DC-DC converters, switch mode power supplies and motor drivers among others, where the high priority are the applications wherein the life of human beings have a directly dependence for instance the application in the car's motor or aircraft' motor.

Due to the innovative properties of wide bandgap materials and own characteristics the SiC MOSFETs are produced resulting interesting features among the most important: very tight variation of on-resistant vs temperature, very high operation junction temperature capability, very fast and robust intrinsic body diode and low capacitance.

The behavior of SiC MOSFETs shows unsurpassed on-resistance per unit area as well as switching performance almost independent of temperature according to datasheets of various production companies but this reliability has to be verified by a mediating institution like the university in this electronic labs to be able to contrast the results provided and be sure of the parameters of reliability in different environments. This university study has reported that high power MOSFETs which are based on wide bandgap SiC semiconductors have problems of threshold voltage instability [1, 2, 6, 7]

Also the outstanding thermal properties presented by SiC MOSFET are able to promote many improvements in the thermal capabilities of the industry in general this means that it's one of most important element in the development of a lot of companies worldwide and its impact are so important at all levels but special in security, developing and economic levels.

In this project we will present the approach to the reliability of SiC MOSFET in different environments of temperature and voltage stress using an experimental study based on hysteresis and positive bias temperature instability (PBTI) measurements to find a trend and allow get information about the degradation of this device as well as the approximation of behavior in the future in base to Zafar's model.

SiC MOSFET presents higher reduction of its static and dynamic losses in a elevated temperature environmental, higher frequency and higher power density. The own features of this high voltage switches show clearly great benefits.

The enhanced fields such as the passive component of diverse high power control circuit due to the low losses in higher frequencies allow the solution most efficient, cheapest, and compact.

The time to achieve this great solution is above 10 years which started when the manufacturer Infineon [3] made and market launch SiC diodes in 2001 ending in 2011 just after the first productive SiC MOSFETs were market launched by the manufacturer Rodhm and Cree (nowadays know like Wolfspeed).

Since 2012 to nowadays ST Microelectronics, Microsemi, Semikrom, Littelfuse among others are increasing their merchandise for market space in this trench technology was showed that the vertical crystal planes of 4H-SiC provide higher channel mobilities than the first generation of planar n-channel DMOS technologies based on 4H-SiC. Through

1.2 Research interest

The main academic interest of this research is to make a report of the analysis of the obtained data to give a way to understand the impact of charge trapping rate in power MOSFETs based on wide bandgap SiC semiconductors.

Other academic interest is contrast the obtained data whit the well know Zafar's model and explain which are the physical sens with the power devices based on wide bandgap SiC semiconductors.

The main industrial interest given this research is to measure the electrical parameters as well as its behavior in function of temperature, stress time and stress voltage which are the ones that determinate its reliability in different process and its fitness to be used in these. This means that there are a special interest in the economic part because the the new power devices based on wide bandgap SiC semiconductors present great monetary and space savings.

Also and not least the security interest due to these high power devices will become the indispensable elements for many daily tasks on which human well-being depends.

1.3 Methodology used

As has been said the methodologies or methods which were used in this research were an experimental study based on hysteresis and positive bias temperature instability (PBTI) the same will have to be explained with more details in the Chapter 3 wherein need to understand who the results are in base of our obtained data and the specific method.

1.4 Purpose of the research work development

The principal aim of this research is the study of the SiC MOSFET reliability through the process of voltage threshold variation measurement by BTI and hysteresis.

Other main is computed the acquired data to give the right mathematical and physical sense according to the Zafar's Model.

1.5 Outline of This Thesis

The following chapters involves all the process in one well done structure explaining and understanding all the process and considerations during the data acquisition in the experimental study.

The Chapter 1 Introduction as you could see it is the brief summary where it describe the generalities, motivation, research interest, methodology used and the purpose of the research work development.

The Chapter 2 Art of History describe who is developed the SiC material since its first study with own physical features such as the atomic structure and crystallography respective according the different presentation of that. As soon as possible we enter to the history of the high power devices based on wide bandgap SiC semiconductors and finally we presented the SiC MOSFET technology nowadays with its last studies.

The Chapter 3 Experimental Details shows the measure system with the technical data of each equipment used such as the Probe Station and Themtronic as well as the connection details where we made clear about the correct form to obtain the experimental data, at the end of this chapter we boarding the sensing that means to give the setting information used in the software Keithley in the distinct purposes

The Chapter 4 Results and Discussion take account the obtained data in the experimental step to give the respective mathematical and physical description of each event of hysteresis and BTI. Here we apprised the whole acquired data which is computed in the MatLab software and displayed by Origin software.

The explanation that we have given to the Zafar's Model is showed here.

The Chapter 5 Conclusions as well know it is the chapter where we have written the principal developed knowledge during the whole research then here there are the confirmation and the impact level of our project in the academic and industrial fields according our goals.

Chapter 2

State of Art

2.1 The SiC Material

The SiC material is rarely founded in the nature, his synthesis like a compound material containing silicon and carbon was first made by Berzelius in 1824. In 1892, Acheson developed a new process to try to synthesize the SiC from silica, carbon, and some additives. The first industrial application of SiC was cutting, grinding and polishing them the goal of this Acheson process was provided volume production of SiC powders used for that. Using the Acheson process, ingots have small single crystalline SiC platelets (mostly 6H-SiC) can be obtained as a by-product (Figure 2.1). Although these SiC platelets are not pure, they were used for some basic studies on the physical and chemical properties of SiC. In 1907 the first discovery of electroluminescence (emission of yellow light) from SiC by Round which was one of the high lights of this work. At the same time, Moissan discovered natural SiC and investigated this material as a mineral. It is the reason why SiC is called “Moissanite” in mineralogy.

In 1955, Lely successfully grew relatively pure SiC crystals by a sublimation technique (Lely method), with this method we can obtain 6H-SiC crystals mostly , but inclusions of foreign polytypes are often observed.

In the 1960s, the first movement of research into SiC as a semiconductor emerged due to the high crystal quality of the Lely platelets. At the same period, the main target

Figure 2.1: SiC platelets (mainly 6H-SiC) collected as a by-product in the Acheson process [5]

purposes for semiconductor SiC were the evolution of high-temperature devices and blue light-emitting diodes. In this movement there was a lot of researchers like Shockley who cooperated in an international conference on SiC, and highlighted the promise of SiC for high-temperature electronics devices. Several important academic studies on optical properties of SiC were substantially accomplished by Choyke.

In the late 1970s, nonetheless, by virtue of the small size of Lely platelets and unstable material furnishing, research and evolution of SiC semiconductors were mitigated, and the technology continued premature. Contrariwise, polycrystalline SiC technology was developed, and SiC-based ceramics, heating elements, passive components, and thermistors were commercialized.

In 1978–1981, a reproducible process for SiC boule growth was developed by the researchers Tairov and Tsvetkov. They popularized a 6H-SiC seed into a sublimation growth furnace, and pattern a suitable temperature gradient to control mass transport from the SiC origin onto the seed crystal, established on thermodynamic and kinetic considerations. This growth method is named the modified Lely method or seeded sublimation method. A lot of groups followed and promoted developed the growth process to achieve SiC boules with a larger diameter and a decreased density of extended irregularity.

in 1991, Davis and Carter significantly refined the modified Lely method and achieved the first commercialization of SiC(6H-SiC) wafers. Over constants efforts, coherent high-quality SiC wafers, 100–150mm in diameter, are economically accessible from several vendors at present (Figure 2.2). The possibility of single crystalline wafers has induced rapid development of SiC-based electronic devices.

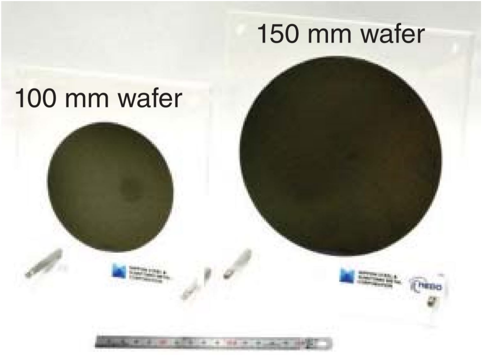


Figure 2.2: 4H-SiC wafers with 100 and 150mm in diamete [5]

In the 1980s, regarding epitaxial growth of SiC, liquid phase epitaxy (LPE)of 6H-SiC on Lely plate was investigated, in studies targeting blue light-emitting diodes. Heteroepitaxial growth of 3C-SiC on a Si substrate by chemical vapor deposition(CVD) was developed in the early 1980s, however the achievement of electronic devices (pn diodes, Schottky barrier diodes (SBDs), MOSFETs) was far under that expected. This effect is associated to a high density of stacking faults and dislocations, which are originated due to considerable inconsistencies in the lattice constants and heated expansion coefficients. Hence, a little number of groups started CVD growth of 3C-SiC on 6H-SiC0001 (Lely or Acheson platelets). Even if the quality of 3C-SiC was much improved, it was not convincing.

In 1987, the high-quality 6H-SiC was developed by the researcher Matsunami and others. who said that 6H-SiC could be homoepitaxially grown by CVD at relatively low growth temperature, while a great amount of degree off-angle is introduced into the 6H-SiC0001 substrates ("step-controlled epitaxy"). The researcher Davis and others described homoepitaxial growth on off-axis substrates of 6H-SiC. Homoepitaxial growth on off-axis 6H-SiC0001 became a standard technical process in the SiC community for the reason that it provided uniformity, high purity, and good doping control.

In 1993, using the Matsunami's technique a high mobility of over 700 [$cm^2V^{-1}s^{-1}$] was first announced for 4H-SiC grown. The consolidation of this result, the other remarkable higher physical properties of Si.

In the mid 1990s, the commercial release of 4H-SiC wafers, and presentation of exceptional 4H-SiC devices made 4H-SiC the main choice for electronic device manufacturing. Meanwhile, exploiting the "site-competition" concept designed by Larkin and others, result in a drastically developed of the doping control. Kordina and others proposed a hot-wall CVD reactor, which design is currently the standard, by this means it allows advanced control of temperature distribution, has a better growth efficiency and longer susceptor life.

2.2 Development of SiC

In 1989, the researcher Baliga advised the exceptional potential of SiC based power devices.

In 1993, Baliga's group published a systematic theoretical analysis of the performance of SiC devices. These papers have inspired engineers and scientists in this field of SiC.

In the early 1990s, as a result of the progress in homoepitaxial growth technology described above,lightly-doped hexagonal SiC epitaxial layers with reasonable quality be came available. Matusetal. reported a1kV6H-SiC pn diode and its rectification operation up to 600C.

In 1993, Urushidanietal demonstrated a 1kV 6H-SiC SBD with a low specific on-resistance and 400C rectification.

In 1994, the on-resistance of high-voltage SiC SBDs was significantly reduced by using 4H-SiC.

In 2001, after structure and process optimization, the first SiC SBD products were released. One of the typical applications of SiC SBDs was as fast diodes employed in a power-factor-correction circuit of switching-mode power supplies. Because of the negligibly small reverse recovery of SiC SBDs, the switching loss can be dramatically reduced and the switching frequency can be increased, leading to the down sizing of passive components. SiC SBDs are currently employed in a broad spectrum of applications, such as industrial motor control, photo voltaic converters, airconditioners,elevators,and traction(subway). In research and development, the maximum blocking voltage of SiC diodes exceeded 20kV.

2.3 SiC Nowadays

High power semiconductors based on Silicon Carbide or Gallium Nitride due to their wide band gap have the great way to improve the power electronics through lower loses, faster switching speeds and higher blocking voltage in contrast to the devices based on silicon.

Silicon carbide is able to present different crystalline structure. There are two hexagonal structures (4H-SiC and 6H-SiC) which are the only ones in the electronic market but exist other new emerging technology on the cubic form 3C-SiC. The hole material have the same features like the high break down field between 2[MV/cm] to 4 [MV/cm] and the high band gap between 2,3[eV] to 3,2[eV] being superior compared to Si.

The principal feature of 3C-SiC, which is a the cubic poly type, is that it's the only one which can be grown on a Silicon substrate, this means that the grow cost of the silicon carbide thickness is reduced. This Technology has the possibility of increasing wafer size faster than the hexagonal poly types could do it.

The Table 2.1 has the comparison of these hexagonal poly types (4H-SiC and 6H-SiC) with the cubic poly type 3C-SiC

Table 2.1: Property 3C-SiC VS 4H-HSiC [3]

Property	SiC	3C-SiC	4H-HSiC	GaN
Band-gap [eV]	1.12	2.35	3.28	3.4
Breakdown field [MV/cm] at $ND = 5x10^{15}/cm^3$	0.3	1.5	2.2	3.5
Intrinsic carrier concentration at 300K$[cm^{-3}]$	$1 * 10^{10}$	$1.5 * 10^{-1}$	$5 * 10^{-9}$	$1 * 10^{-10}$
Electron mobility $[cm^2V^{-1}s^{-1}]$	1350	900	800	2000
Hole mobility $[cm^2V^{-1}s^{-1}]$	480	40	120	200
Saturated electron velocity $[*10^7cms^{-1}]$	1	2	2	2.5
Thermal conductivity $[Wcm^{-1}K^{-1}]$	1.5	3.2	3.7	1.3
Dielectric constant	11.7	9.7	9.6	8.9

By this table we can understand that 3C-SiC and GaN work in the same range of breakdown voltage but 3C-SiC is more suitable for high power applications due to the thermal conductivity while GaN is more suitable to RF applications according to the high saturated electron velocity.

The regarded feature is the narrow band gap of 3C-SiC (2.3[eV]) and 4H-SiC (3.28[eV]) which is the the principal advantage. The reduced density of states at the $SiO_2/3C-SiC$ interface as a result of the lowering of the conduction band minimum. Hence, the highest channel mobility of above $300cm^2/(V * s)$ demonstrated by Metal Oxide Semiconductor Field Effect Transistor (MOSFET) based on 3CSiC achieved a remarkable reduction in the power consumption.

An additional benefit of 3C-SiC/Si in front of 4H-SiC is the much lower Temperature Coefficient of Resistance. This allow a large reduction of device on-resistance at realistic junction temperatures for power device operation. The potential electrical activity of extended defects in 3C-SiC is a concern for electronic device functionality comparatively with the 4H-SiC. This mechanisms of defects formation are been understanding as well as the methods for their reduction developed to accomplish viable commercial yields [3].

As a typical figure showed in a lot of researches (see Fig. Figure 2.3) for power devices tell us that SiC is ten times better than Si in terms of device on resistance for a given operating voltage also in power density per unit area. Nowadays 4H-SiC is the preferred material but its principal limitation is the low channel mobility of carriers, which reduce the performance of the MOSFET switch used in high power applications. Especially In the region below a breakdown voltage of 800 V this limitation is extremely important where DC-DC converters and DC-AC inverters are needed for electric vehicles or hybrid cars.

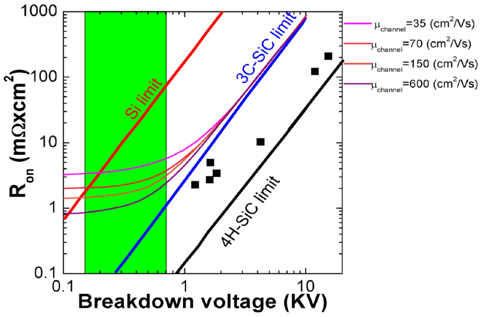


Figure 2.3: A figure caption beneath the figure for description of the depicted concept which sometimes can be very long

In the actuality there are a lot of improvements in the process to get the material of SiC with the best features such as in the different presentations of crystals but also there are many research by the industry to improve the actual material distribution inside the device which was selected since 2001 with the SiC diodes that allow us diverse kind of structures for instance the purpose of a trench SiC MOSFET based on a novel asymmetric concept in stead of the commonly planar cell in Si MOSFET

Chapter 3

Experimental Details

3.1 Phenomenon to be Measured

As we said in the introduction here we going to talk about method to measure and the process to calculate the respective values presented in the next chapters but first we need to understand the phenomenon to be measured which is explained below using one example of SiC power MOSFET manufactured with 4H-SiC.

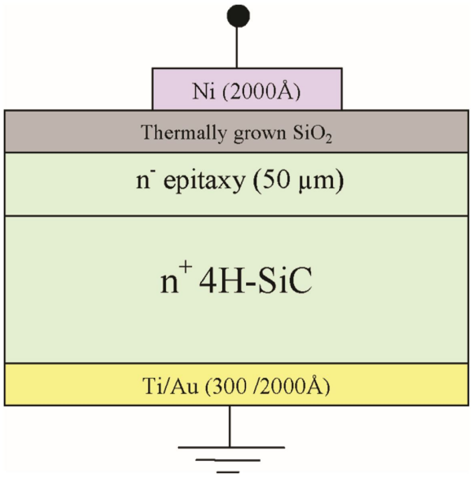


Figure 3.1: Schematic of metal oxidesilicon carbide structure [4]

The phenomenon is into the gate stack this dielectric charging is the process by which charges tunnel into the dielectric layer and become trapped, screening the applied potential and hindering device operation. The exact physics of dielectric charging are not fully understood.

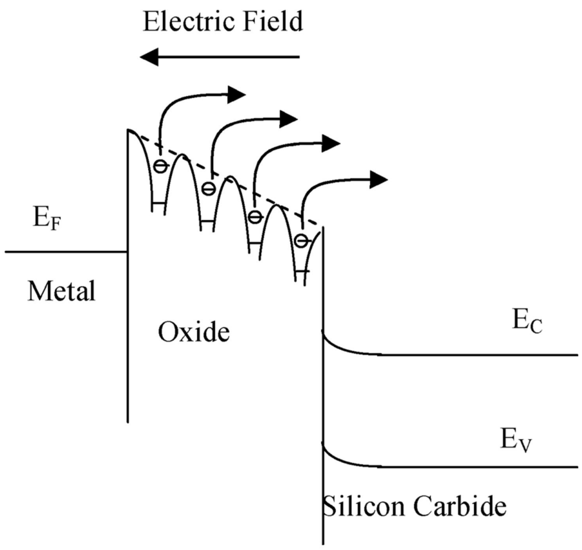


Figure 3.2: Energy band diagram for Poole– Frenkel conduction in MOSiC structure having multiple Coulombic traps [4]

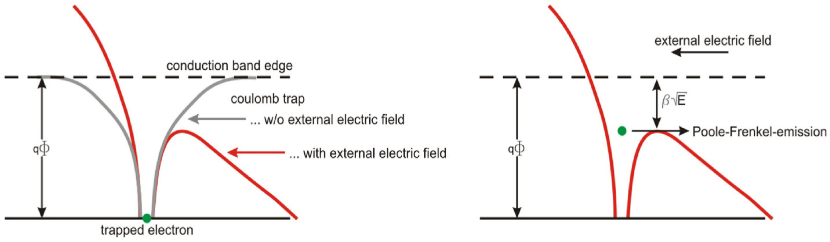


Figure 3.3: Illustration of the Poole-Frenkel-effect/Poole-Frenkel-emission. Left: The conduction band edge and energetic trap geometry changes at the transition from the equilibrium state to the application of an external electric field. Right: The external electric field leads to an effective reduction of the potential barrier, and the trapped electron has a higher possibility to escape from the trap state into the conduction band. [9]

The Poole-Frenkel-effect (PFE) is used if the trap center is neutral with the captured carrier (e^-,h^+) as only then an attractive (coulomb) interaction is working when the charged carrier escapes from the then charged trap! The general mechanism of the PFE is sketched Figure 3.4: The barrier $e_0\Phi_{tn} = |E_C - E_{tn}|$ for an electron to escape from its trap at energy level E_{tn} into the conduction band (and a barrier $e_0\Phi_{tp} = |E_{tp} - E_V|$ for a hole to escape into the valence band, respectively) is equal in both directions in this simplified linear model for the field-free state ($F = 0$). This is changed by the presence of an electric field ($F \neq 0$): In forward direction (in our case, the direction of the drift of the electrons), the barrier is diminished by $\Delta\Phi_{PF}$ compared to the field free state by the applied and/or internal electric field F with appropriate sign. A field with the opposite sign enlarges the barrier in the same direction by about the same value. Usually, the coulomb interaction between the leaving carrier and remaining charged trap is used. Therefore, the barrier reduction $\Delta\Phi_{PF}$ is similar to that for the Schottky effect (SE) in the thermionic emission with an electric field present. The difference is that the trap is localized (spatially fixed) while in the Schottky emission both interacting charges are moving [8].

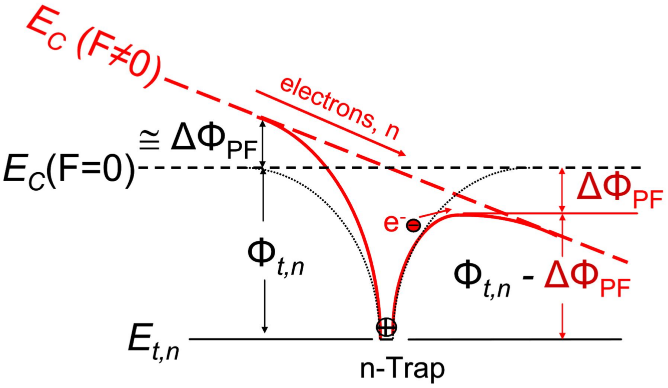


Figure 3.4: Schematic sketch of the Poole-Frenkel-effect without and with electric field. (POSITIVELY CHARGED BY DETRAPPING) [8]

3.2 Measure System

Firs we have to present the two SiC power devices which are going to be measured.

3.2.1 SCT30N120 Power SiC MOSFET

Silicon carbide Power MOSFET 1200V, 45A, 90 mΩ (typ., TJ = 150 °C) in an HiP247^{TM} package:

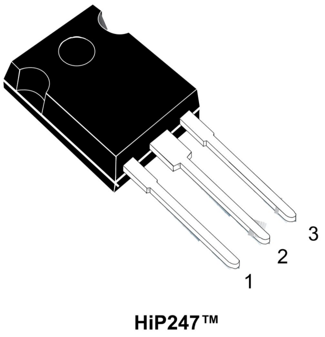


Figure 3.5: SCT30N120 Power SiC MOSFET

Table 3.1: SCT30N120 Power SiC MOSFET Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 25	V
I_D	Drain current (continuous) at TC = 25°C (limited by die)	45	A
I_D	Drain current (continuous) at TC = 25°C (limited by package)	40	A
I_D	Drain current (continuous) at TC = 100°C	34	A
I_{DM}	Drain current (pulsed)	90	A
P_{TOT}	Total dissipation at TC = 25 °C	270	W
T_{stg}	Storage temperature range	-55 to 200	°C
T_j	Operating junction temperature range	-55 to 200	°C

3.2.2 SCT50N120 Power SiC MOSFET

Silicon carbide Power MOSFET 1200 V, 65 A, 59 mΩ (typ., TJ=150 °C) in an HiP247^{TM} package

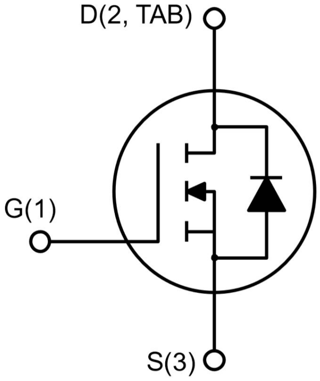


Figure 3.6: SCT50N120 Power SiC MOSFET

Table 3.2: SCT50N120 Power SiC MOSFET Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 25	V
I_D	Drain current (continuous) at TC = 25°C (limited by die)	65	A
I_D	Drain current (continuous) at TC = 100°C (limited by package)	50	A
I_D	Drain current (continuous) at TC = 130°C	34	A
I_{DM}	Drain current (pulsed)	130	A
P_{TOT}	Total dissipation at TC = 25 °C	318	W
T_{stg}	Storage temperature range	-55 to 200	°C
T_j	Operating junction temperature range	-55 to 200	°C

3.2.3 Probe Station

The probe station that has been used is similar to the Figure 3.7 with the following model in Table 3.3.

Table 3.3: Probe Station characteristic

CASCADE MICROTCH	
MODEL	SUMMIT 11861B
S/N	427320403

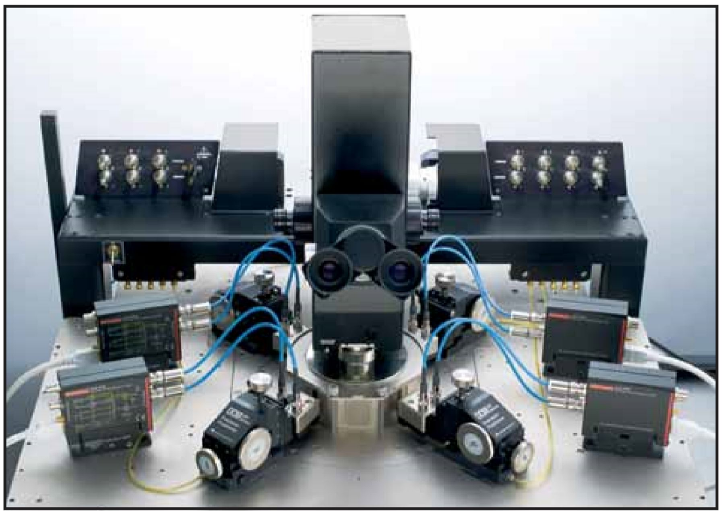


Figure 3.7: Probe Station

3.2.4 Semiconductor Characterization System 4200SCS

Semiconductor Characterization System Figure 3.8 which characterizes are presented in Table 3.4 was used in this research project.

The 4200-SCS supports many instrument configurations that can include SMUs, C-V measurement units, ultra-fast I-V modules, pulse generators, and oscilloscopes. The standard configuration includes two medium power Source-Measure Units (SMUs) and a Ground Unit.

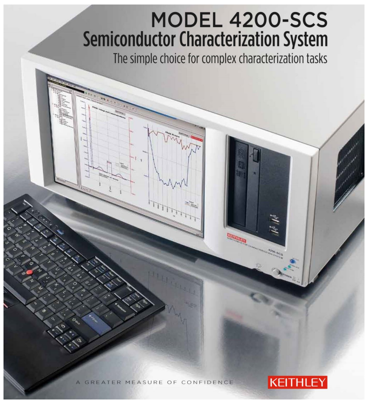


Figure 3.8: Probe Station

Table 3.4: Probe Station characteristics

Standard 4200-ScS models	
4200-SCS/F	9 slot chassis with integrated controller 12.1 inch flat panel display Two (2) Model 4200-SMU medium power SMUs One (1) Remote Sense Ground Unit LAN, GPIB, USB, RS-232, parallel port, hard disk, DVD/CD-RW

The 4200-SCS is modular, configurable and upgradeable; four core measurement modules can be mixed and matched in the nine instrument slots.

Up to nine precision DC Source-Measure units can supply voltage or current and measure voltage or current from 0.1fA to 1A and from $1_{\mu}V$ to 210V.

AC Impedance testing is easy with the Model 4210-CVU Multi-Frequency C-V Module, at test frequencies from 1 kHz to 10MHz. Capacitance from nF to uF can be measured.

Pulse and transient measurements can be performed with the Model 4225-PMU UltraFast I-V module. This module has two independent voltage sources that can slew the voltage at 1V/ns while simultaneously measuring both the voltage and the current.

When multiple modules are installed, they are internally synchronized to less than 3ns

Figure 3.9: 4200SCS Semiconductor Characterization System Distribution

a) Configurable with from two to nine SMUs and optional sub-femtoamp Remote PreAmps.

b) 4210-CVU Card for multi-frequency C-V testing.

c) Dual-channel ultra-fast I-V module supports pulse I-V testing and other pulse applications.

d) Two LAN Ethernet ports and USB ports.

e) Low noise ground unit with remote sense.

3.2.5 DC Source-Measure Unit (SMU)

The basic SMU circuit configuration is shown in Figure 3.10. The SMU operates as a voltage or current source (depending on source function) in series with an I-Meter, and connected in parallel with a V-Meter. The voltage limit (V-limit) and current limit (I-limit) circuits limit the voltage or current to the programmed compliance value. In this local sensing example, the SMU FORCE terminal is connected to device-under test (DUT) HI, while the DUT LO is connected to COMMON.

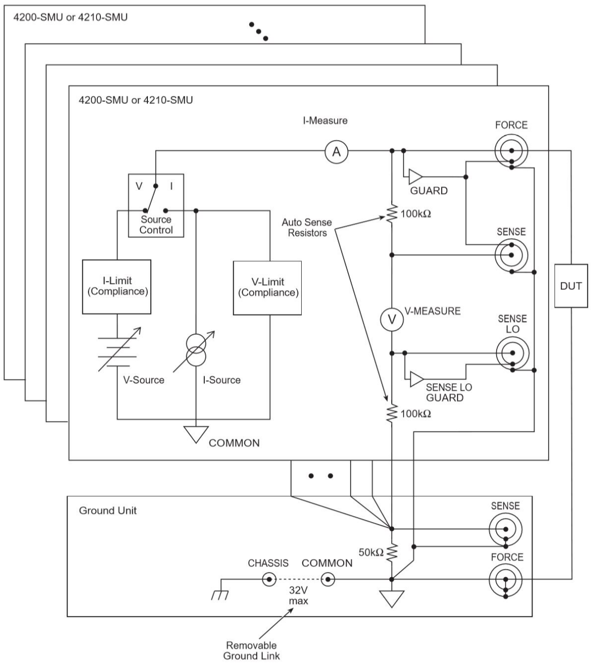


Figure 3.10: Basic SMU source-measure configuration

3.2.6 PreAmp terminals and connectors

The locations and configuration of the Model 4200-PA terminals are shown in Figure 3.11. Basic information about these terminals is summarized below:

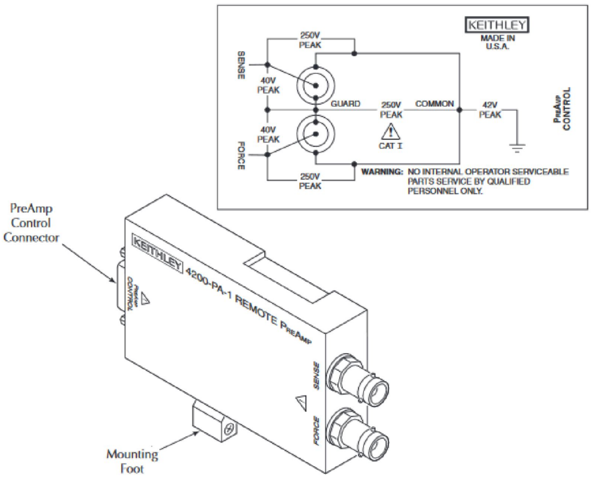


Figure 3.11: PreAmp terminals and connectors

FORCE terminal

The FORCE terminal is a standard triaxial connector used to apply the preamp

FORCE signal to the DUT.

⟶ The center pin is FORCE.

⟶ The inner shield is GUARD.

⟶ The outer shield is circuit COMMON

SENSE terminal

The SENSE terminal is a standard triaxial connector used to apply the preamp SENSE signal to the DUT in a remote sense application.

⟶ The center pin is SENSE.

⟶ The inner shield is GUARD.

⟶ The outer shield is circuit COMMON.

3.3 Connections details

The Figure 3.12 is a photograph taken at the time of measurement, where we presented the easy connection to SMU1(GATE), SMU2(DRAIN) and SMU3(GROUND).

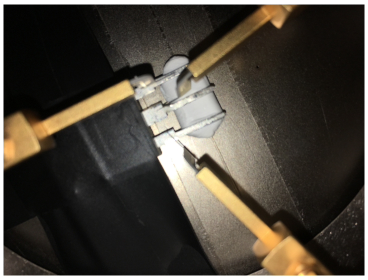


Figure 3.12: Probe Station

3.4 Sensing and Data Acquisition

The first step to sensing is put the electrical characteristic to initial point as close as possible to the fresh curve (device never used) to take as reference point for all measurements below like Figure 3.13, this step is to stabilize the device. The way to get the same initial electrical characteristic without trapping charge is put to -1[v] during 10[s] before each measure.

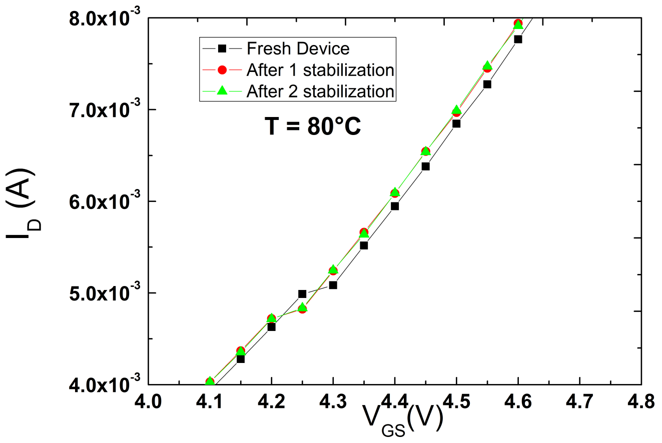


Figure 3.13: SiC Power MOSFEST Stabilization: Black(stabilized curve), Green (Fresh Curve).

Next we need to use the Keithley Interactive Test Environment (KITE) which is the main software component of the KTE Interactive software tool set. KITE is the primary user interface for the Keithley Instruments Model 4200 Semiconductor Characterization System (SCS). KITE is a versatile tool that facilitates interactive characterization of an individual parametric test device or automated testing of an entire semiconductor wafer.

The KITE application consists of a variety of graphical user interfaces (GUIs) that allow you to do the following:

◊ Customize existing / supplied interactive test modules (ITMs) or create new ITMs from existing templates.

◊ Create UTMs from supplied or user-programmed C-code modules.

◊ Automatically execute tests and associated operations (switch matrix connections, probe movements, and so on), including:

a. A single test for one selected device (transistor, diode, resistor, capacitor, and so on).

b. A sequence of tests for one selected device.

c. A sequence of tests for multiple devices, for example, all of the devices contacted by a probe at a given touchdown or subside location on a semiconductor wafer.

View test results numerically and graphically.

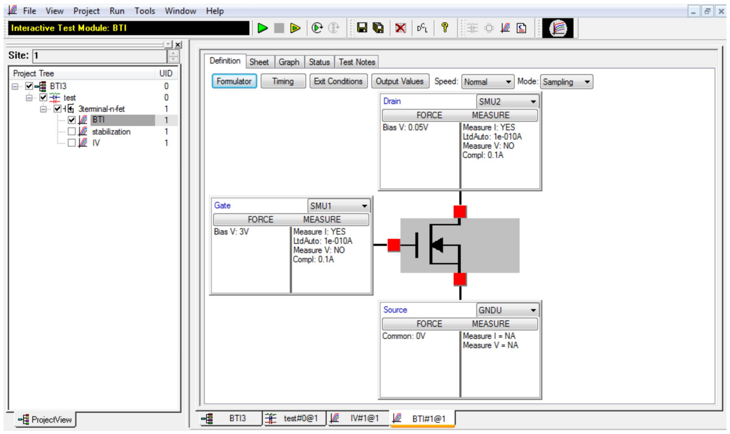
◊ Analyze test results using built-in parameter extraction tools.

◊ View the analysis results numerically and graphically.

◊ Interactively build and edit test / execution sequences using the project navigator.

General Settings

The Figure 3.14 present the settings in the software Keithley interactive test environment in the general process.



Site: 1

Project Tree	UID
☑ BTI3	0
☑ test	0
☑ 3terminal-n-fet	1
☑ BTI	1
☐ stabilization	1
☐ IV	1

Speed: Normal
Mode: Sampling

Drain SMU2
Bias V: 0.05V
Measure I: YES
LtdAuto: 1e-010A
Measure V: NO
Compl: 0.1A

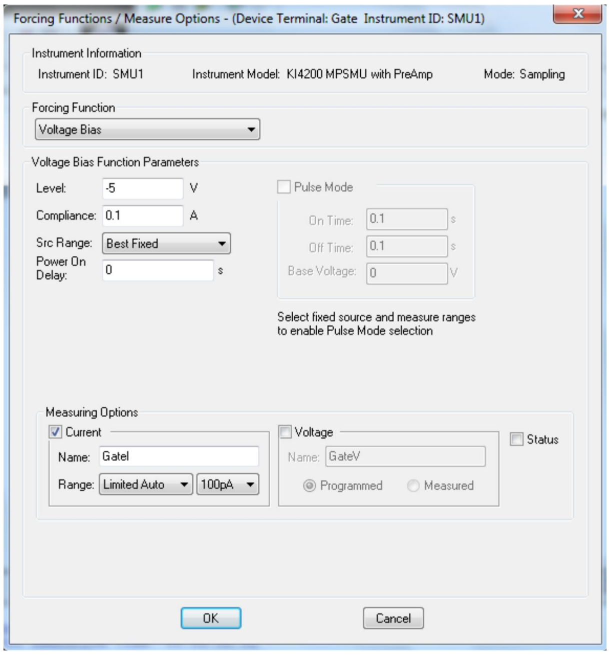
Gate SMU1
Bias V: 3V
Measure I: YES
LtdAuto: 1e-010A
Measure V: NO
Compl: 0.1A

Source GNDU
Common: 0V
Measure I = NA
Measure V = NA

Figure 3.14: General Settings of the measure process

Stabilization Settings

The Figure 3.15 present the settings in the software Keithley interactive test environment in stabilization phase.



Forcing Functions / Measure Options - (Device Terminal: Gate Instrument ID: SMU1)

Instrument Information

Instrument ID: SMU1
Instrument Model: KI4200 MPSMU with PreAmp
Mode: Sampling

Forcing Function: Voltage Bias

Voltage Bias Function Parameters

Level: -5 V
Compliance: 0.1 A
Src Range: Best Fixed
Power On Delay: 0 s

☐ Pulse Mode
On Time: 0.1 s
Off Time: 0.1 s
Base Voltage: 0 V

Select fixed source and measure ranges to enable Pulse Mode selection

Measuring Options

☑ Current
Name: GateI
Range: Limited Auto 100pA

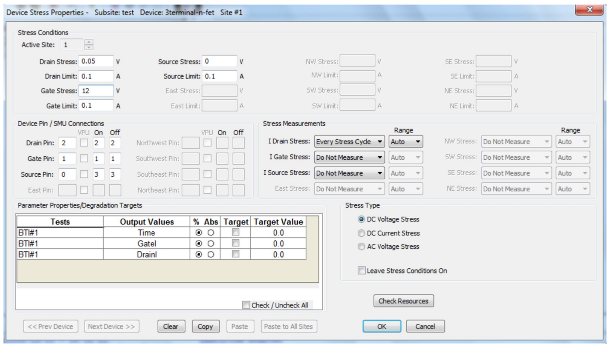
☐ Voltage
Name: GateV
● Programmed ○ Measured

☐ Status

Figure 3.15: Stabilization Settings

PBTI Settings

The Figure 3.16 present the settings in the software Keithley interactive test environment in PBTI phase.



Device Stress Properties - Subsite: test Device: 3terminal-n-fet Site #1

Stress Conditions

Active Site: 1

Drain Stress: 0.05 V
Drain Limit: 0.1 A
Gate Stress: 12 V
Gate Limit: 0.1 A
Source Stress: 0 V
Source Limit: 0.1 A

Device Pin / SMU Connections

		VPU	On	Off
Drain Pin:	2	☐	2	2
Gate Pin:	1	☐	1	1
Source Pin:	0	☐	3	3

Stress Measurements

		Range
I Drain Stress:	Every Stress Cycle	Auto
I Gate Stress:	Do Not Measure	Auto
I Source Stress:	Do Not Measure	Auto
East Stress:	Do Not Measure	Auto
NW Stress:	Do Not Measure	Auto
SW Stress:	Do Not Measure	Auto
SE Stress:	Do Not Measure	Auto
NE Stress:	Do Not Measure	Auto

Parameter Properties/Degradation Targets

Tests	Output Values	%	Abs	Target	Target Value
BTI#1	Time	●	○	☐	0.0
BTI#1	GateI	●	○	☐	0.0
BTI#1	DrainI	●	○	☐	0.0

☐ Check / Uncheck All

Stress Type

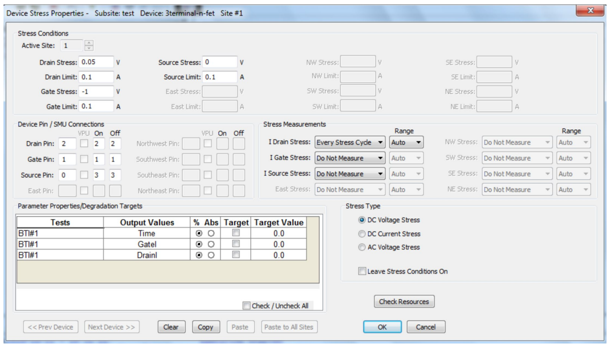
● DC Voltage Stress
○ DC Current Stress
○ AC Voltage Stress

☐ Leave Stress Conditions On

Figure 3.16: PBTI Settings

Recovery Settings

The Figure 3.17 present the settings in the software Keithley interactive test environment in recovery phase.



Device Stress Properties - Subsite: test Device: 3terminal-n-fet Site #1

Stress Conditions

Active Site: 1

Drain Stress: 0.05 V

Drain Limit: 0.1 A

Gate Stress: -1 V

Gate Limit: 0.1 A

Source Stress: 0 V

Source Limit: 0.1 A

Device Pin / SMU Connections

	VPU	On	Off
Drain Pin: 2	☐	2	2
Gate Pin: 1	☐	1	1
Source Pin: 0	☐	3	3

Stress Measurements

		Range
I Drain Stress:	Every Stress Cycle	Auto
I Gate Stress:	Do Not Measure	Auto
I Source Stress:	Do Not Measure	Auto

Parameter Properties/Degradation Targets

Tests	Output Values	%	Abs	Target	Target Value
BTI#1	Time	●	○	☐	0.0
BTI#1	GateI	●	○	☐	0.0
BTI#1	DrainI	●	○	☐	0.0

Stress Type

● DC Voltage Stress

○ DC Current Stress

○ AC Voltage Stress

☐ Leave Stress Conditions On

Figure 3.17: Recovery Settings

3.4.1 PBTI in MOSFETs

The instability of the threshold voltage VTH of a MOSFET subsequent bias temperature stress (BTS) is a reliability problem universal to all variants of the device and independent of the semiconductor material. In appropriate, MOSFETs based on silicon carbide (SiC) also experience from this issue. While there is large research, tackling the effect on silicon (Si) based devices, only narrow information is accessible for SiC based MOSFETs.

The bias temperature instability (BTI) block the applicability of SiC power MOSFETs. The principal cause occurs to be electron trapping into preexisting traps in the oxide layer], where the brand and nature of these defects remains debated.

By achieving a large research of the drain current instability at use conditions and the bias temperature instability (BTI) on a variety of four-layer-hexagonal SiC devices and a wide temperature narrow from -60°C to 250°C, we find crucial particulars of the trapping mechanisms of electrons into SiO2. We then interconnection derive with the buildup knowledge from the advance of processes distributed in activation energy and charge trapping into SiO2 layers on silicon. This provides a valuable insight into the root cause of this instability mechanism and serves as a starting point for atomic scale calculations for point defect charging in SiO2 near the SiC interface.

Positive Bias Temperature Instability (PBTI) occurs in n-MOSFETs when the gate of the device is made positive with relation to other terminals. PBTI causes negative charges in the gate insulator and results in positive ΔV_{th}.

The assessment of BTI induced MOSFET parametric degradation were done by stressing the device at an accelerated aging condition, using a gate bias (VG) that is higher ($V_G = V_G - V_{STR}$) than that used during normal operation. The degradation in MOSFET drain current can be continuously monitored as the gate is being stressed.

The measurements are performed by interrupting the stress at certain predefined times, the interruptions are spaced in logarithmic intervals of time, and the time evolution of BTI induced shift in MOSFET parameters is estimated. The accelerated stress test were performed up to several seconds.

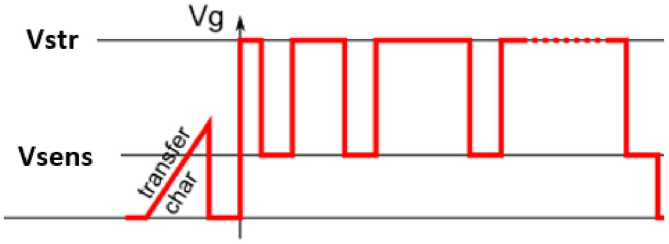


Figure 3.18: The measure sequence interrupts the stress by switching to the VTH of the device in logarithmically increasing intervals.

The recovery step is equal to the PBTI but using negative V_{STRESS}. as we can see in Figure 3.19.

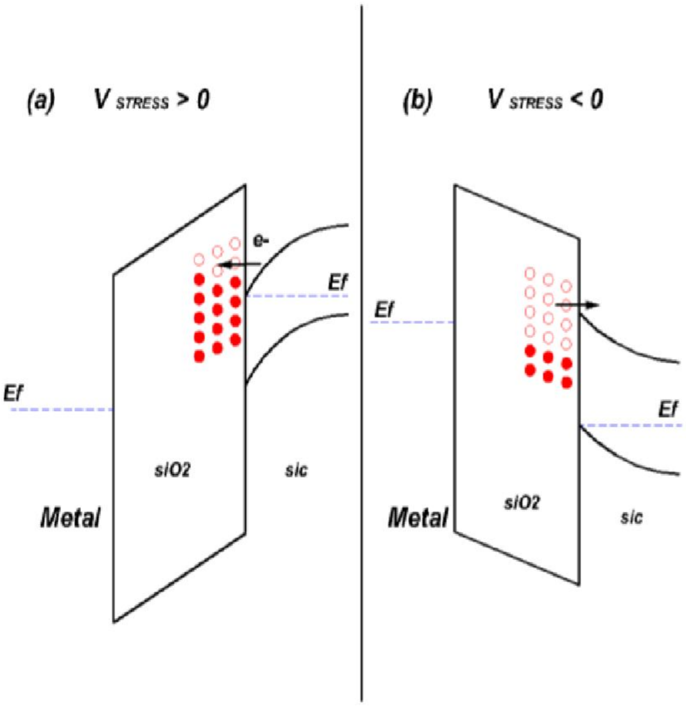


Figure 3.19: Band diagram for the stress phase (a) and the recovery phase (b)

Chapter 4

Results and Discussion

4.1 PBTI's Results

The PBTI was developed because $high - k$ films present considerable charge trapping. This charge trapping is the reason that the threshold voltage shift with different stressing time become an important transistor reliability issue, which is unlike to the SiO_2 films.

Threshold voltage depended of on stressing time and with positive bias stress voltage and temperature the injected the charge density is investigated as a function of this voltage and temperature.

The stack of gate dielectric of typical MOSFET is constituted of interfacial oxide layer at the Si substrate and $high - k$ films but the in the SiC MOSFET the SiC replaces the Si.

4.1.1 $I_D - V_{GS}$ curves shift

The Figure 4.1 is the PBTI's result in the first SiC power MOSFET (SCT50N120) which present the $I_D - V_{GS}$ curves shift at different temperatures (20°C, 50°C, 100°C and 150°C), therefore we can observe a displacement of V_{th} toward the left it means a diminution of this for temperature increase.

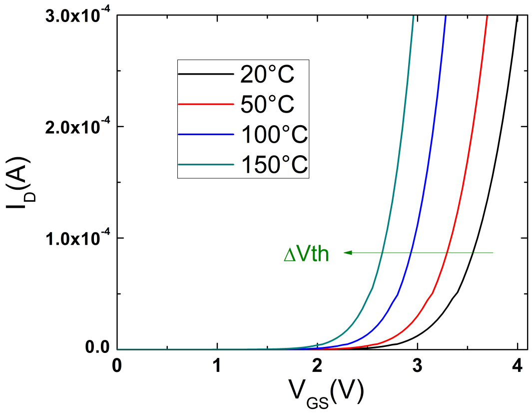


Figure 4.1: The $I_D - V_{GS}$ curves shift for different temperatures

In base of acquired data of Table 4.1 belonging to the Figure 4.2 which was obtained from the Figure 4.1 where we use the $I_D = 0.1[mA]$ to calculate the V_{th} respective to each temperature (20°C, 50°C, 100°C and 150°C) and get a best point of view. This behavior present the threshold voltage shift towards the left (decrease) when the temperature increase then it means that the features of ON are better at high temperature as its ON-resistance.

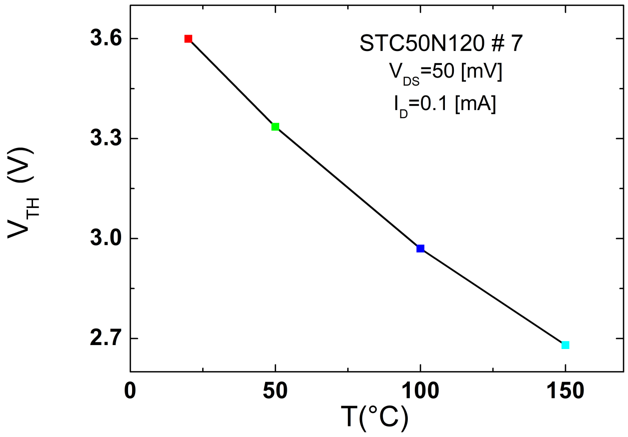


Figure 4.2: The V_{th} for different temperatures

Table 4.1: V_{th} in different temperatures

Temp °C	Vth
20	3.599
50	3.335
100	2.969
150	2.680

4.1.2 PBTI to Different Stress Voltages

The Figure 4.3 and Table 4.2 present the PBTI's results of the SiC Power MOSFET for different stress voltages (8[v], 12[v], 16[v], and 20[v]) at constant temperature (Tem=100°C) and with $V_{DS} = 50[mV]$ where we get an ascending behavior of ΔV_{th} in function of the logarithmic time.

The Figure 4.3 also present the increase of charging traps which means the rise of ΔV_{th} while increment the stress voltage and in a long time too.

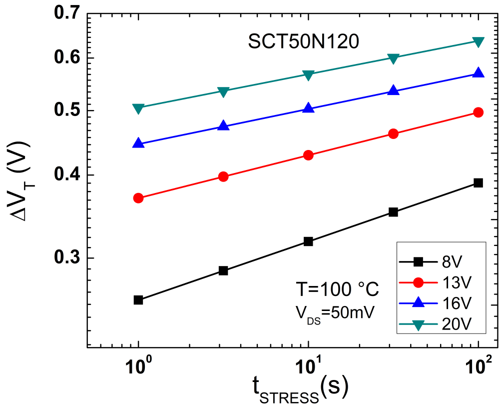


Figure 4.3: PBTI to ΔV_{th} in function of $time_{stress}$ with Temp=100°C

Table 4.2: PBTI to ΔV_{th} in function of $time_{stress}$ with Temp=100°C

$Time_{STRESS}[s]$	8V	12V	16V	20V
1	0.2594	0.3693	0.4453	0.5053
3.16228	0.2871	0.3977	0.4732	0.5353
10	0.3177	0.4284	0.5029	0.5672
31.62278	0.3517	0.4614	0.5345	0.6009
100	0.3892	0.4969	0.5681	0.6366

4.1.3 BTI to Different Stress Temperatures

The Figure 4.4 and Table 4.3 present the PBTI's results of the SiC Power MOSFET for different stress temperatures (20°C, 50°C, 100°C, 150°C) at constant stress voltage ($V_{GS} = 16[V]$) and with $V_{DS} = 50[mV]$ where we get an ascending behavior of ΔV_{th} in function of the logarithmic time.

The Figure 4.4 also present the increase of charging traps which means the rise of ΔV_{th} while decrease the stress temperature and in a long time too. It can be a way to do a de-trapping process using high temperature due to the kinetic energy of the electrons in the traps.

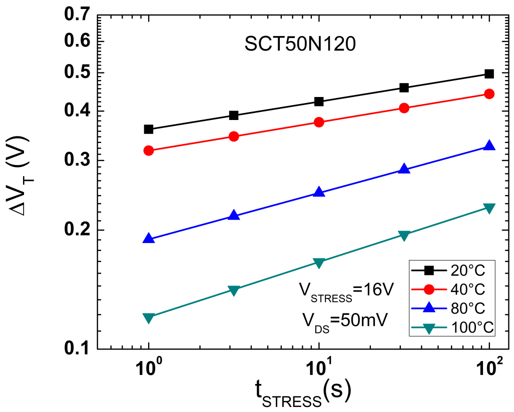


Figure 4.4: PBTI to ΔV_{th} in function of $time_{stress}$ with $V_{stress} = 16V$

Table 4.3: PBTI to ΔV_{th} in function of $time_{stress}$ with $V_{stress} = 16V$

$Time_{STRESS}[s]$	20°C	40°C	80°C	100°C
1	0.3596	0.3177	0.1895	0.1206
3.16228	0.3898	0.345	0.2169	0.1415
10	0.4225	0.3748	0.2483	0.1661
31.62278	0.458	0.4071	0.2842	0.1948
100	0.4965	0.4421	0.3254	0.2285

4.1.4 Charge Trapping Rate

The Figure 4.5 presents the results of charge trapping rate (called b) ($b = \frac{\partial Log \Delta V_{th}}{\partial log(t)}$) of the SiC Power MOSFET for different stress voltages (8[v], 13[v], 16[v] and 20[v]) at constant stress temperature (Temp=100°C) and with $V_{DS} = 50[mV]$ where we get a decrease behavior of charge trapping rate (b-) in function of the stress voltage.

This acquired data demonstrate the reduction of the charge trapping rate while the V_{stress} increase.

The Figure 4.6 presents the results of charge trapping rate (b) ($b = \frac{\partial Log \Delta V_{th}}{\partial log(t)}$) of

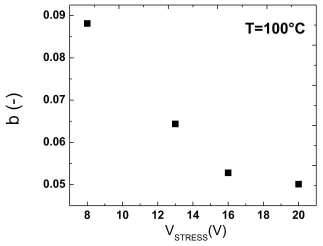


Figure 4.5: The charge trapping rate (named b) in function of voltage stress

the SiC Power MOSFET for different stress temperatures (20°C, 40°C, 80°C, 100°C) at constant stress voltage ($V_{GS} = 16[V]$) and with $V_{DS} = 50[mV]$ where we get an ascending behavior of charge trapping rate (b-) in function of the temperature.

This acquired data demonstrate the reduction of the charge trapping rate while the $Temperature_{stress}$ decrease.

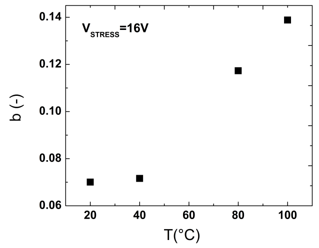


Figure 4.6: The charge trapping rate named b) in function of temperature

The Figure 4.7 presents the results of charge trapping rate (b) ($b = \frac{\partial Log \Delta V_{th}}{\partial log(t)}$) of the SiC Power MOSFET in function of ΔV_{th} at constant stress voltage ($V_{GS} = 8[V]$), constant stress temperature (Temp=100°C) and with $V_{DS} = 50[mV]$.

Here we get a decrease behavior of charge trapping rate (b-) with very small variation due to the logarithmic function and dependency of ΔV_{th} but it will be considered to continue with the physic study of this charging traps.

The Figure 4.8 and Table 4.4 present the results of variation of charge trapping rate for the SiC Power MOSFET in function of logarithmic stress time to different stress voltage (8[v], 12[v], 16[v] and 20[v]) at constant stress temperature (Temp=100°C) and with $V_{DS} = 50[mV]$ where we get a decrease behavior of $\Delta b(-)$ in function of the logarithmic

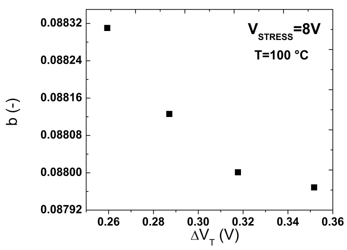


Figure 4.7: The charge trapping rate (named b) in shift voltage threshold

time.

This acquired give information about how fast change the charge trapping rate, in other words is the velocity of change which decrease while the time increase and the stress voltage decrease. Here we conclude that the charge trapping rate (b) started to remain constant after 31.6[s] for $Temp_{stress} = 100°C$.

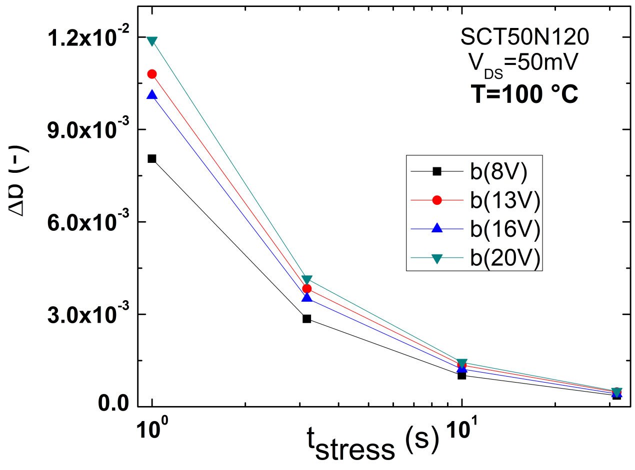


Figure 4.8: The variation of charge trapping rate (named b) in function of time

Table 4.4: charge trapping rate VS Time $Time_{STRESS}[s]$

$Time_{STRESS}[s]$	b(8V)	b(12V)	b(16V)	b(20V)
1	0.00805	0.0108	0.0101	0.0119
3.16228	0.00285	0.00383	0.00352	0.00415
10	0.00102	0.00135	0.00122	0.00144
31.62278	3.61E-4	4.77E-4	4.2E-4	5E-4

The Figure 4.9 and Table 4.5 present the results of variation of charge trapping rate for the SiC Power MOSFET in function of logarithmic stress time to different stress voltage

(8[v], 12[v], 16[v] and 20[v]) at constant stress temperature (Temp=100°C) and with $V_{DS} = 50[mV]$ where we get a decrease behavior of $\Delta b(-)$ in function of the logarithmic time. The difference with the last table and figure is the logarithmic $\Delta b(-)$ plotted instead of lineal $\Delta b(-)$. In other words there is a power law function who predominates this behavior.

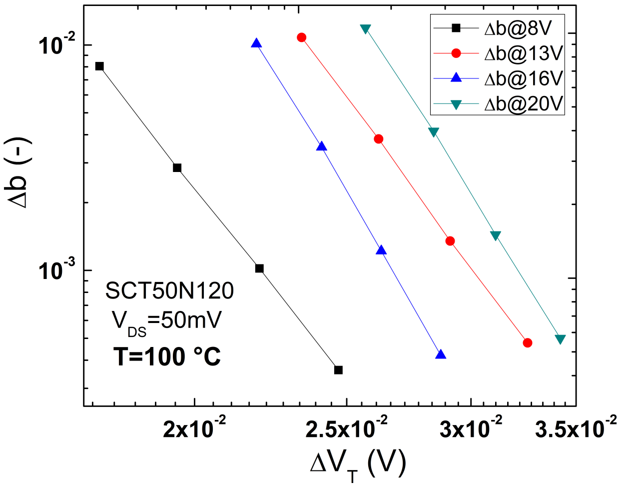


Figure 4.9: The variation of charge trapping rate (named b) in shift voltage threshold

Table 4.5: Charge trapping rate VS ShiftVth

$\Delta V_{th}(8V)[V]$	b(8V)	$\Delta V_{th}(12V)[V]$	b(12V)	$\Delta V_{th}(16V)[V]$	b(16V)	$\Delta V_{th}(20V)[V]$	b(20V)
0.0174	0.00805	0.0234	0.0108	0.0219	0.0101	0.0257	0.0119
0.0195	0.00285	0.0262	0.00383	0.0241	0.00352	0.0284	0.00415
0.022	0.00102	0.0291	0.00135	0.0263	0.00122	0.0311	0.00144
0.0247	3.61E-4	0.0326	4.77E-4	0.0287	4.2E-4	0.0342	5E-4

The Figure 4.10 and Table 4.6 present the results of logarithmic charge trapping rate (b-) for the first SiC Power MOSFET (SCT50N120) in function of logarithmic ΔV_{th} at constant stress time ($time_{stress} = 1[s]$) and with $V_{DS} = 50[mV]$ where we get a decrease behavior of logarithmic b(-).

This information give us a universal decreasing behavior of the charging rate in function of the number of filled traps independent of stress conditions. Then, the probability of charging traps is associated with the number of available empty traps for the first SiC Power MOSFET (SCT50N120).

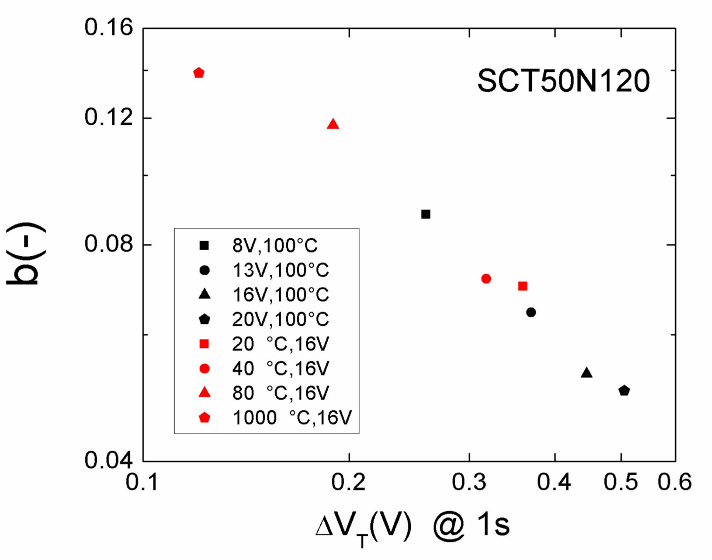


Figure 4.10: The $\Delta V_{th} RATE$ VS $\Delta V_{Recovery}$ for SCT50N120

Table 4.6: $\Delta V_{th} RATE$ VS $\Delta V_{Recovery}$ for SCT50N120

b(-)	$\Delta V_{th} to 1[s]$
0.2594	0.0881
0.3693	0.06444
0.4453	0.05289
0.5053	0.05016
0.3596	0.07005
0.3177	0.07175
0.1895	0.1174
0.1206	0.13877

4.1.5 Universal Decreasing Behavior

The Figure 4.11 present the results of logarithmic charge trapping rate (b-) for the second SiC Power MOSFET (SCT30N120) in function of logarithmic ΔV_{th} at constant stress time ($time_{stress} = 1[s]$) and with $V_{DS} = 50[mV]$ where we get a decrease behavior of logarithmic b(-).

This information give us a universal decreasing behavior of the charging rate in function of the number of filled traps independent of stress conditions. Then, the probability of charging traps is associated with the number of available empty traps for the first SiC Power MOSFET (SCT50N120).

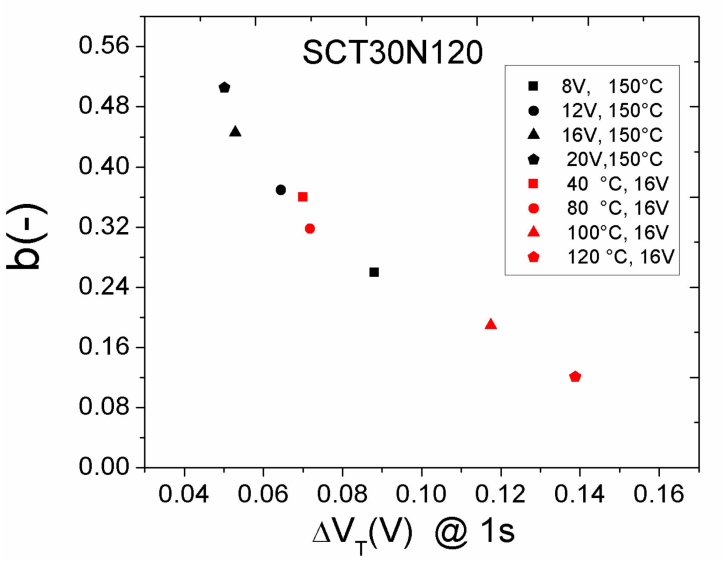


Figure 4.11: The $\Delta V_{th} RATE$ VS $\Delta V_{Recovery}$ for SCT30N120

4.2 Zafar's Fitting

Measurements of Zafar's model are made on long channel nFETs with channel length ¿1 μm and channel width ranging between 20 and 50 μm. [10].

The acquired data of charge trapping are showed as a function of temperature and stress voltage on SiC MOSFET with silicon carbide gates. Where we observe that ΔV_{th} increases with stressing time at a constant stress voltage. Even similar shapes in ΔV_{th} curves at various stress voltages are observed but while increasing stress voltage the curves increase too.

In the graphic (Figure 4.12,Figure 4.13,Figure 4.14,Figure 4.15) we can note that all ΔV_{th} curves for SiC exhibit a marked characteristic. At the beginning the stages of stressing, ΔV_{th} is observed to increase with a power law dependence on stress time.

Observing the shift in threshold voltage it concludes that ΔV_{th} is due to trapping of charges in the existing traps without generation of extra traps because the ΔV_{th} start to stop.

Zafar's model predict ΔV_{th} shifts in function of injected charge density and stressing time and the gaining perception into the trapping physics, a model for charge trapping is developed for high k gate dielectric stacks. Owing to the trapping of electrons in existing traps, the entire trap density is considered in the gate dielectric stack keeping constant with stressing and that the stress induced ΔV_{th} shifts.

Using the model (Equation 4.1), ΔV_{th} is calculated as a function of stress time.

$$\Delta V_{th} = \Delta V_{MAX} * [1 - exp^{-(\frac{t}{\tau_0})^{\gamma}}] \tag{4.1}$$

4.2.1 PBTI to 20 °C for Longer Time

The Figure 4.12 and Table 4.7 present the PBTI's (for longer time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress voltage (8[v], 12[v], 16[v] and 20[v]) at constant stress temperature ($Temeperature_{stress} = 20°C$) and with $V_{DS} = 50[mV]$.

Here we get a ΔV_{th} saturation behavior for time over 1000 seconds, then we see the

the saturation of the charging traps due to ΔV_{th} started to stop.

The Zafar' model tell us that trapping of charges in the existing traps without generation of extra traps start to stop in a longer time therefor is possible use this model the give a fitting and predict the ΔV_{th} behavior for longer times in the SiC Power MOSFET device SCT50N120 to $Temeperature_{stress} = 20°C$.

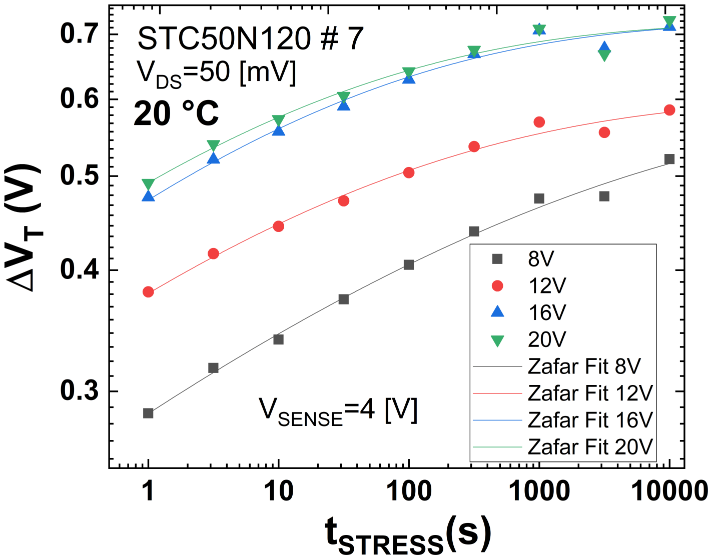


Figure 4.12: The Zafar's fitting for 20°C

Table 4.7: Zafar's fitting for 20°C

Model	Zafar 20°C			
Equation	$\Delta V_{MAX} * [1 - exp^{-(t/\tau)^{\gamma}}]$			
Plot	8[v]	12[v]	16[v]	20[v]
ΔV_{MAX}[mV]	0.59451 ± 0.05014	0.60098 ± 0.01941	0.72097 ± 0.0199	0.72005 ± 0.02361
τ[s]	33.07386 ± 41.92713	1.0481 ± 0.39083	0.6527 ± 0.21857	0.37768 ± 0.17002
γ	0.12252 ± 0.01561	0.13521 ± 0.01742	0.1475 ± 0.02148	0.14387 ± 0.02836

4.2.2 PBTI to 50 °C for Longer Time

The Figure 4.13 and Table 4.8 present the PBTI's (for longer time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress voltage (8[v], 12[v], 16[v] and 20[v]) at constant stress temperature ($Temeperature_{stress} = 50°C$) and with $V_{DS} = 50[mV]$.

Here we get a ΔV_{th} saturation behavior for time over 1000 seconds, then we see the the saturation of the charging traps due to ΔV_{th} started to stop.

The Zafar' model tell us that trapping of charges in the existing traps without generation of extra traps start to stop in a longer time therefor is possible use this model the give a fitting and predict the ΔV_{th} behavior for longer times in the SiC Power MOSFET device SCT50N120 to $Temeperature_{stress} = 50°C$.

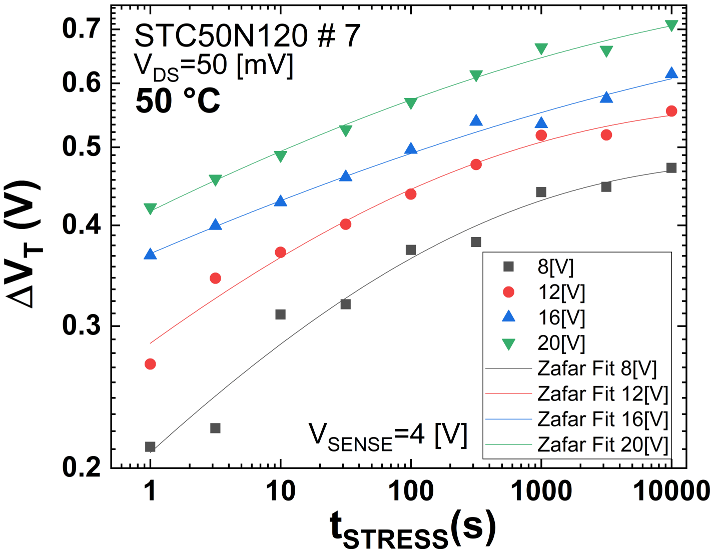


Figure 4.13: The Zafar's fitting for 50°C

Table 4.8: Zafar's fitting for 50°C

Model	Zafar 50°C			
Equation	$\Delta V_{MAX} * [1 - exp^{-(t/\tau)^{\gamma}}]$			
Plot	8[v]	12[v]	16[v]	20[v]
ΔV_{MAX}[mV]	0.48292 ± 0.0276	0.56959 ± 0.0255	0.74219 ± 0.12102	0.80245 ± 0.07076
τ[s]	17.9391 ± 10.98189	8.67231 ± 4.46697	44.08095 ± 130.69354	14.66907 ± 20.10698
γ	0.19628 ± 0.02965	0.16756 ± 0.02108	0.09895 ± 0.02087	0.11605 ± 0.01784

4.2.3 PBTI to 100 °C for Longer Time

The Figure 4.14 and Table 4.9 present the PBTI's (for longer time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress voltage (8[v], 12[v], 16[v] and 20[v]) at constant stress temperature ($Temep_{stress} = 100°C$) and with $V_{DS} = 50[mV]$.

Here we get a ΔV_{th} saturation behavior for time over 1000 seconds, then we see the the saturation of the charging traps due to ΔV_{th} started to stop.

The Zafar' model tell us that trapping of charges in the existing traps without generation of extra traps start to stop in a longer time therefor is possible use this model the give a fitting and predict the ΔV_{th} behavior for longer times in the SiC Power MOSFET device SCT50N120 to $Temeperature_{stress} = 100°C$.

Table 4.9: Zafar's fitting for 100°C

Model	Zafar 100°C			
Equation	$\Delta V_{MAX} * [1 - exp^{-(t/\tau)^{\gamma}}]$			
Plot	8[v]	12[v]	16[v]	20[v]
ΔV_{MAX}[mV]	0.39751 ± 0.0155	0.50894 ± 0.02034	0.4829 ± 0.03136	0.53078 ± 0.02717
τ[s]	4.94259 ± 2.38592	1.52459 ± 0.71788	2.84436 ± 2.11185	1.80959 ± 1.06459
γ	0.14376 ± 0.0156	0.13633 ± 0.01976	0.15526 ± 0.03633	0.14605 ± 0.02841

4.2.4 PBTI to 150 °C for Longer Time

The Figure 4.15 and Table 4.10 present the PBTI's (for longer time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress voltage (8[v], 12[v], 16[v] and 20[v]) at constant stress temperature ($Temeperature_{stress} =$

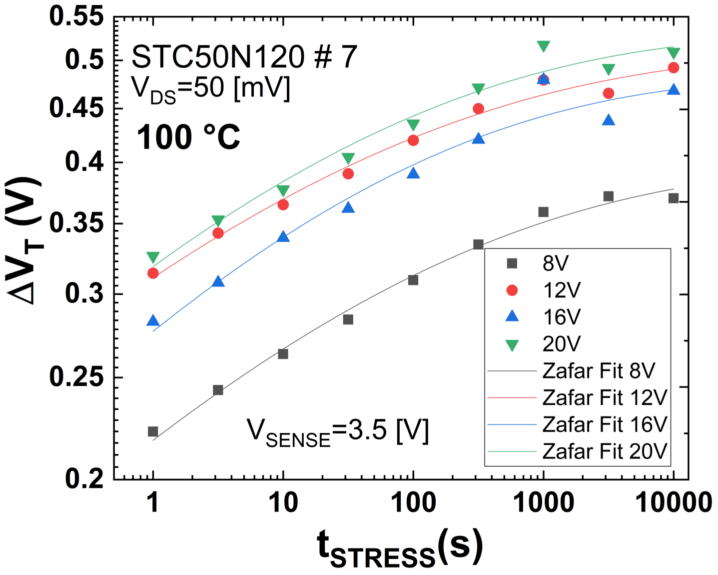


Figure 4.14: The Zafar's fitting for 100°C

$150^{\circ}C$) and with $V_{DS} = 50[mV]$.

Here we get a ΔV_{th} saturation behavior for time over 1000 seconds, then we see the the saturation of the charging traps due to ΔV_{th} started to stop.

The Zafar' model tell us that trapping of charges in the existing traps without generation of extra traps start to stop in a longer time therefor is possible use this model the give a fitting and predict the ΔV_{th} behavior for longer times in the SiC Power MOSFET device SCT50N120 to $Temeperature_{stress} = 150^{\circ}C$.

Table 4.10: Zafar's fitting for 150°C

Model	Zafar 150°C			
Equation	$\Delta V_{MAX} * [1 - exp^{-(t/\tau)^{\gamma}}]$			
Plot	8[v]	12[v]	16[v]	20[v]
ΔV_{MAX}[mV]	0.23 ± 0.00888	0.32034 ± 0.01575	0.3696 ± 0.0154	0.48562 ± 0.14343
τ[s]	6.62378 ± 2.75287	1.1857 ± 0.8841	1.8644 ± 0.90079	25.10472 ± 102.89325
γ	0.19645 ± 0.02791	0.26763 ± 0.11807	0.18065 ± 0.03815	0.13432 ± 0.06772

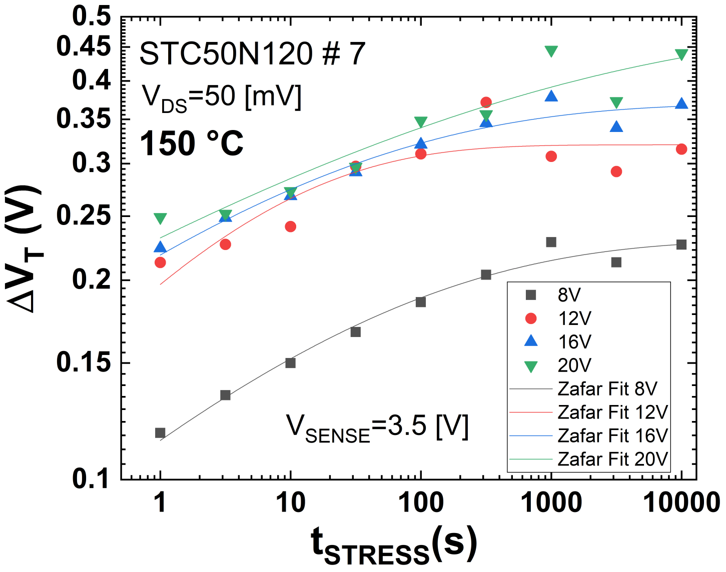


Figure 4.15: The Zafar's fitting for 150°C

4.2.5 Zafar's Variables

Varible ΔV_{max}

ΔV_{max} is related to the total trap density as shown

$$\Delta V_{th} = \Delta V_{MAX} * [1 - exp(-(N_{inj} * \sigma_0)^{\beta}] \tag{4.2}$$

Which predicts the dependence of threshold voltage shifts on injected charge carrier density (N_{inj}). This equation can also be expressed as a function of total stress time [10]. Later consider β which is a depended constant of the gate stack.

The curves behavior in Figure 4.16 confirm with more security and in direct form the lower injected charge carrier density to higher temperatures and lower stress voltage watched previously.

The curves behavior in Figure 4.17 also confirm with more security and in direct form the higher injected charge carrier density to higher stress voltage and lower temperatures

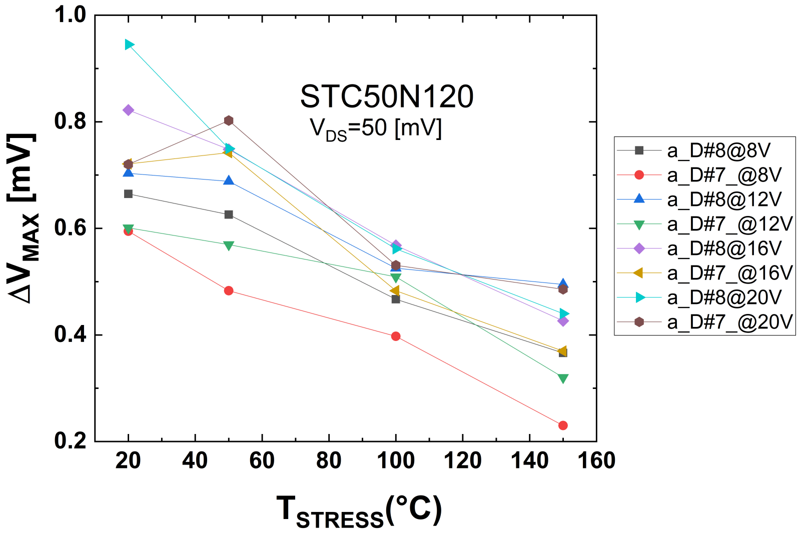


Figure 4.16: The Zafar's variable ΔV_{max} in function of $Temperature_{stress}$

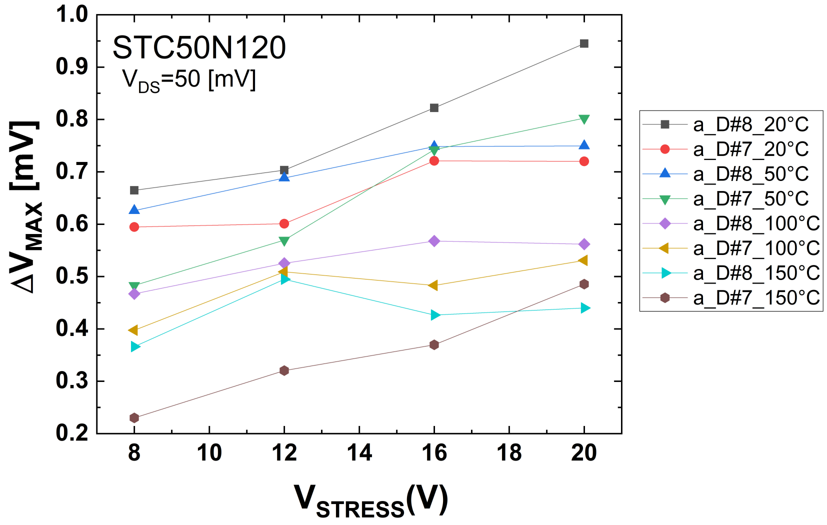


Figure 4.17: The Zafar's variable ΔV_{max} in function of $Voltage_{stress}$

watched previously.

Varible γ

$$\gamma = (1 - \alpha) * \beta \tag{4.3}$$

Where $\beta \approx 0.32$ according to Zafar's model for all its curve. Then β not is necessary the same value for us because the studied devices have different gate stack structure and material.

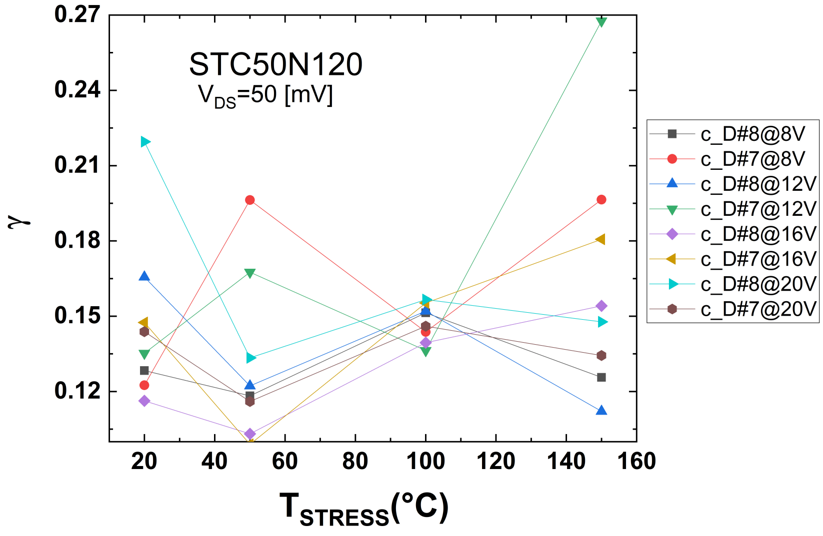


Figure 4.18: The Zafar's variable γ in function of $Temperature_{stress}$

The curves behavior in Figure 4.18 is difficult to read because it depends to the gate stack structure and SiC material, but if we contrast the figures of PBTI for longer time (Figure 4.12, Figure 4.13, Figure 4.15 and specially Figure 4.14) the best acquired data is in the Figure 4.14 then fortunately we should give a range for this Zafar's model constant γ between 0.13633 and 0.15662 for $Tem_{stress} = 100°C$ having to be confirmed for the other temperatures with an improved data acquisition.

In the Figure 4.19 we considered the curve for $Tem_{stress} = 100°C$ getting the same conclusion because this curve try to be constant in the range of γ between 0.13633 and 0.15662. And having to be confirmed for the other voltages with an improved data acquisition.

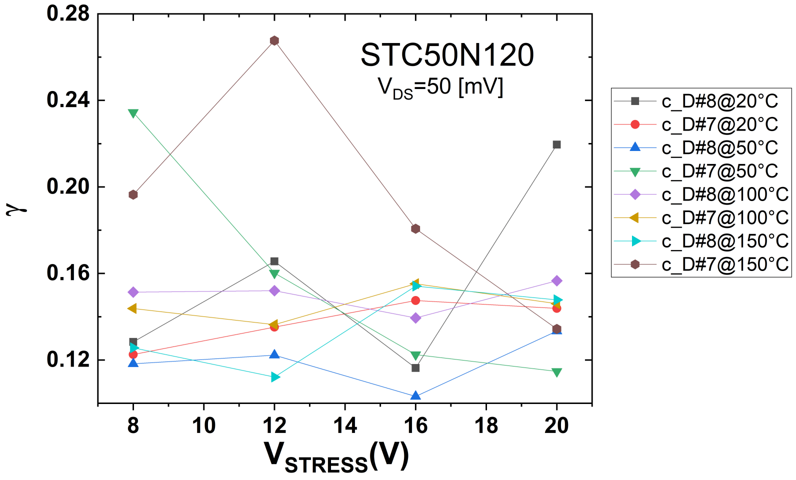


Figure 4.19: The Zafar's variable γ in function of $Voltage_{stress}$

Varible τ_0

$$\tau_0 = exp^{(1-\alpha)^{-1}*Ln[e*\frac{(1-\alpha)}{j_0*\sigma_0}]} \tag{4.4}$$

According to Sufi Zafar and his research team:

σ_0 is estimated from the calculated results for ΔV_{th} vs N_{inj} curves. j_0 and α are two constant determined from gate leakage current density (J_g) versus time measurements.

The curves behavior in Figure 4.20 is difficult to read because it depends to the leakage current density variation (J_g), then we aren't available to get information about this information.

The curves behavior in Figure 4.21 is difficult to read due to his dependency to the leakage current density variation (J_g), then we aren't available to get assured information about this behavior. But we dare to see a behavior or a convergence under $\tau_0 = 5$ which need to be study in the future with more samples with an improved data acquisition.

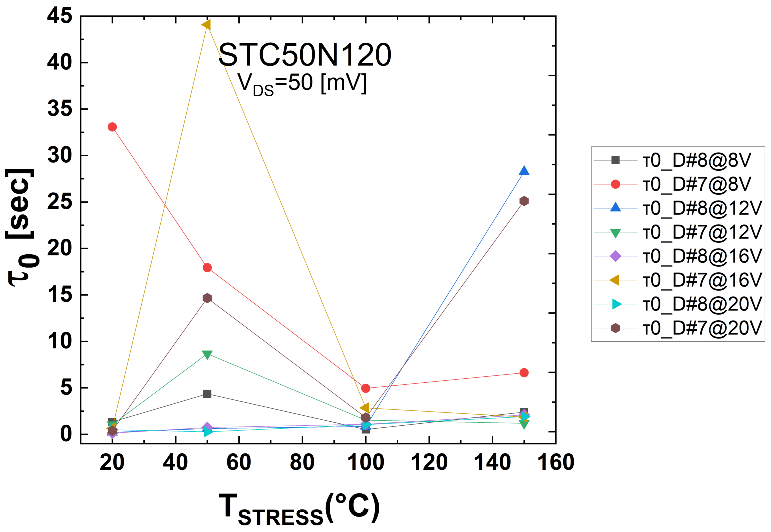


Figure 4.20: The Zafar's variable τ_0 in function of $Temperature_{stress}$

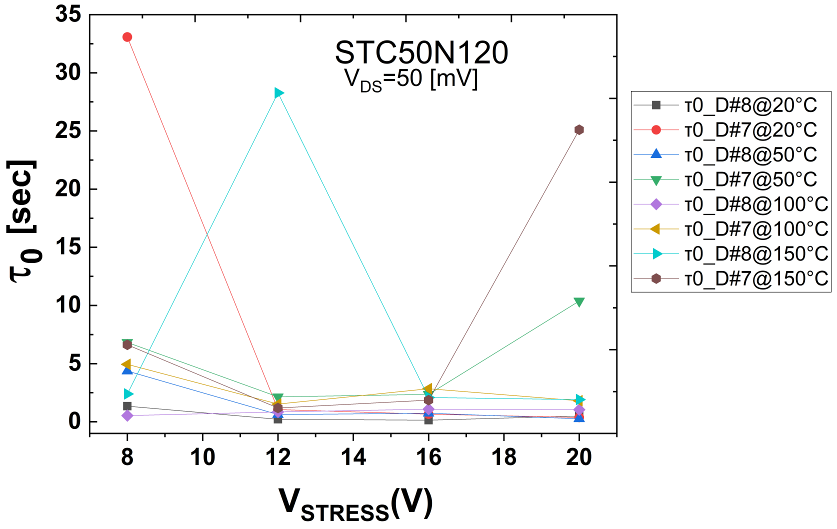


Figure 4.21: The Zafar's variable τ_0 in function of $Voltage_{stress}$

4.3 Recovery's Results

4.3.1 Acquired Data with Different $\frac{Saample}{Decade}$

The Figure 4.22 and Table 4.11 present the recovery's (for short time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different $\frac{Saample}{Decade}$ (5 and 2[) at constant stress temperature ($Temeperature_{stress} = 20°C$) and with $V_{DS} = 50[mV]$.

This acquired data was doing with the target to select the best way to measure the recovery voltage because the $V_{sense} = 3[v]$ produce new trapping charge induced in direct form with the recovery. Then as we can see the best form to measure is with $2\frac{Saample}{Decade}$.

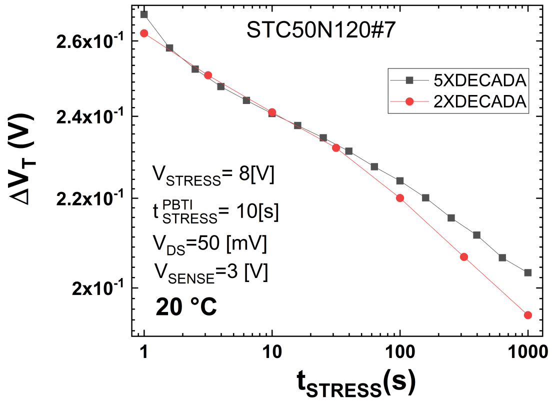


Figure 4.22: Measure variation by $\frac{Saample}{Decade}$

Table 4.11: Measure variation by $\frac{Saample}{Decade}$

$Time_{STRESS}[s]$	$5\frac{Sample}{Decade}$	$Time_{STRESS}[s]$	$2\frac{Sample}{Decade}$
0	0.29328	0	0.28839
1	0.26738	1	0.26209
1.58	0.25802	3.16228	0.25067
2.51	0.25231	10	0.24101
3.98	0.24766	31.62278	0.23207
6.31	0.24406	100	0.22003
10	0.24069	316.22777	0.2067
15.85	0.23763	1000	0.19431
25.12	0.23456		
39.81	0.23124		
63.1	0.22747		
100	0.22408		
158.49	0.22008		
251.19	0.21542		
398.11	0.21154		
630.96	0.20651		
1000	0.20324		

4.3.2 Acquired Data with Different $V_{RECOVERY}$

The Figure 4.23 and Table 4.12 present the recovery's (for short time) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different recovery voltage (0[v] and -2[v]) at constant stress temperature ($Temeperature_{stress} = 20°C$), with $V_{DS} = 50[mV]$ and $V_{sense} = 3[v]$.

The recovery's results show us that the negative stress voltage produce a recovery more fast than a recovery with 0[v] it's due to the negative electric field that repels the charge trapping of the gate stack.

4.3.3 Recovery for Different Stress Temperature

The Figure 4.24 and Table 4.13 present the recovery's (ΔV_{th}) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress temperature (20 °C, 80 °C, 100 °C and 150 °C) at $V_{recovery} = -2[V]$, constant stress

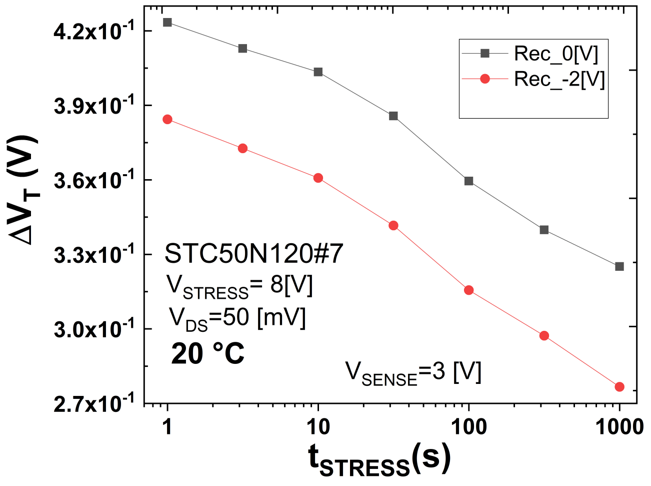


Figure 4.23: Measure variation by $V_{RECOVERY}[s]$

Table 4.12: Measure variation by $V_{RECOVERY}[s]$

$Time_{STRESS}[s]$	Rec 0[v]	Rec -2[v]
1	0.18254	0.14804
3.16228	0.17077	0.13205
10	0.16081	0.11884
31.62278	0.14881	0.10395
100	0.13607	0.08829
316.22777	0.12306	0.07349
1000	0.10847	0.05912
3162.28	0.10006	0.05547
10000	0.09247	0.0425

voltage ($V_{stress} = 12[V]$), with $time_{stress} = 1000[s]$, $V_{DS} = 50[mV]$, and $V_{sense} = 3[v]$.

This Figure 4.24 determine an immediately de-trapping process at the beginning, it indicates a natural de-trapping of the material which is minimum in 150°C due to the extra de-trapping by the temperature thus started to avoid V_{th} variation.

4.3.4 Recovery for Different Stress Voltage to $Temp_{stress} = 20°C$

The Figure 4.25 and Table 4.14 present the recovery's (ΔV_{th}) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress voltage (8[v, 12[v], 16[v] and 20[v]]) at $V_{recovery} = 0[V]$, constant stress temperature

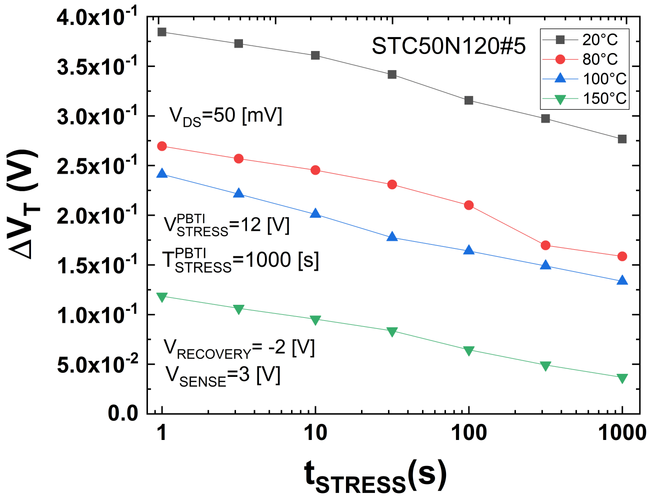


Figure 4.24: The Recovery in function of $Time_{stress}$ to different $Temp_{stress}$ and $V_{stress} = 12[v]$

Table 4.13: Recovery in function of $Time_{stress}$ to $Tempe_{stress}$ and $V_{STRESS} = 12[v]$

$Time_{STRESS}[s]$	20°C	50°C	100°C	150°C
1	0.38436	0.26952	0.2412	0.11847
3.16228	0.37268	0.25692	0.22123	0.10632
10	0.36078	039788	0.20086	0.09547
31.62278	0.34164	0.23085	0.17746	0.08361
100	0.31558	0.21011	0.16397	0.0645
316.23	0.29725	0.16969	0.1489	0.04924
1000	0.27663	0.15856	0.1336	0.03675

$(Temp_{stress} = 20 \circ C)$, with $time_{stress} = 1000[s]$, $V_{DS} = 50[mV]$, and $V_{sense} = 3[v]$.

The Figure 4.25 determine an immediately de-trapping process at the beginning in the first second which confirm the natural de-trapping of the material which is minimum in 1000[s], then ΔV_{th} tends to zero, thus indicating that in our experimental conditions no permanent damage was introduced during the stress phase.

4.3.5 Recovery for Different Stress Voltage to $Temp_{stress} = 150°C$

The Figure 4.26 and Table 4.15 present the recovery's (ΔV_{th}) results for the first SiC Power MOSFET (SCT50N120) in function of logarithmic $time_{stress}$ to different stress

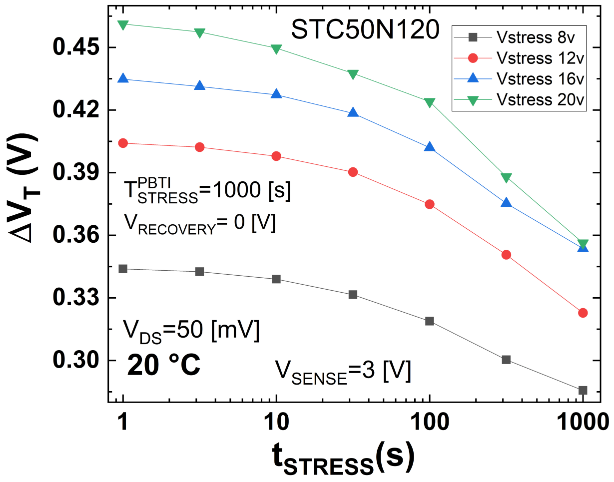


Figure 4.25: Recovery in function of $Time_{stress}$ to different V_{stress} and $Tempereture_{stress} = 20°C$

Table 4.14: Recovery in function of $Time_{stress}$ to different V_{stress} and $Tempereture_{stress} = 20°C$

$Time_{STRESS}[s]$	8[v]	12[v]	16[v]	20[v]
1	0.34389	0.40413	0.43477	0.46122
3.16228	0.40223	0.345	0.4313	0.4574
10	0.339	0.39788	0.42731	0.44968
31.62278	0.339	0.39788	0.41847	0.43756
100	0.3188	0.37483	0.40199	0.42402
316.23	0.30033	0.35063	0.37528	0.38801
1000	0.28566	0.32278	0.35364	0.35627

voltage (8[v, 12[v], 16[v] and 20[v]]) at $V_{recovery} = 0[V]$, constant stress temperature ($Temp_{stress} = 150 \circ C$), with $time_{stress} = 1000[s]$, $V_{DS} = 50[mV]$, and $V_{sense} = 3[v]$.

The Figure 4.26 determine an immediately de-trapping process at the beginning in the first second which confirm the natural de-trapping of the material which is minimum in 1000[s], then ΔV_{th} tends to zero, thus indicating that in our experimental conditions no permanent damage was introduced during the stress phase. And take account the same behavior to 20°C we consider as a general performance to all temperatures.

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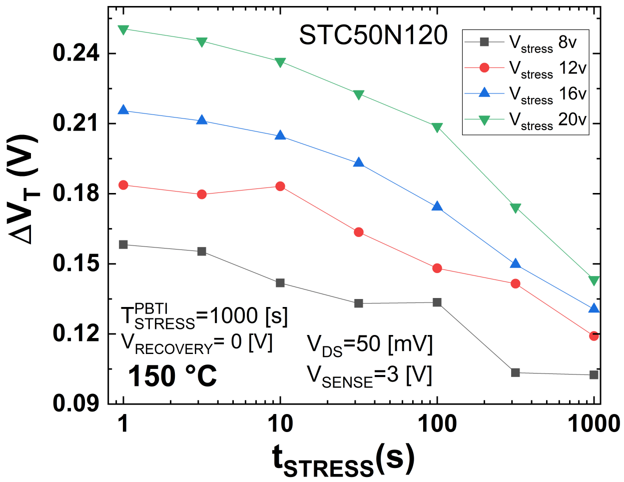

Figure 4.26: The Recovery's results in function of V_{STRESS} to 150°C

Table 4.15: Recovery's results in function of V_{STRESS} to 150°C

$Time_{STRESS}[s]$	8[v]	12[v]	16[v]	20[v]
1	0.15819	0.18371	0.21553	0.25057
3.16228	0.15528	0.17973	0.21119	0.24532
10	0.14182	0.18318	0.20462	0.2366
31.62278	0.13306	0.16357	0.19302	0.22274
100	0.13349	0.14811	0.17428	0.20878
316.23	0.10343	0.14151	0.14972	0.17426
1000	0.10245	0.11912	0.13062	0.14326

Chapter 5

Conclusion

With PBTI method used in the SiC power MOSFET we can concluded according to Figure 4.1 and Figure 4.2 that exist the threshold voltage shift towards the left (decrease) when the temperature increase then it means that the features of ON are better at high temperature as its ON-resistance.

In the PBTI shows in the Figure 4.3 concludes that while the V_{stress} increase the ΔV_{th} increase too, then the variation of V_{th} respect to the room temperature is higher at high voltage stress. Also the slop time tell us that the variation is according to a power law of ΔV_{th} in function of $Time_{stress}$ which depends of the V_{stress}.

With the behavior presented by PBTI in the Table 4.2 allow us to conclude that while $Temperature_{stress}$ increase the ΔV_{th} decrease, then the variation of V_{th} respect to the room temperature is higher at high temperature. Also the slop tell us that the variation is according to the power law of ΔV_{th} in function of $Time_{stress}$ which depends of the $Temperature_{stress}$. It can be a way to do a de-trapping process using high temperature due to the kinetic energy of the electrons in the traps.

The performance of the charge trapping rate (called b) ($b = \frac{\partial Log \Delta V_{th}}{\partial log(t)}$) in the Figure 4.5 give us a conclusion which demonstrate the reduction of the charge trapping rate while the V_{stress} increase.

The next performance in the Figure 4.6 of the charge trapping rate (called b) give us a conclusion which demonstrate the increment of the charge trapping rate while the T_{stress} increase.

Continuing with charge trapping rate in the Figure 4.7 we can conclude that exist reduction with very small variation due to the logarithmic function and dependency of ΔV_{th} but it will be considered to continue with the physic study of this charging traps.

In the Figure 4.8 there is the variation of charge trapping rate in function of stress time concluding how fast change the charge trapping rate, in other words is the velocity of change which decrease while the time increase and the stress voltage decrease. Here we conclude that the charge trapping rate (b) started to remain constant after 31.6[s] for $Temp_{stress} = 100°C$.

To finalize with charge trapping rate the Figure 4.9 presented the variation of charge trapping rate in function of threshold voltage shift for different stress voltage where can conclude that exist increasing of ΔV_{th} while the stress voltage increase and ΔV_{th} started to decrease with the logarithm of the charge trapping rate (b). In other words there is a power law function who predominates this behavior.

To summarize everything the Figure 4.10 and Figure 4.11 for both studied devices we concluded with a universal decreasing behavior of the charging rate in function of the number of filled traps independent of stress conditions. Then, the probability of charging traps is associated with the number of available empty traps.

With acquired data for time over 1000 seconds we can appreciate the saturation of the charging traps due to ΔV_{th} started to stop then in conclusion trapping of charges in the existing traps without generation of extra traps start to stop it means that we can use the Zafar' model to generate the respective fitting. This Zafar' model behavior is appreciated in Figure 4.12, Figure 4.13, Figure 4.14 and Figure 4.15.

Taking a count the Figure 4.16 and Figure 4.17 which presented the ΔV_{max} behavior we confirm with more security and in direct form the lower injected charge carrier density to higher temperatures and lower stress voltage watched previously.

Considering the Figure 4.18 with Figure 4.19 and take a count the best acquired data between Figure 4.12, Figure 4.13, Figure 4.15 and specially Figure 4.14 then fortunately we should give a range for this Zafar's model constant γ between 0.13633 and 0.15662 for $Tem_{stress} = 100°C$ having to be confirmed for the other temperatures with an improved data acquisition.

The curves of Figure 4.21 aren't available to get confirmed information about this behavior. But we dare to see a behavior or a convergence under $\tau_0 = 5$ which need to be study in the future with more samples with an improved data acquisition.

The recovery's results in Figure 4.23 conclude that the negative stress voltage produce a recovery more fast than a recovery with 0[v].

The first second of Figure 4.24 allow us determine an immediately de-trapping process at the beginning it indicates a natural de-trapping of the material which is minimum in 150°C due to the extra de-trapping by the temperature thus started to avoid V_{th} variation.

The Figure 4.24 and Figure 4.24 determine an immediately de-trapping process at the beginning in the first second which confirm the natural de-trapping of the material which is minimum in 1000[s], then ΔV_{th} tends to zero, thus indicating that in our experimental conditions no permanent damage was introduced during the stress phase.

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