UNIVERSIDAD SAN FRANCISCO DE QUITO

Colegio de Posgrados

Firmware Update of the CTP7 Card to Achieve a 5 Gbps Optical Communication for the HCAL Calorimeter at CMS Project

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HOJA DE APROBACIÓN DE TRABAJO DE TITULACION

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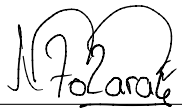
Firma del estudiante:	
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DEDICATORIA

A mis padres.

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Pero sobre todo, quisiera agradecer a mis padres por darme siempre palabras de motivación que resultaron fundamentales para que yo no desista de perseguir mis objetivos.

RESUMEN

Un ejemplo de decodificador es presentado en este artÍculo como complemento del firmware para la tarjeta CTP7 usada para el procesamiento de datos en el calorimetro HCAL en el experimento CMS CERN El decodificador propuesto fue diseñado para recolectar datos desde el parte receptora de la tarjeta y seleccionarlos de acuerdo a las especificaciones manejadas en los documentos del subdetector HB, dentro del HCAL. Se realizó una simulación en el software Vivado para tener un preámbulo de su desempeño. Un tentativo de incluir el decoder en el firmware para probarlo en tiempo real, mostró que existen varios errores en las consideraciones de clocking.

ABSTRACT

Key words: CERN, CMS, FPGA, VHDL, HCAL, programming, SoC, AXI, Vivado, Xilinx

An example of decoder is presented on this article, to complement the CTP7 card firmware used for processing data at the calorimeter HCAL for CMS CERN experiment. The decoder proposed was designed to collect the data from the receiver side of the card and select it according to the specifications document managed by the HB subdetector inside HCAL. A simulation was performed on Vivado software to show a preview of it's perform. A tentative of including the design on the firmware to test on real time processing, showed that the design presents some errors of clocking considerations.

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Chapter 1

INTRODUCTION

In order to fulfil the requirements of high speed in data acquisition and data processing, engineers, physicists and technicians at CERN CMS experiment, design plans for migration of technology, to have electronic devices more efficient and more resistant to radiation which is constantly increasing to get more valid data for physicists. These migrations are known as the Phase 1 and Phase 2. To achieve this objective, it is necessary to enhance the electronics and firmware inside the detectors and calorimeters including the components that involve the optical communication for an optimal data transmission, from its collection until its reception in the μTCA infrastructure at the back-end system where the data is analysed and stored.

CMS is the first project at CERN, to use a card specifically designed for such high speed communication between front-end and back-end systems, which includes a Virtex-7 FPGA for processing and a ZYNQ SoC for TCP/IP connection and ancillary control tasks. This card is known as CTP7.

The new CTP7 card has intention to replace the current card used for Phase 1 which contains two Virtex-6 fpgas. The replacement of one FPGA by a ZYNQ Soc Linux based will simplify the control and general use of the card.

The Wisconsin Firmware team, in charge of designing and building the card, developed a demo for the new CTP7, that allows to increase the optical speed from 4.8 Gbps (current speed) to 5Gbps, for a better and more efficient data processing, using Intellectual Property (IP) Xilinx resources and AXI standardize architecture.

This demo will be tested in laboratory as a first step and for the purpose of this thesis.

Chapter 2

CERN'S STRUCTURE

CERN is the European Organization for Nuclear Research and it's the biggest laboratory dedicated to the study of particle physics. It was created in 1954 and is located in Geneva, close to the Franco-Swiss border. CERN is well know for the resent discovery of the Higgs boson which justifies the theory developed 1964.

This laboratory has the biggest particle collider (Large Hadron Collider or LHC) that allows to test different predictions about the existence of new fundamental particles and other theories about particle physics.

Figure 2.1: Large Hadron Collider[1]

CERN has purposed-build instruments for particle acceleration and detection. Most of these accelerators and detectors are built in CERN premises or in its partner lab in United States, Fermilab.

The accelerators are in charge to boost the beams of particles to increase their energy

before the collision and the detectors observe the results after this collision. The LHC is one of the 9 accelerators installed at CERN, including the famous Proton Synchrotron.

The LHC consist of a 27 kilometre ring of superconducting magnets and superconducting electromagnets to boost the energy of the particles of two beams that travel in different directions inside the collider. There are thousands of magnets dedicated to direct the beam around the accelerator. Other type of magnets have the function of increase the chance of collision by "sqeezing" the particles closer together.

The beam inside the LHC, collide in four locations, corresponding to the location of each one of the particle detectors: ATLAS, CMS, ALICE and LHCb.

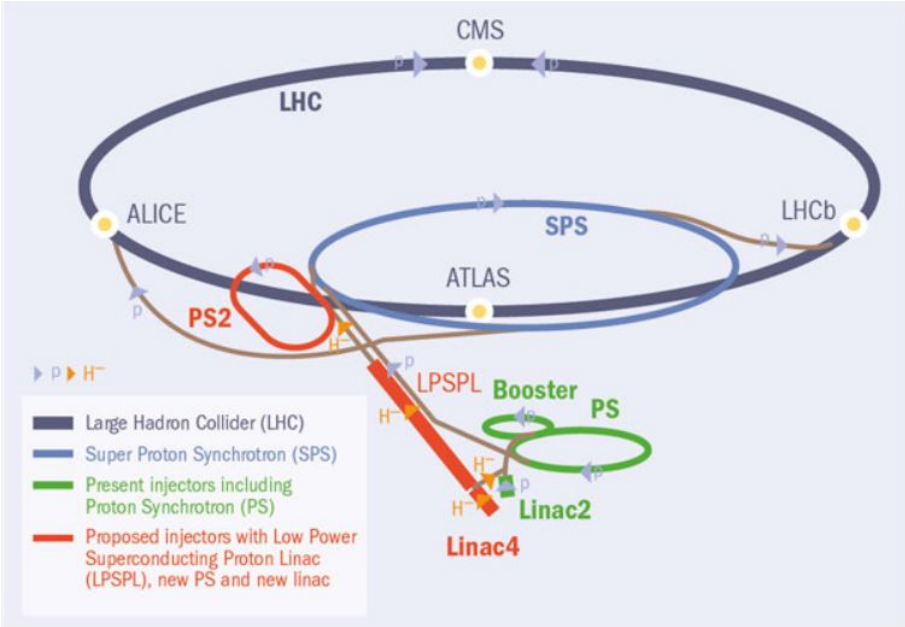

Figure 2.2: CERN complex[1]

2.1 CMS and HCAL architecture

The Compact Muon Solenoid or CMS, is one of the four particle detectors along the Large Hadron Collider or LHC. This detector is part of the program that looks for extra dimensions and particles that could make up dark matter.

The CMS experiment is one of the largest scientific collaborations, involving 4300 physicists, engineers, technicians, students and support staff from 182 institutions in 42 countries, being the San Francisco de Quito university in Ecuador, one of them.

The CMS was built around a big solenoid magnet and takes the form of a cylindrical coil of superconducting cable, generating 4 tesla (about 100000 times the magnetic field of the Earth). CMS was build in 15 sections and were put in place in an underground cavern near Cessy in France and then reassembled. The detector is 21 meters long, 15 meters wide and 15 meters high.

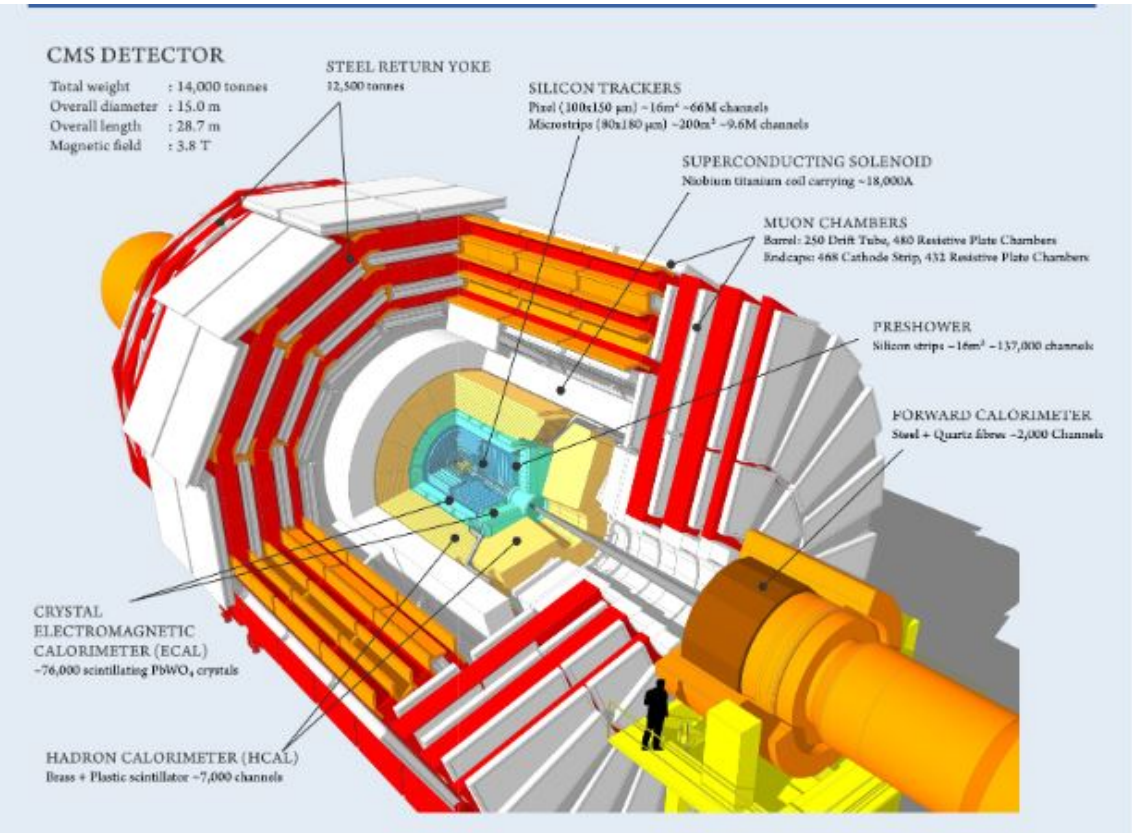

Figure 2.3: CMS Detector Design[1]

The CMS magnet has the job of bending the paths of particles coming from the collision in the LHC. When a particle is less curved, by the magnetic field, means that it has more momentum. Tracing the path, allows to measure the momentum.

This magnet is a solenoid, which means that is made of coils of wire that produce a uniform magnetic field when electricity flows through them. The magnet is superconducting and allows to reduce the resistance of electricity through it, which creates a powerful magnetic field.

The tracker of the CMS, records the paths taken by the particles. The lecture is based on a multi position reading of the same particle in some key points.

To not confuse particle from two different events, the detectors must have very good resolution and the signals from the million of electronic channels must be synchronised to be identified as being from the same event.

To measure the energy, CMS has two calorimeters: the ECAL and HCAL.

The measurement of the energy of the particles produced in each collision, helps to understand the characteristics of every event.

The Electromagnetic Calorimeter or ECAL, measures the energy of electrons and photons by stopping them completely. The Hadron Calorimeter or HCAL, measures the hadrons that are composite particles made up of quarks and gluons and can not be detected by the ECAL.

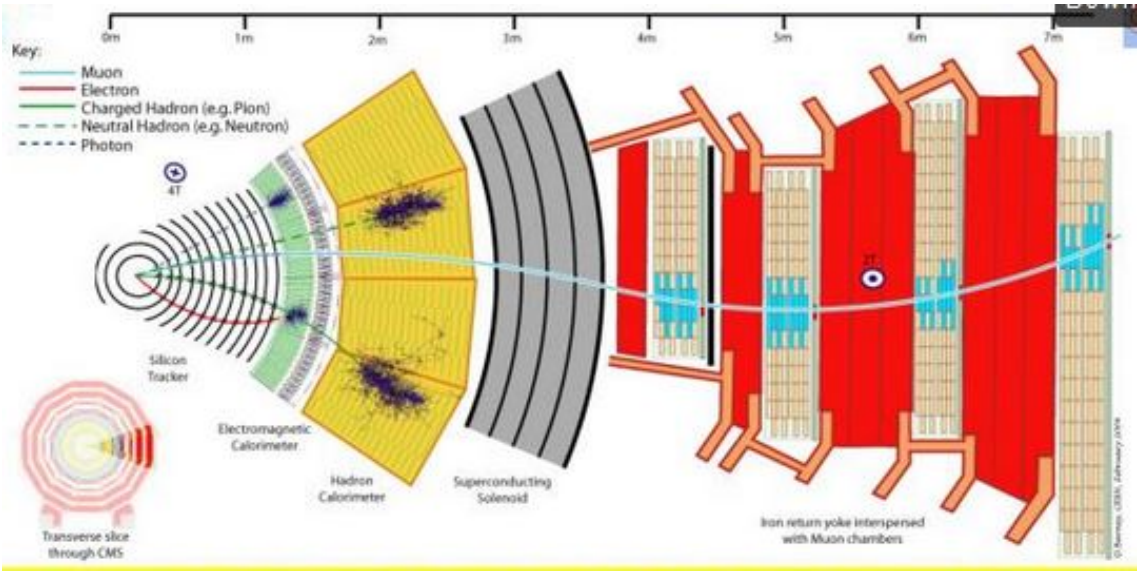

Figure 2.4: Structure of the detection at CMS[1]

This report is based on the work realized on HCAL, however, for Phase 2, CMS experts are planing to unify most of the electronics from HCAL and ECAL, at least for processing and store the data collected.

Triggering

A complex system of dedicated electronics and large computer clusters "filters" the data in quasi-real time to select few hundred events per second. The filter portion of the system is called the "trigger" and the part that records the data is called the Data Acquisition

System (DAQ). The data rate leaving the detector for analysis is over 1Gbps, even with a very efficient trigger system. The final data is stored and made available "off-line" analysis for final physics results and subsequent publications.

The trigger is an extremely fast and automatic process that finds signs of particles with large amount of energy or interesting information for physicists.

The computing process has to be as fast as the reading process. The computers (and electronics in general) have to go under testing constantly and have to be able to select 100 events per second from 100,000 events. The rest of events are thrown out, however, CMS stores and analyses many petabytes of data.

2.1.1 HCAL

The HCAL measures the energy of hadrons like protons neutrons pions and kaons. It also measures indirectly, the presence of non-interacting, uncharged particles known as neutrinos.

The HCAL finds a particle position, energy and arrival time, which gives it the characteristic of sampling calorimeter. It uses alternating layer of "absorber" and "fluorescent scintillator" materials that produce a light pulse when a particle is passing through. Special optical fibres collect the light and send them into read out boxes where the signal is amplified by Hybrid Photodiodes (HPDs). This read out boxes belong to the set of equipment organized in the "Front-End" electronics, and the HPDs are configured specially for CMS. The amount of light is summed up over many layers of tiles in depth (tower) and the total amount of light is considered as the particles energy.

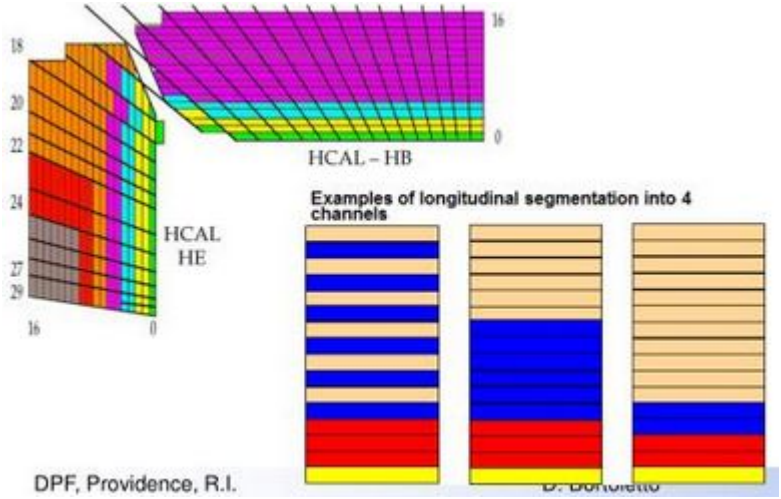

Figure 2.5: Segmentation of the SiPMs at HCAL[1]

The HCAL is organized into barrels (HB and HO), endcap (HE) and forward (HF) sections, as shown in figure 2.5, which performs the job of sub-detectors. Each of these sub-detectors, catch the energy of different particles and as a group, they make sure that no energy is leak out and not being measured.

CMS was part of an international agreement to convert Russian military industry into peaceful technology. For that reason, some of the CMS components were constructed with World War II Russian brass shells[2].

Front-End system

The front-end system is dedicated to detect the light signals from the experiment using Hybrid Photdiodes (HPDs) and amplify them for the next step of processing.

This HPDs can operate in a high magnetic field and give an amplified response. This photodiodes are housed inside readout boxes and receive light signals from the calorimeter by special fibre-optic waveguides.

The light-sensitive surface of a HPD is called photocathode and converts light into electrons (photoelectric effect). inside the HPD, the low energy electrons are quickly accelerated across a narrow gap of a few millimetres onto a silicon diode target. The target is divided up into 19 pixels each of which can generate its own amplified electronic signal when the the accelerated electrons arrive into it. This means that there will be

19 separate calorimetry signals detected and amplified with only one HPD. The signals are amplified approximately 2000 times. The electronic signals are then sampled and digitised for each collision using HCAL-designed integrated circuits called QIE chips (Charge Integration and Encode) and send to the trigger and data acquisition system for analysis.

The hybrid photodiode employed at HCAL is now being replaced by silicon photomultipliers or SiPMs. These are more resistant to radiation that the previous technology, have a better signal to noise ratio and are more reliable for data taking.

The front-end readout system is designed to be modular and flexible to replacements or modifications.

The electronics are constantly tested in "test beams", where scientists and engineers recreate the physical and environmental conditions of the actual experiment. After the electronics have been validated, they are placed into the CMS chambers in a scheduled "shutdown" of the whole experiment.

μTCA Back-End system: μHTR

The Micro TCA is an open and modular standard infrastructure and is mainly dedicated as a platform for telecommunications and computer network equipment. This infrastructure allows to manage Advance Mezanine Cards (AMCs) wich, at the same time, provides the processing and clock to all the cards inside the μTCA.

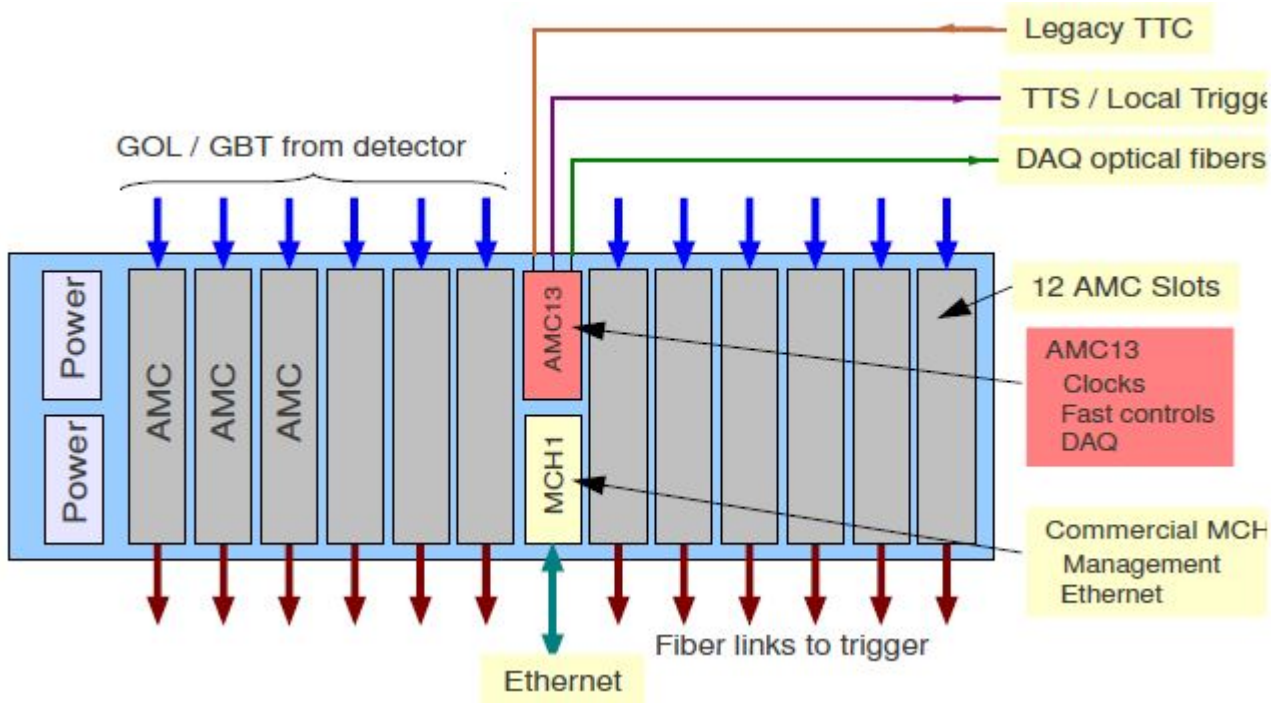

Figure 2.6: uTCA Mechanical Details[11]

For HCAL, this standard provides important high-bandwidth interconnectivity capabilities to handle the increasing front-end data volume from the SiPMs readout. For this reason there are important subsystems installed inside the microTCA at CMS like:

- The HCAL back-end
- TCDS system
- Global Trigger
- Calorimeter trigger
- Muon trigger

The μTCA HCAL Trigger and Readout (μHTR) cards receive front-end digital data, compute trigger primitive information for prompt transmission to the trigger system, and pipeline front-end data during trigger decision time for subsequent transmission to the central DAQ (Data Acquisition) for triggered data. The use of μTCA architecture is

considered as an opportunity to exploit the use of backplane for distribution of synchronisation signals and a possibility to unify ECAL and HCAL back-end system.

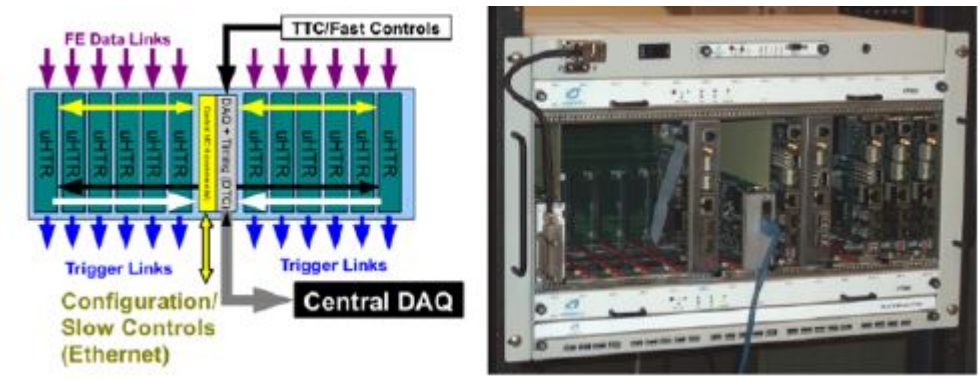

Figure 2.7: Current μTCA configuration at HCAL back-end system

The figure 2.7 shows the μTCA backplane usage for configuration and slow controls, the DAQ data transmission and for fast DAQ back-pressure, timing and trigger controls. The μTCA Data and Timing Concentrator card (DTC) distributes trigger and timing information to the μHTR cards and collects the triggered data for transmission to the central DAQ. The design of the AMC13 μTCA card was made by the HCAL team from the US, including the Calorimeter Trigger Processor Virtex-7 card or CTP7, which has importance for the development of this thesis.

The calorimeter trigger works with an algorithm in order to accept and reject data from the experiment. The efficiency of the calorimeter trigger, depends on the processing power of FPGAs and on the state-of-the-art Telecom technology to support the increased bandwidth requirements imposed by the higher granularity of the trigger input data.

The CMS calorimeter trigger's efficiency is based on the capability of recognize trigger objects such as photons and electrons, muons, τs, jets and transverse missing energy.

The front-end is connected to the back-end through a number of high speed data links of 1.6 Gbps and 4.8/5 Gbps, like data links that carry DAQ data from the front FPGAs to the back FPGAs, data link which carries luminosity and self-trigger information from front FPGA to back FPGA (LHC synchronous 4.8 Gbps or 3.2 Gbps), trigger links and the DAQ data output format to AMC13/DTC.

For the Data Aquisition system (DaQ)at the HCAL, there are 8 channels dedicated to

the transportation of the data from the front-end to the back-end electronics, in optical links of 5Gbps, however, the HCAL still uses a speed of 4.8 Gbps for this communication. The purpose of the new firmware of the CTP7 cards is to allow the HCAL to increase the speed and efficiency of data transmission.

2.1.2 LHC and TCDS: the clock system

The LHC distributes the timing, trigger and control signals (TTC) to all of the electronics systems of the subdetectors[3] and its collision rate is of 40MHz which means that every 25 ns there is a collision inside the LHC. The data is received at this frequency.

The phase-noise characteristics of the clock signals given by the TTC systems, are not compatible with the jitter requirements of the data serializers for a Gigabit optical communication. For this reason, it was necessary to develop Quartz crystal based Phase-Locked Loops, or QPLLs, that help to filter jitter effects in LHC experiments[4].

In 2015, CMS phased a new problematic when the TTC reached its limits in terms of the number of separate elements that could be supported. In order to solve this situation, it was necessary to create a new Timing and Control Distribution System or TCDS. The TCDS is responsible for sending the triggers, clock and fast control signals to the CMS subsystems. TCDS is based on the μTCA standard and it consist of 3 main boards: the Central Partition Manager (CPM) which is located on an AMC13, the local Partition Manager (LPM) whch is based on the FC7 and the Partition Interface (PI) which is also based on the FC7. The FC7 is a μTCA compatible card for generic CMS data acquisition and system control uses.

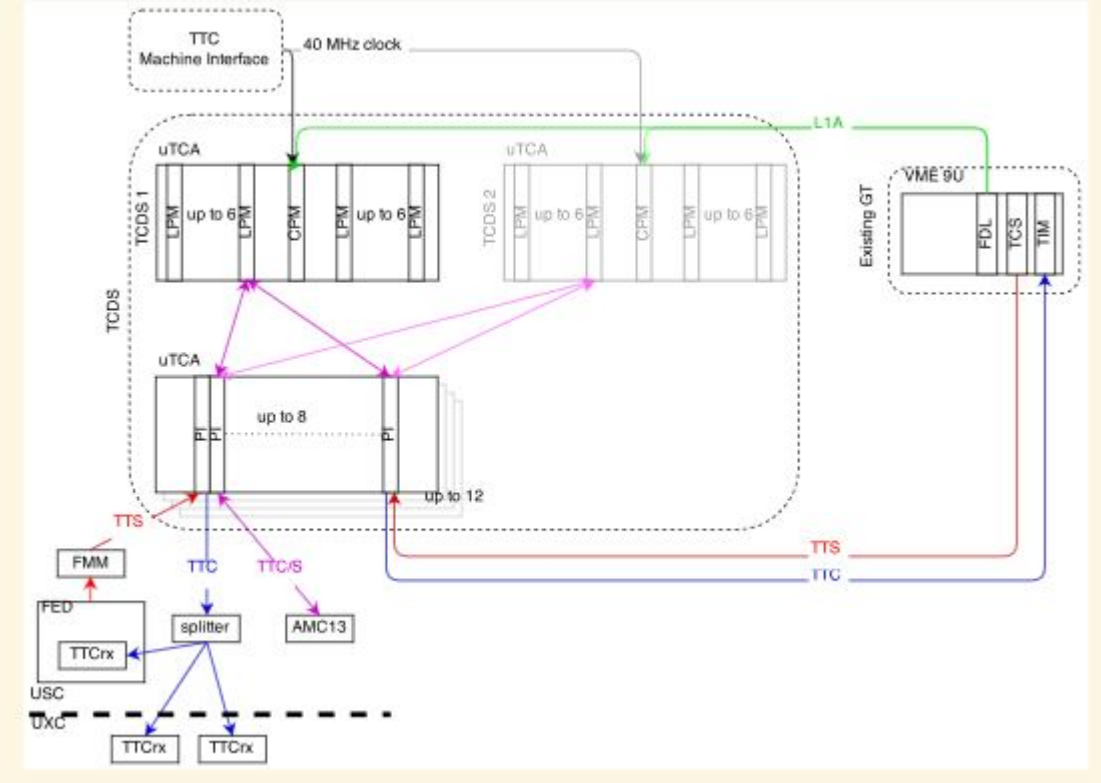

Figure 2.8: TCDS system overview

The figure 2.8 shows the organization of the TCDS system. Is possible to see that it incorporates other TTC signals like TTS or Trigger Throttling System used for monitoring problems with the TCS. The TCS or Trigger Control System is other signal incorporated to the TCDS and is the conductor of CMS data-taking. The TTCmi or the machine interface is in charge of receiving the clock and synchronisation signals from the LHC and the LHC RF system. One specific feature of the new Timing and Control Distribution System is to have additional partitions for the luminometers, trigger upgrades, spectrometers, etc.

Chapter 3

CTP7 CARD AND ARCHITECTURE

3.1 CTP7 architecture

The Calorimeter Trigger Processor card or CTP7 Virtex-7, was designed to cover the requirements of higher and simpler processing, for the large amount of data that is collected on each run of the experiment. This card is a combination of a Virtex-7 FPGA, a ZYNQ System on Chip and AXI infrastructure.

The card was designed for a Micro TCA telecommunications architecture because it allows to build high performance electronics in a small form factor, which was a requirement for the next generation of electronics in the Calorimeter Trigger update[5].

For the CTP7, the μTCA crate, has an specific AMC called AMC13, for the optical connections and the clock coming from the Data Acquisition (DAQ) and the LHC (TTs).

The CTP7 was designed by the Physics Department of the University of Wisconsin and the firmware was implemented by the Wisconsin's Firmware Design group.

Inside the CTP7, the virtex-7 FPGA works as a primary processor and the ZYNQ, provides the board support functions and TCP/IP communication.

Previously, for Phase 1, the card included 2 fpgas Virtex-6. It was necesary to change one of them with a Virtex-7 FPGAs, to have enough computational power for larger amount of data result of the increment of the luminosity inside of the experiment.[**?**] The use of a ZYNQ SoC in replacement of the other fpga Virtex-6 will simplify the use and control of the card.

Figure 3.1: CTP7 Card with Virtex -7 and ZYNQ FPGAs[5]

The CTP7 card includes 10 gigabit transceivers for optical communication. 36 TX and RX links on three CXP modules. In addition there are 12 TX and 31 RX links on the MiniPods modules. There are also 14 TX and 14 RX backplane optical links.

On the backplane, there are additional 10 Gigabit-Ethernet (GbE) and Data Acquisition (DAQ) links. The GbE can operate synchronously and asynchronously with the LHC clock provided by the crate infrastructure. The GTH transceivers have access to two reference clocks, simultaneously, to support a multi-rate use model for multiple reference clock input, from TTC or oscillator sources. Two clock frequencies are distributed on each side of the FPGA. thanks to this, the CTP7 can support all the proposed combination of link speeds. On figure 3.1 is possible to see the location of each basic component of the CTP7 card.

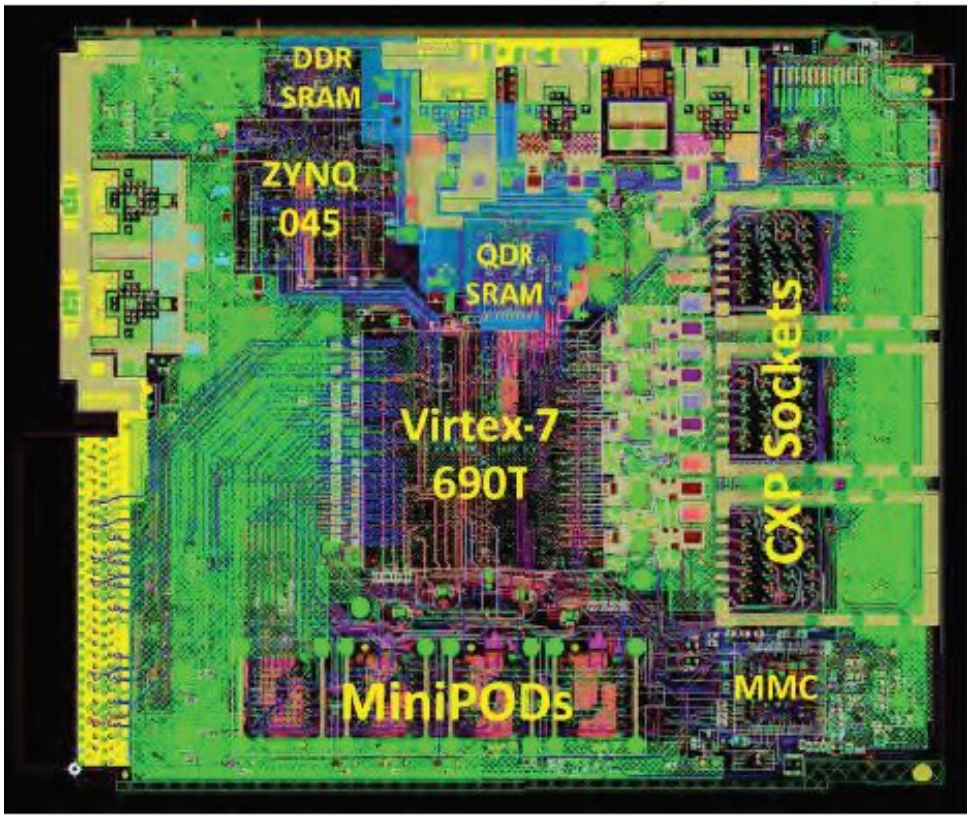

Figure 3.2: CTP7 Card CAD view[**?**]

3.1.1 ZYNQ system on chip

ZYNQ is a System-on-Chip (SoC) technology, created by Xilinx, that provides a dual ARM Cortex-A9 processor with capability of running up to 667 MHz and a capacity of 256 KB of on-chip RAM, and a Kintex-7 FPGA in the same package The ZYNQ SoC runs embedded Linux OS, which allows the designers the use of scripts to have a easier control of the firmware and hardware of the card by physicists or programmers. ZYNQ allows the user, to access remotely to the card with a TCP/IP connection, thanks to the ZYNQ based Xilinx Virtual Cable. This is useful to avoid JTAG connection inside of the μTCA crate. The ZYNQ is considered the backend of the CTP7 and its firmware is responsible for the drivers of all the peripherals including:

- the micro-sd card driver
- DDR memory
- I2C for all peripherals

- MMC interface
- AXI chip-to-chip bridge
- Ethernet
- TTC interface

3.1.2 AXI architecture

AXI (Advanced eXtensible Interface) protocol is part of ARM AMBA, a family of micro controller buses adopted by Xilinx for Intellectual Property blocks (IP) starting with Spartan -6 and Virtex -6. The protocol was first introduced in 1996.

The AXi infrastructure was implemented on the CTP7 design, to allow flexible and modular tools with the main objective of reduce time between project conception to final implementation.

There are three types of AXI4 interfaces[7]:

- AXI4: For high performance memory-mapped requirements.
- AXI4-Lite: for ismple, low-throughput memory-mapped communication (for control and status registers).
- AXI4-Stream: for high-speed streaming data.

Xilinx also gets flexibility when using AXI interfaces, for example, by using AXI4, it allows to burst up to 256 data transfer cycles with only one single address phase. With AXI-Lite, is possible to use a simpler interface, in design and usage. With AXI4-Stream, allows unlimited data burst size. Availability is another benefit for using an industry-standard because it's possible to have access not only to the Xilinx IP catalog, but also to other ARM partners.

AXIs exchange information between a master and a slave interface. Memory mapped AXI masters and slaves can be connected by using an Interconnect structure that contains AXI-compliant master and slave interfaces, and can be used to route the sending

and receiving data between more than one AXI master/slaves. The data can move simultaneously from master to slave in burst of data of up to 256 data transfers for AXI4 and only one data transfer for AXI4-Lite.

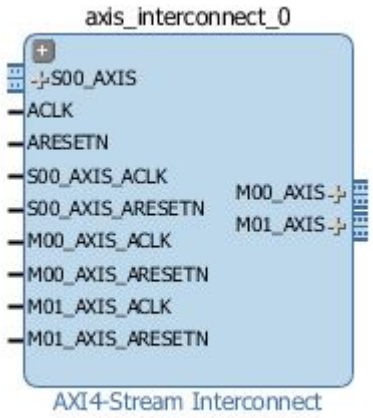

Figure 3.3: AXI Interconnect Infrastructure[8]

AXI4 and AXI-Lite interfaces consist of five channels:

- Read Address Channel
- Write Address Channel
- Read Data Channel
- Write Data Channel
- Write Response Channel

AXI makes sure that IP blocks can exchange data with each other and their interoperability can affect the space of the IP application, the way IP interprets data and the kind of AXI protocol it should be used (AXI4, AXI4-Lite or AXI-Stream), this means that AXI can define how data is exchanged, transferred and transformed in a predictable way.

AXI is compatible with Ethernet MAC (EMAC) or Video Display IP by using the specific module that allows streaming (AXI4-Stream).

The AXI4-Stream Protocol is used for applications that are focus on data-flow and data-centric transmissions, where there is not necessary the use of an address. Each AXI4-Stream behaves as a single unidirectional channel for a handshake data flow. Meanwhile, the memory mapped protocol (AXI, AXI4-Lite) work around a defined memory map and use specific addresses for data. It is possible to use Direct Memory Access (DMA) engines for a memory mapped to stream conversion.

The AXI Chip-to-Chip (Chip2CHip) is an adaptable block and soft Xilinx IP core to use with the Vivado® Design Suit, that provides bridging properties between AXI architecture and SoC devices.

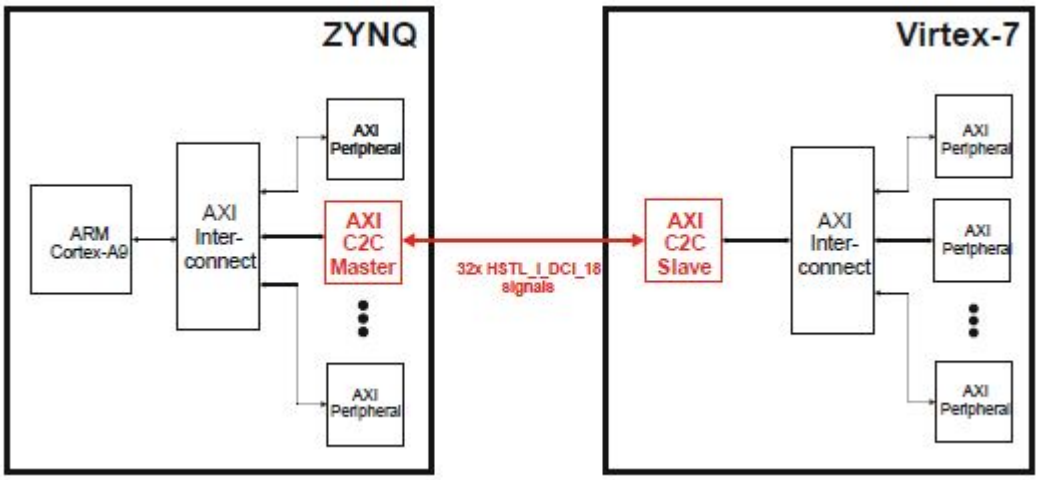

Figure 3.4: AXI Chip-to-Chip connection

Inside the CTP7, the ZYNQ FPGA already use AXI infrastructure and Chip2Chip to move data from/to processor and peripherals. This allows extend the memory on the ZYNQ FPGA, to the Virtez-7 FPGA.

Xilinx provides a wizard to create AXI blocks that generates HDL code templates for the user.

3.1.3 GTH transceivers

The GTH transceivers, from the 7 series FPGAs, are power-efficient and support rates up to 13.1 Gb/s for optical communication. Are configurable and integrated with the programmable logic resources of the FPGA. It provides different reference clock input options and support a LC tank (PLL) and ring oscillator (CPLL) to drive the TX and

RX data-path. Every characteristic of the GTH transceiver is managed by a register file inside the CTP7 firmware. All the GTH transceivers have simultaneous access to two reference clock sources to allow a multi-rate use model without restrictions on link allocation in the firmware design.

3.1.4 8bto10b encoding

This encoding is mainly use for high speed optical serial data communication to ensure sufficient data transitions for clock recovery. The 8b10b coding was initially proposed by Albert X. Widmer and Peter A. Franaszek from IBM Corporation in 1983. A basic communication system, like shown on the figure 3.5, the encoder on the transmitter side maps the 8 bits into 10 bits. Then, this 10 bits are shifted out through a high speed serializer (Parallel-in Serial-out 10 bit Shift Register). The serial data stream is transmitted to the receiver via optical fibre. On the receiver, there is the high speed deserializer (serial-in parallel-out 10-bit shift register) and converts the received serial data stream into parallel. Then, the decoder will remap the 10-bit data back to 8 bit data.

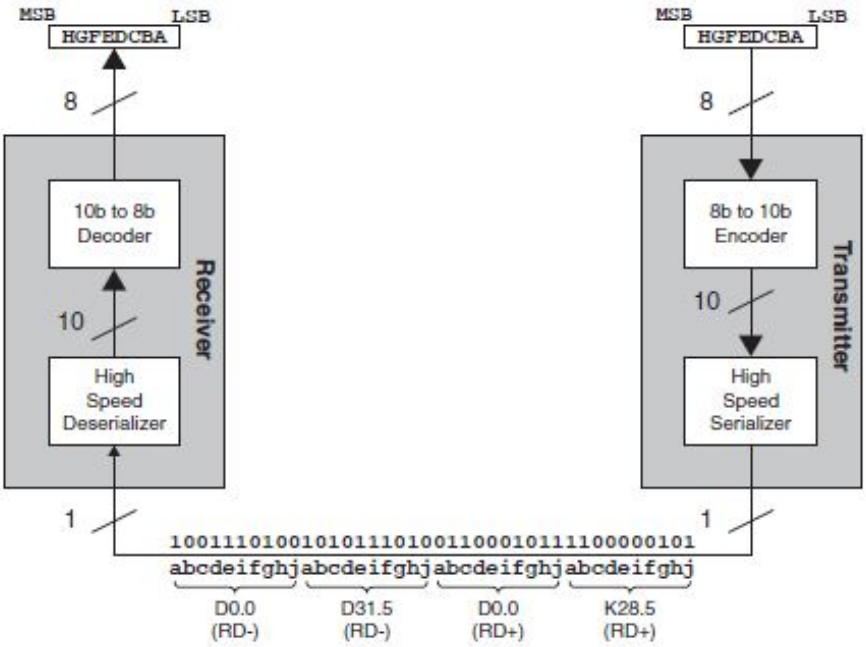

Figure 3.5: 8b10b encoder/decoder usage in a communication system

The main purpose of using this encoding in a high speed communication system is to

have DC balance and run length. A DC-balanced serial data means that it has the same number of 0s and 1s for given length data stream. This avoids to build up charge inside the media.

The run-length is defined as the maximum numbers of contiguous 0s and 1s in the serial data stream. When the run-length is small, it provides small transitions within a small length of data. Data transitions are very important for clock recovery. The PLL of the CDR (Clock and Data recovery) generates a phase-adjustable output clock from the reference clock input. Transitions on the serial data stream provide the transmission clock phase information to the PLL and allow the PLL to recover the transmission clock with the correct phase.

The input reference clock is necessary for the CDR. The serial data stream embeds the phase of the transmission clock. The reference clock comes from the receiver system, not the transmitter.

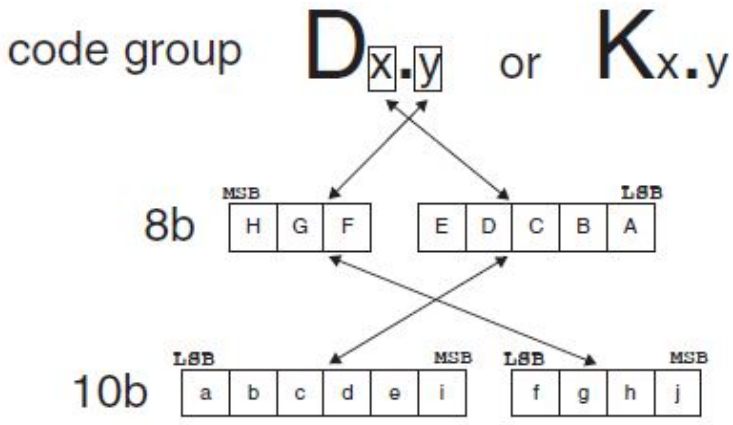

Figure 3.6: 8b10b code mapping

This encoding breaks the 8 bit word into two blocks, three most significant bits (y) and 5 least significant bits (x). From the most significant bit to the least significant bit, they are named as H, G, F and E, D, C, B, A. [9] The 3 bit block is encoded into 4 bits j, h, g, f. The 5-bit block is encoded into 6 bits i, e, d, c, b, a as shown in figure 3.6. Finally, the 4-bits block combined with the 6-bits block into a 10-bits encoded word.

In the 6-bits and 4-bits blocks there should be a case of disparity neutral (number of 1s is equal to number of 0s) which allows to create a DC-balanced data stream. but

there are only few combination of bits in which the blocks can have disparity neutral. This combinations are dependant of the table of values of the encoding 8b10b.

Control symbols

Input				RD = −1	RD = +1
	DEC	HEX	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	28	1C	000 11100	001111 0100	110000 1011
K.28.1 †	60	3C	001 11100	001111 1001	110000 0110
K.28.2	92	5C	010 11100	001111 0101	110000 1010
K.28.3	124	7C	011 11100	001111 0011	110000 1100
K.28.4	156	9C	100 11100	001111 0010	110000 1101
K.28.5 †	188	BC	101 11100	001111 1010	110000 0101
K.28.6	220	DC	110 11100	001111 0110	110000 1001
K.28.7 ‡	252	FC	111 11100	001111 1000	110000 0111
K.23.7	247	F7	111 10111	111010 1000	000101 0111
K.27.7	251	FB	111 11011	110110 1000	001001 0111
K.29.7	253	FD	111 11101	101110 1000	010001 0111
K.30.7	254	FE	111 11110	011110 1000	100001 0111

Figure 3.7: 8b10b K characters

The encoding and decoding is managed on the firmware for the CTP7. The used of the values depend on the data format documents used at CMS experiment.

3.1.5 Data format

The data received, after the 8b10b decoding , has a specific format according to HCAL documents and standards. In CMS, the K characters are used to give specific control information from the front-end system for example, from table 3.7, the character K 28.5 is a Comma character and its main purpose is synchronization. This character is on the first 16-bits block of the received data in hexadecimal format as BC. This byte is the bunch counter alignment marker which is sent once per orbit at an agreed phase, it means that it's the beginning of the data block. It's also known as the byte 0. Bytes 1, 10 and 11 are the TDC (Time to digital converter) bytes and indicate the measurements from inside the QIE cards about the time of the events. Bytes from 2 to 9 are the sampled

data coming from the QIE (Charge Integration and Encode) chips

3.2 CTP7 Virtex-7 firmware

The Virtex-7 firmware is considered the Front-end of the CTP7 card and its composed by some major blocks like:

- Clock and control configuration
- QDR Memory
- CXP links
- MiniPOD links
- Input data capture to BRAM
- EDecoding of input data ECAL: 4.8 Gbps TPGs for 2016+ HCAL: 6.4 Gbps TPGs for 2016+
- DAQ buffering
- Packetization for DAQ
- Output playback from BRAM, etc

The designers opted for a modular firmware approach, thanks to AXI interconnect protocol family, which allows to connect with existing firmware blocks for a faster configuration[10].

One important block from the AXI IP catalogue, for this firmware, is the standard AXI BRAM Controller that works as a memory mapped device to manage user signals (read, write, enable, address write/read). This block helps to integrate AXI infrastructure and custom peripherals.

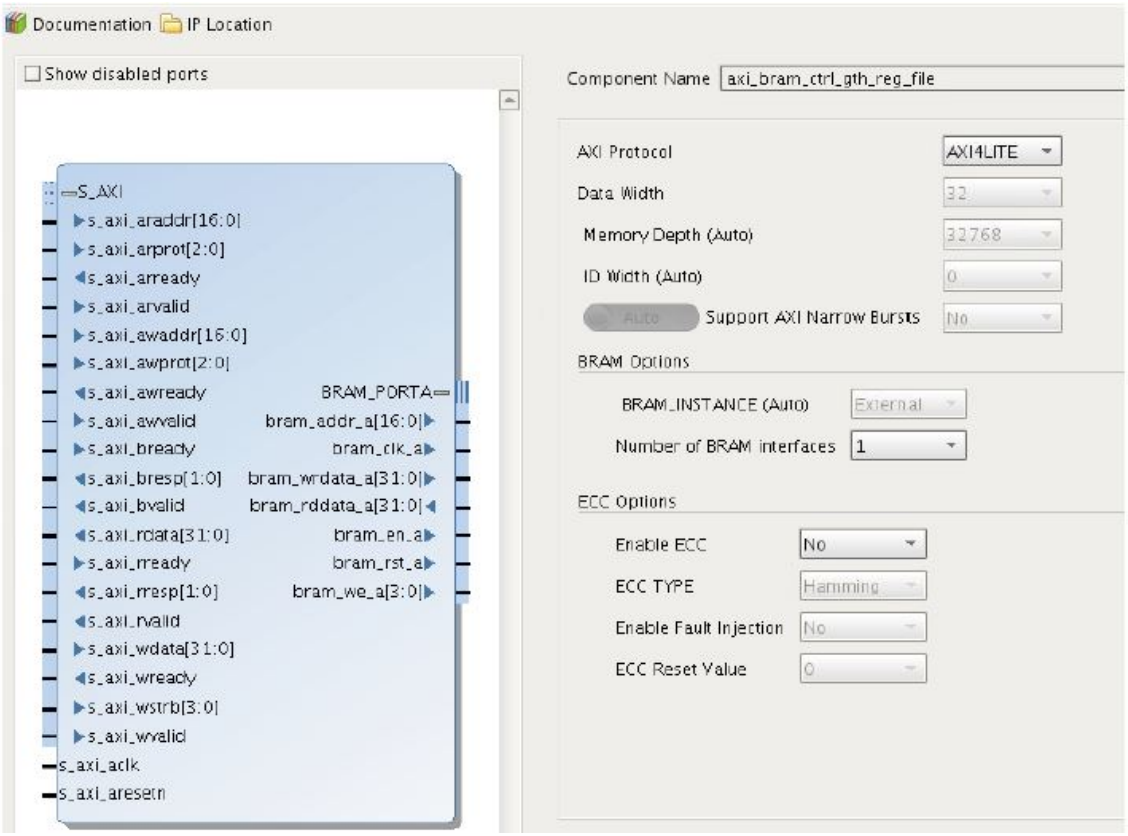

Figure 3.8: Input/output signals of the AXI BRAM Controller

The demo was realized as a project of Xilinx Vivado 2016.4 and its purpose is to manage the different clock and the incoming data from the Data Acquisition (DAQ) Electronics. It simulates the process of transmission and reception of data, through the optical connection with a speed of 5Gps. The demo allows to access the specific register for the internal loopback connection of the GTH transceiver and check if the data received is correct.

The figure 3.9 shows the general schematic of the structure of the demo. Every 250/6 MHZ (41.6 MHz) a block of 12 bytes needs to be encoded in the transmitter (8b10b) before send it into the optical link with a speed of 5 Gbps. This means that blocks of 20 bits will be transmitted with a frequency of 250 MHz. The *Pattern Generator* block, simulates the data going to the transmitter at 240 MHz in blocks of 16 bits. The transmitter (Front-End electronics), performs de encoding and the opposite operation is done by the receiver CTP7 (Back-End electronics).

For the encoding, the transmitter adds *filling* words (F7 and FB), according to the *HB*

Data Format document mentioned before. The job of the pattern checker is to compare the data from the pattern generator and the data from the receiver.

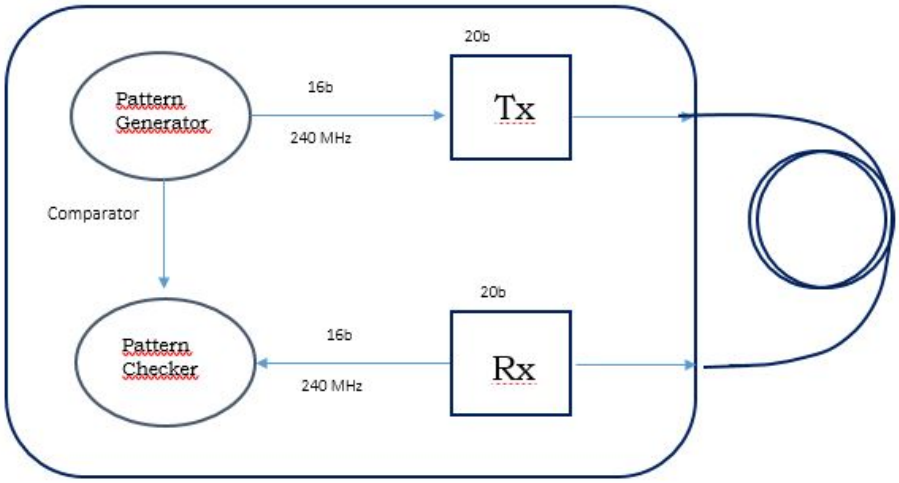

Figure 3.9: Transceiver of CTP7

The structure of the firmware is describe in the figure 3.10. The TOP level block contains the IP Block Diagram (BD) that manage the connection and use of the AXI infrastructure and the connection to the ZYNQ. There are two blocks dedicated to manage the registers, one for the GTH transceiver and one for the other interfaces like the TTC.

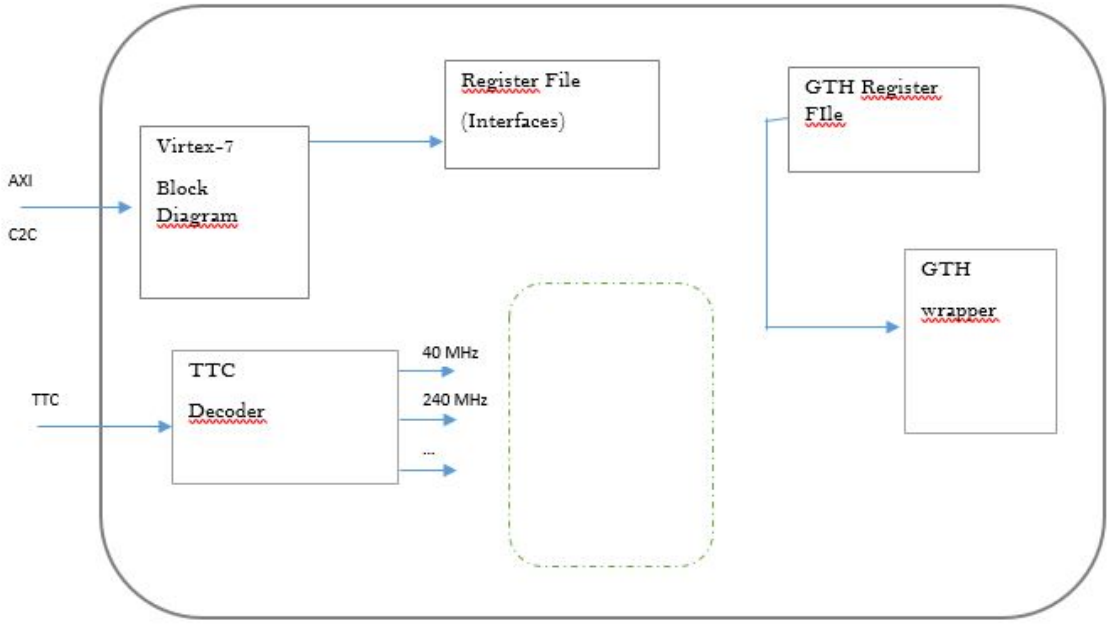

Figure 3.10: Structure of the CTP7 firmware

The GTH register file is connected to the GTH wrapper that allows to connect with

the QPLL (reference clocks). The TTC decoder receives the clock signals from the TTC and distribute them to the rest of the blocks.

The data received still contains some errors and needs to be classified according to the Data Format document mentioned before.

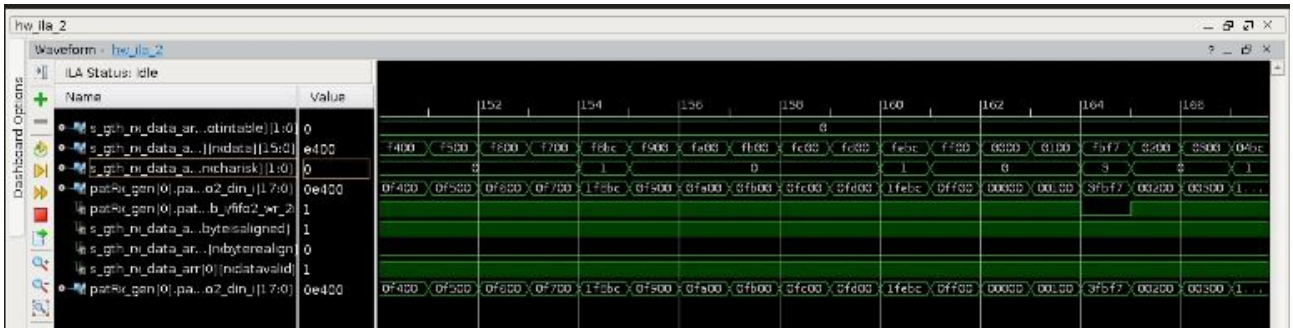

Figure 3.11: Waveform of the signals on the receiver

The second and the third signals, shown on the figure 3.11, are the data signal and the "k" character respectively. The data coming from the pattern generator to the receiver, simulates an 8 bit counter. Each 8 bit words, there is a bc word, giving the beginning of the 12 byte data block. For each BC word, the *k character* is equal to *1*. If the data from the receiver is a filling word, then the *k character* will be equal to 3 and if it's a valid data, the *k character* will remain as *0*. After that process, it can be included into a IP BRAM for storage and then incorporate it to the AXI infrastructure, using one of the BRAM AXI controllers available on the CTP7 demo.

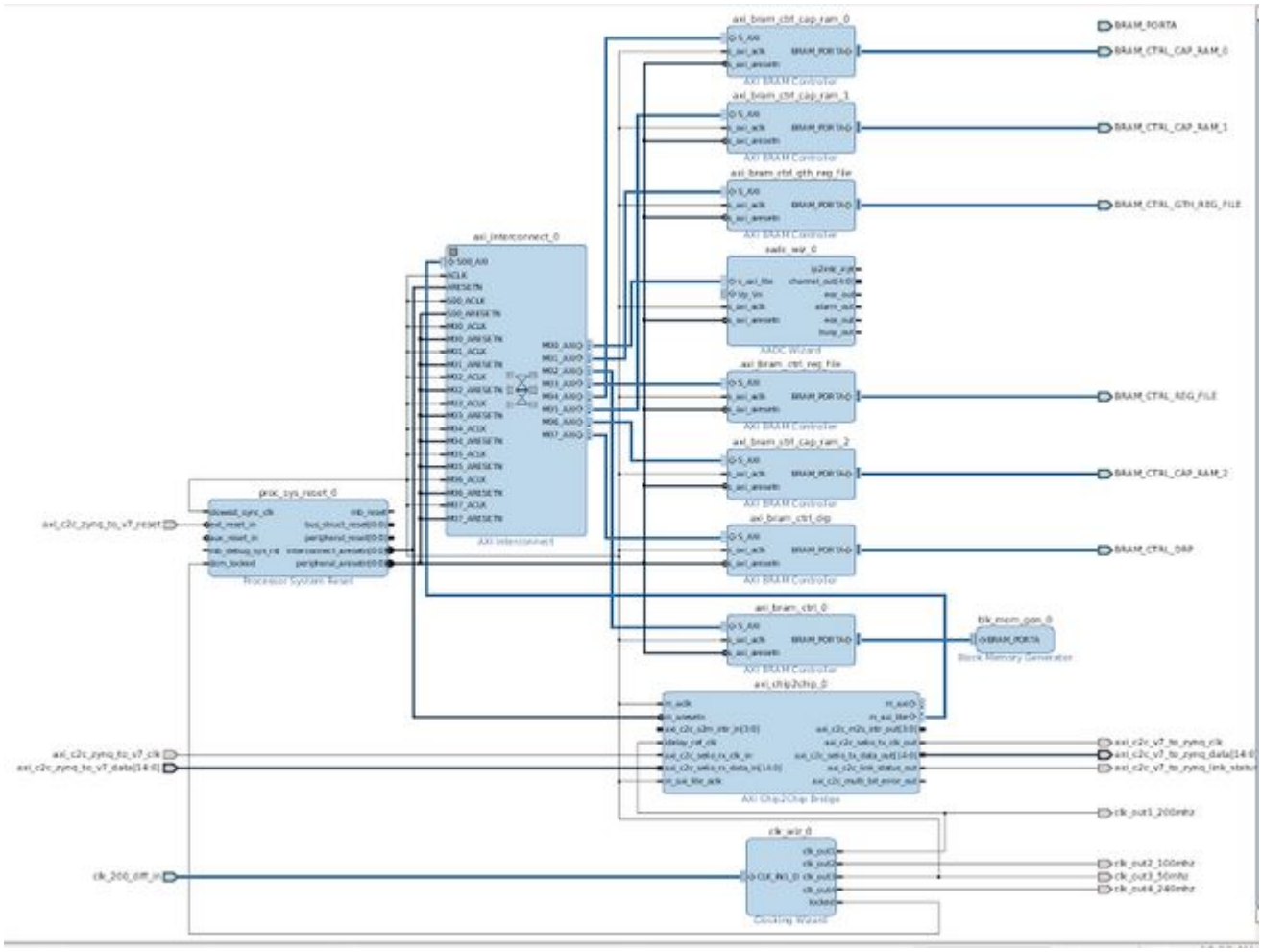

Figure 3.12: AXI infrastructure for the CTP7 demo

The figure 3.12 shows the AXI infrastructure designed for the CTP7 demo. Four of he seven AXI BRAM controllers are used by the registers files from the firmware. The other three are available for the user. All of the blocks are connected to an AXI Interconnect block to manage the BRAM signals (address, read, write, etc). Inside the infrastructure there is the clock block connected to three different clocks 50, 100 and 240 MHz for different blocks inside the demo. It also includes the AXI chip2chip Bridge to connect the ZYNQ with the Virte-7 and finally the Processor System Reset.

Chapter 4

DESIGN OF THE DATA DECODER

The job of the decoder is to collect the data from the receiver, select the useful data and eliminate the errors. The useful data, at the same time, will be decoded according to the Data Format document.

The availability of the cards was very limited, for this reason the design of the decoder remains as a simulation.

As a first step it was necessary to recreate a pattern generator (rx data gen) to simulate the 16 bits words at the receiver and the 2 bits signal for the k character (kchar gen).

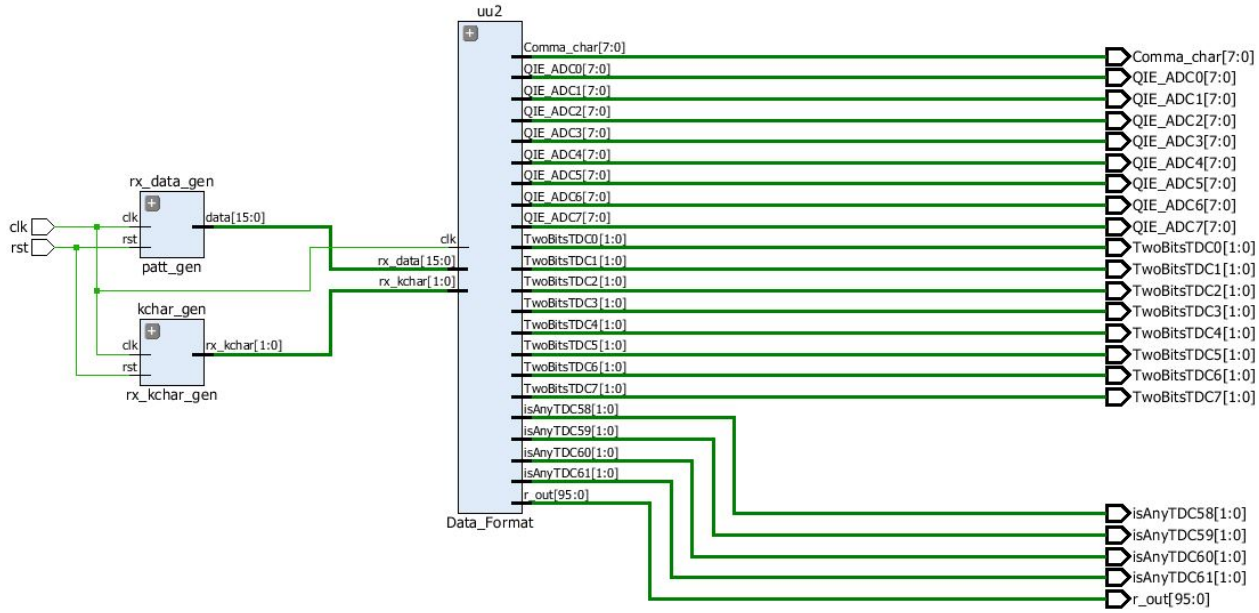

Figure 4.1: Data generator, k character generator and decoder connection

The k character will tell the decoder the beginning of the 12 byte data block that is

going to be analized and if there is any filling word from the 8b10b encoder.

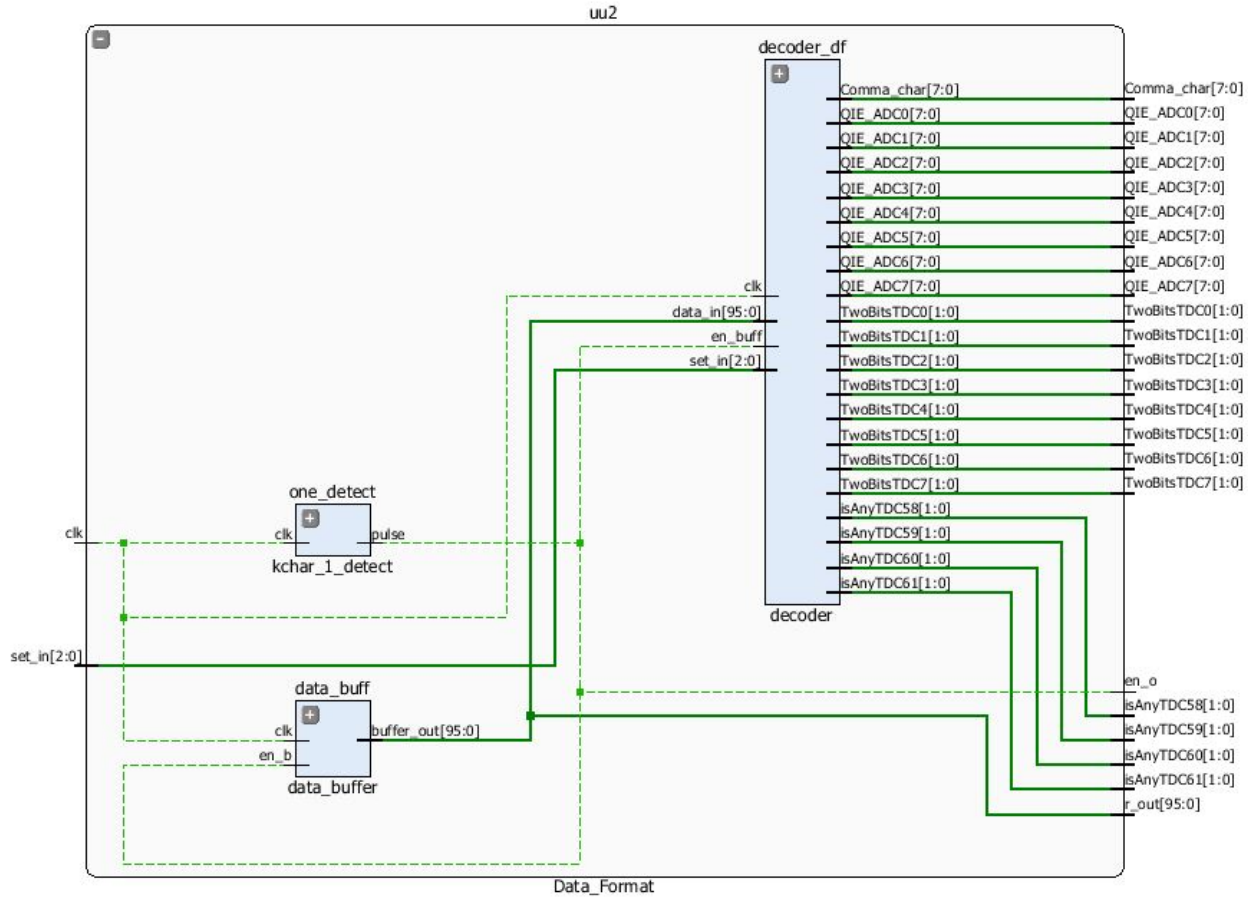

Figure 4.2: Proposed decoder

The decoder has a block that will detect when the k character is equal to 1 and will create a pulse to enable the next block (data buffer). The data buffer will collect and select the 12 bytes in a big block of 96 bits. In this step, the filling words are eliminated. After, the block of 96 bits go to the data format block, where it's separated into 12 blocks of 8 bits and later, separated according to the HB Data Format document explained on the previous chapter.

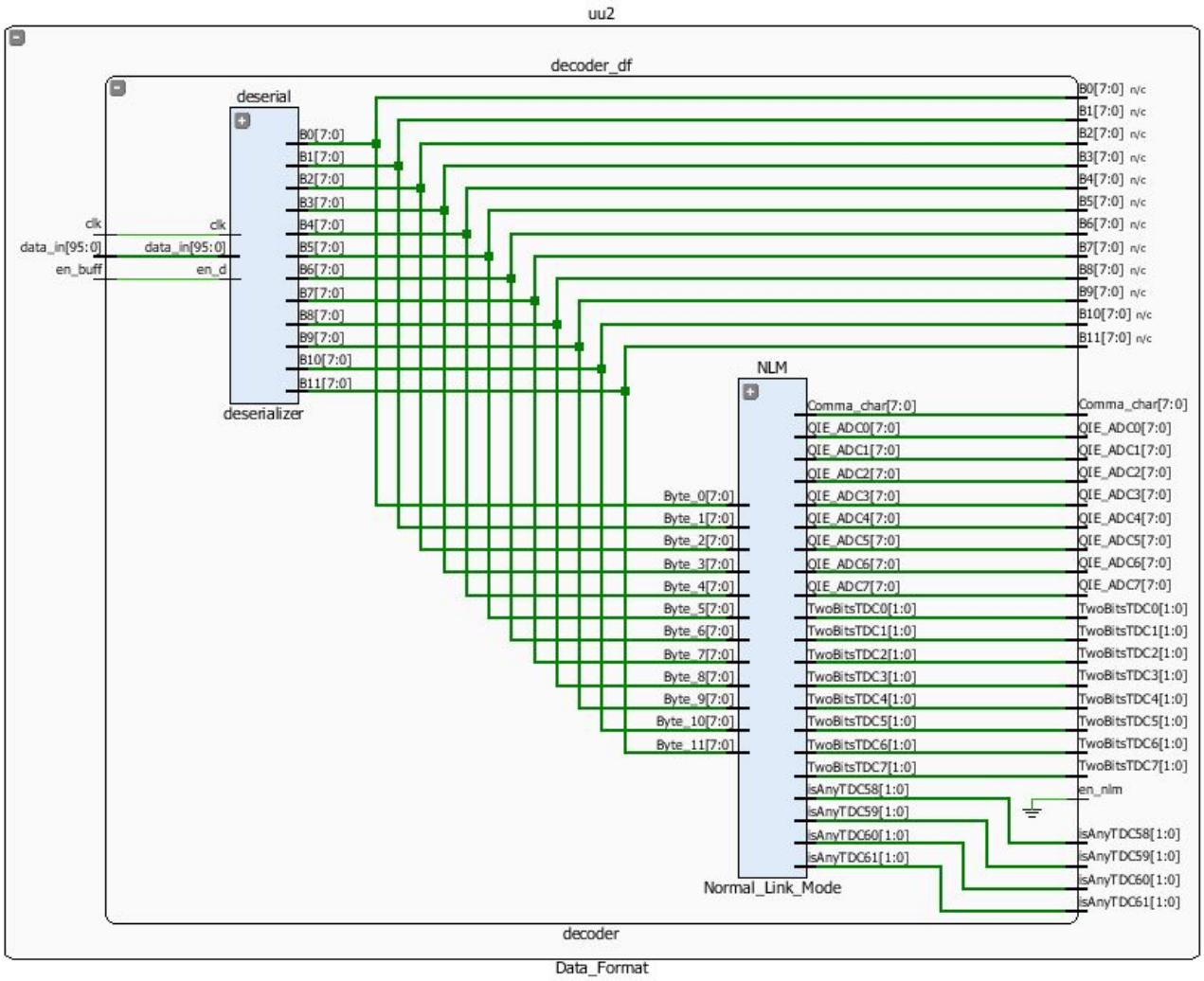

Figure 4.3: Data Format block

In figure 4.4, it's possible to see the waveform of the signals simulated.

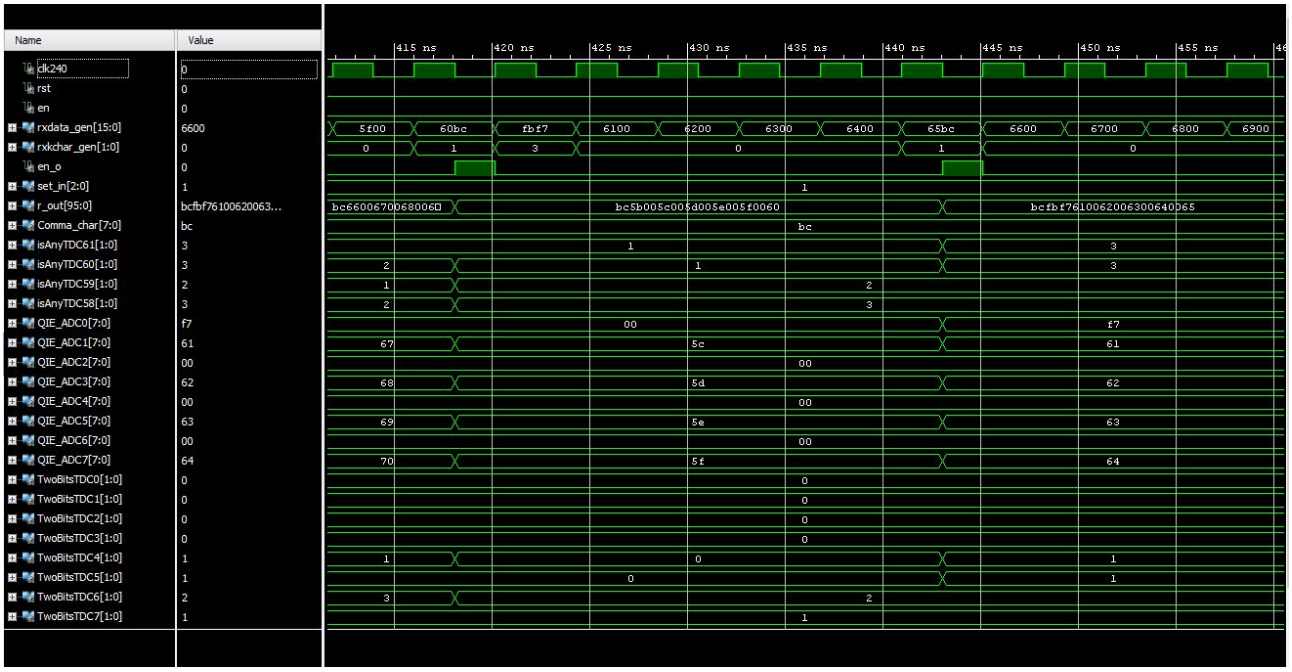

Figure 4.4: Simulation of the Decoder

The next step, after the simulation, it was planned to test the Data buffer into the CTP7 demo, using the AXI infrastructure already proposed on the demo.

The data collected into the *buffer* block (96 bits), without the filling words were stored into an IP BRAM block connected to an AXI BRAM controller from the existent AXI infrastructure. This last task wasn't tested because of lack of available CTP7 cards and it remains incomplete.

CONCLUSIONS

The migration to a new technology is crucial for the survival of any long term experiment. CERN and specifically CMS is not an exception. Several new cards and modules are being tested for Phase 2 that will take place tentatively in 2020.

So far, the test of the new CTP7 card allows to take a great advantage of the Virtex-7 processor for the optical communication between front and back-end electronics inside CMS. Meanwhile the Zynq allows to implement software algorithms on a high speed processor and provide ancillary functions and extensive board monitoring. Thanks to the new clocking infrastructure of the CTP7 which allows the use of multiple spees systems, it is possible to integrate HCAL and ECAL systems in the same μTCA crate, how ever this is only possible in laboratory tests so far.

In simulation and in laboratory tests, the new speed of 5 Gbps is possible thanks to the new CTP7 card, however there are concerns about if the rest of electronics will respond favourable to this new change with real conditions of data transmission and radiation.

The addition of the standard AXI buses with the CTP7 firmware, allows to reduce time and improve flexibility for integration between the firmware and IP blocks. In this case, the update of the firmware to move the data transmission from 4.8 to 5 Gbps didn't need any change on the IP design or AXI architecture.

The experts and engineers bet for an upgrade of the FPGA for the final design of the cards for Phase 2, if the results are good enough with the CTP7 after this period of testing in laboratory.

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