UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio de Posgrados

Design of a low-voltage low-power CMOS current reference

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Trabajo de titulación de posgrado presentado como requisito para la obtención del titulo de Magíster en Nanoelectrónica

Quito, 21 de Mayo del 2019

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HOJA DE APROBACIÓN DE TRABAJO DE TITULACIÓN

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Firmas

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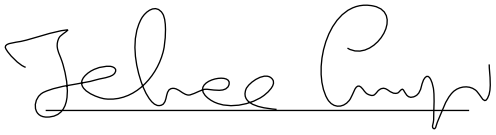

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To the hands of my father,

to the love of my mother,

and my adored sisters.

Resumen

Hoy en día, los espejos de corriente o *current reference*, pueden ser mejorados con las características de inversión débil *subthreshold-region* cuando son construidos con tecnología CMOS, está tesis trata sobre cuatro estructuras de *current reference* basadas en un circuito de solo tres transistores, las figuras de merito como coeficiente de temperatura, consumo de potencia, y sensibilidad de carga y proceso son obtenidas en cada una de las estructuras, y posteriormente son comparadas para disernir cual de las implementaciones ha presentado un mejor desempeño. Las simulaciones fueron realizadas en una tecnología de 180 nm, nanómetros, TSMC CMOS usando transistores de tipo *MEDIUM VOLTAGE THRESHOLD* (MVT) para un voltaje máximo de alimentación de 2 y 3 voltios. La tesis esta compuesta de cuatro capítulos, el primero muestra los principios físicos para inducir una corriente cuando el transistor MOSFET se encuentra en la región de *subthreshold,* lineal y saturación. El segundo capitulo muestra las especificaciones tomadas en cuenta para implementar los cuatro diferentes diseños, como son el dimensionamiento y los parámetros eléctricos de las fuentes de alimentación, los diseños fueron implementados en Virtuoso de Cadence. El tercer capitulo muestra los resultados obtenidos en cada uno de los circuitos y una comparativa de las figuras de merito calculadas. Finalmente, el cuarto capitulo muestra las conclusiones de cada bloque, los beneficios obtenidos al implementar cada uno de los diseños así como la mejor solución acorde a las figuras de merito obtenidas.

PALABRAS CLAVE: *espejo corriente, CMOS, inversión débil, MOSFET, consumo, potencia, coeficiente temperatura, sensibilidad carga.*

Abstract

Nowadays, the current reference circuits can be improved using the CMOS weak inversion characteristic, this thesis deals different current reference structures in order to design a circuit which figures of merit can be reduced like the temperature coefficient, power consumption, and load and process sensitivity. Simulation results related to the 180 nm TSMC CMOS process are shown to evaluate the benefits of the proposed solutions. The thesis is composed of four chapters, the first chapter shows the physic principles to induce a current when the transistors are in subthreshold, linear and saturation regime over a MOSFET. The second chapter shows the specifications at technology, sizing and electric level in order to implement the designs in Virtuoso of Cadence. The third chapter shows a discussion about the findings obtained in each one of the circuits implemented, and how the figures of merit have been reduced. Finally, the fourth chapter shows the benefits of each block that composes a certain design, and the best solution is mentioned.

KEY WORDS: *current reference, weak inversion, low power, low voltage, CMOS, temperature coefficient, load sensitivity*

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Sub-micron CMOS technologies had opened a new branch to design low power structures, at the same time these are more dependent on temperature and process. Some of these structures could be: the current and voltage reference whose goal is retaining a value as much as possible while the temperature changes. On the other hand, the scaling has allowed to integrate and improve the density when the CMOS technologies are used but the temperature dependence has increased too. Mainly sub-micron transistors have problems to handle the temperature changes. In addition, each working transistor region can be used to create new circuits with different topologies, one of these is the subthreshold or weak inversion region which behavior can be used to control the diffusion current with the temperature changes.

The low-power design, especially in the IoT and biomedical applications, is a field with a constant growth. Reducing the power consumption is one of the main items to treat at the designing time, this is the reason that new methodologies have been studied, one of them is the current reference circuit, which aim is the giving a voltage and current stable with a certain dependence level about the temperature and process sensitivity. This section discusses the function principles inside of CMOS to perform in low-voltage mode, the reference circuits needed to implement a voltage and current reference, the parameters to evaluate its performance and the latest

researches about voltage generator and current references.

1.1 Function Principles

In this section, the main principles to design a voltage and current reference are explained. First, the temperature and process sensitivity are explained as main factors for low power designing, the zero temperature coefficient (ZTC) point, as parameter to lead the voltage reference to the optimum working point, which is focused in the mutual cancellation of temperature dependence of the threshold voltages and thus the mobility of the charge carriers. Secondly, the weak inversion region where the transistor should work in order to have the lowest power consumption as possible. Finally, the self cascode arrangement, useful for low voltage analog circuit, is explained and its dependence to the voltage supply variations.

1.1.1 ZTC point

The transconductance characteristics in function of the temperature, for a NMOS transistor is shown in Fig (1.1), where the ZTC point for some curves in function of the temperature are depicted. The figure shows than at low gate-source voltage, V_{GS}, the dominating factor is the threshold voltage, V_{TH}, which decreases with the temperature on the other hand the drain current increases while at higher V_{GS} the mobility decreases with temperature and so the current will be lower. The mutual cancellation of this two different effects occurs at one point called Zero Temperature Coefficient (ZTC) point. The analytical expression of the drain current saturation is:

$$I_D = \frac{C_{ox}}{2}\frac{W}{L}\mu_n \left(V_{GS} - V_{TH}\right)^2$$

and the gate-source voltage V_{GS} is

$$V_{GS} = V_{ZTC} = V_{TH}(T_o) - |k| T_o$$

The temperature independence can be observed

$$I_D = I_{ZTC} = \frac{C_{ox}}{2}\frac{W}{L}\mu_n(T_o)(|k| T_o)^2$$

By choosing a correct V_{GS} the cancellation of the threshold voltage can be possible, so the circuit will work in the ZTC point. In this point (V_{ZTC}, I_{ZTC}) exists, the curves obtained at different temperature have a common intercept point, Fig (1.1), in this point the temperature coefficient of the threshold voltage can be expressed as:

$$|k| = \frac{V_{TH}(T_o) - V_{ZTC}}{T_o}$$

There is a mutual accomplishment between the threshold voltage and the mobility, since of the doping concentration increases above $10^{17} cm^3$ the mobility is proportional to $T^{-1.2}$ while with a doping equals to $10^{12} cm^3$ the mobility is proportional to $T^{-2.42}$[1].

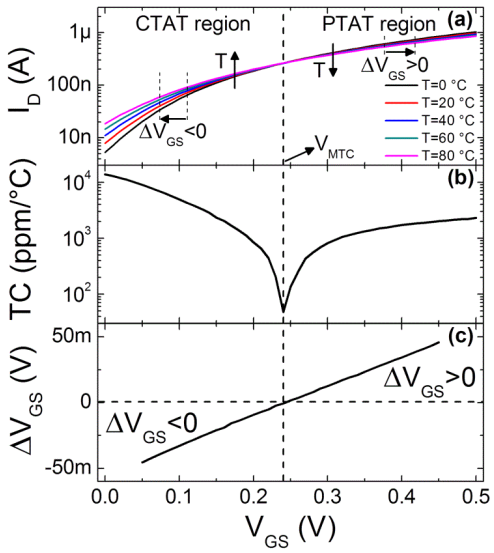


Fig. 1.1: Transconductance characteristics of a NMOS transistor [2]

The temperature dependence of the MOSFET drain current, I_D, shows two opposite trends Fig (1.1)(a): at low gate-source voltage, I_D increases with the temperature since the threshold voltage V_{TH} decreases and the thermal voltage V_T increases; on the other hand, at high gate-source voltage, I_D decreases with the temperature, due to the decrease of the charge carrier mobility. The transition point between these two operating regions is usually referred as ZTC point.

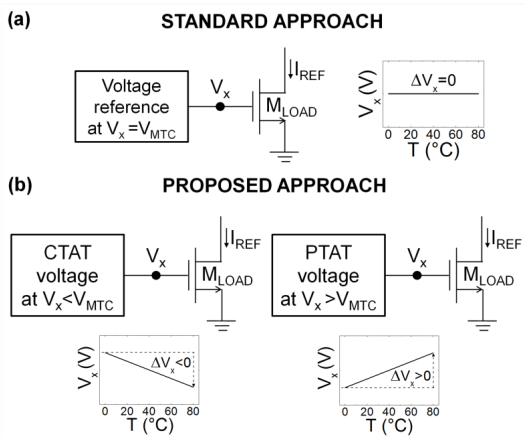


Fig. 1.2: Conceptual diagram of a current reference based on (a) the standard approach and (b) the approach proposed in [2]

Typically, this standard is used to implement the temperature compensation in a current reference depends on the use of a voltage reference with an output voltage equal to the V_{MTC} and adding an output MOSFET that converts the V_{MTC} at the gate terminal into the reference current (I_{REF}) at the drain terminal, as shown in Fig (1.2)(a). However, there are some evident drawbacks related to this design approach, like the need of a very precise bias voltage for the load transistor, which typically requires the use of an amplifier stage with a very precise and process-voltage-temperature insensitive gain added to a basic voltage reference, so it is possible having to large penalties in terms of power consumption and area occupancy, and the high bias voltage typically required to get the MTC point, which translates into high reference currents, high power consumption, and high minimum supply voltage (V_{DDmin}).

1.1.2 The body effect

In a common circuit the source terminal is tied to the substrate (body) terminal B, which results in the *pn* junction between the substrate and the induced channel having a constant zero bias, in this case the body do not play any role in circuit operation and it is neglected, but in integrated circuits, the substrate is common to many MOS transistors. In order to have the zero bias condition for all the substrate-to-channel junctions, the body is connected to the most negative power supply. The reverse-bias voltage between source and body, V_{SB}, will have an effect on device operation. If the body is more negative as the source voltage, the reverse-bias voltage will widen the depletion region. This in turn reduces the channel depth and to return the channel to its former state, the gate-to-source voltage, V_{GS}, has to be increased.

The effect of the body-bias on the channel can be represented as a change in the threshold voltage , V_{TH}, so an increase in the reverse substrate bias voltage V_{SB} results in an increase in V_{TH} according to

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \tag{1.1}$$

where V_{TH0} is the threshold voltage for $V_{SB} = 0$; ϕ_f is a physical parameter $\left(2\phi_f \approx 0.6V\right)$; γ is a fabrication-process parameter given by

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{OX}}$$

where q is the electron charge, N_A is the doping concentration of p-type substrate and ε_S is the permitivity of silicon, γ has a dimension $\sqrt{V}$ and is commonly $0.4\mathrm{V}^{1/2}$. Equation (1.1) shows that an increase in V_{SB} yields an increase in V_{TH}, which in turn results in an increase in drain current I_D even though the V_{GS} is kept constant. In conclusion, the body voltage controls the drain current I_D, so the body plays as another gate for the MOSFET, this phenomena is known as the body effect, and the

parameter γ is known as the body-effect parameter [3].

Small-signal model for the Body Effect

The body plays as a second gate or a *backgate* for the MOSFET, so the V_{BS} yields an increase to the drain-current, this increase in function of the transconductance can be $g_{mb}V_{BS}$, where g_{mb} is the body transconductance given by

$$g_{mb} = \frac{\partial i_D}{\partial V_{BS}}$$

where V_{GS} and V_{DS} are constant, equation (1.1) shows the dependence of V_{TH} on V_{BS} so the I_D depends on V_{BS} and the body transconductance is given by

$$g_{mb} = \chi g_m$$

where

$$\chi \approx \frac{\partial V_{TH}}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_t + V_{SB}}}$$

χ has commonly a value from 0.1 to 0.3. Fig (1.3) shows the nMOSFET model with the controlled source $g_{mb}V_{BS}$ that models the body effect [3].

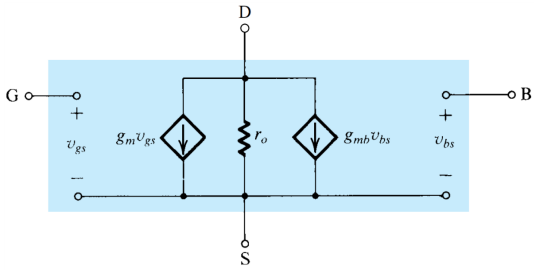


Fig. 1.3: Small-signal equivalent-circuit model of nMOSFET [3]

1.1.3 Sub-thershold Region

Low-voltage operation requires a trade between the threshold voltage and the off currents of the devices, a higher off current more power consumption in idle mode. In addition to off current control, the circuit has to control independently certain sections in order to turn off sections in idle mode. One method to reduce the off currents is designing the transistor with a low threshold voltage which limits the power to use in the circuit in the active mode, studies has shown that the low power consumption in standby mode can be reached by including a back-gate-bias threshold-voltage control for the idle circuits. Another solution is to use variable threshold devices, where the technique of tying the gate potential to the substrate potential to create a lateral bipolar action in the devices is used, in this solution the threshold voltage is reduced when the circuit is turned on. These improvements can be reached only if the circuit is fabricated on an SOI substrate because the channel region can be contacted and the individual transistors are isolated from the rest of device [4].

In order to achieve such low-power, the circuits should operate in the subthreshold region, where the gate-source voltage of MOSFET is lower than the threshold voltage [5].

The bias current in weak inversion for a nMOSFET is given by:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{1.2}$$

$$I_0 = \mu C_{OX} (\eta - 1) V_T^2$$

where μ is the carrier mobility, C_{OX} is the gate oxide capacitance, $V_T (= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and

$\eta(\approx 1.5)$ is the subthreshold slope factor.

Equation (1.2) shows that subthershold current has an exponential trend in function of the gate-source voltage. Fig (1.4) shows how changes the value of the current at different temperatures and gate-source voltage, than means the subthershold current is sensitive to temperature and process variation.

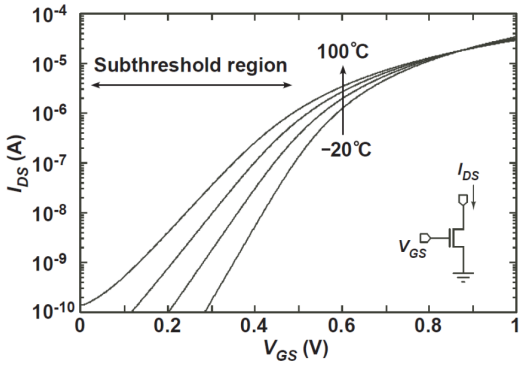


Fig. 1.4: Subthreshold Current curves in function of gate-source voltage at different temperatures[6]

The temperature dependence of the threshold voltage (V_{TH}) and the mobility (μ) of MOSFET is given by:

$$V_{TH} = V_{TH0} - \kappa T \tag{1.3}$$

The temperature coefficient (TC) is given by

$$TC = \frac{2-m}{T} + \frac{\kappa - (V_{GS} - V_{TH})/T}{\eta V_T}$$

where m is the mobility temperature exponent, κ is the temperature coefficient of V_{TH}, V_{TH0} is the threshold voltage at 0 K [7]. Equation (1.3) shows that the threshold voltage depends directly on the temperature variation around the transistor. Otherwise, process variation could be intra-die variation and inter-die variation, the first happens within-die (WID) and the second is the difference between die to die (D2D) [8]. The WID is caused by mismatches between parameters within a chip and af-

fects the accuracy of the parameters and the D2D affects the absolute accuracy of transistor between chips.[6]

The process dependence of the subthreshold current is given by:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}}\left(\frac{\partial I_{DS}}{\partial \mu}\Delta\mu + \frac{\partial I_{DS}}{\partial V_{TH}}\Delta V_{TH}\right) = \frac{\Delta\mu}{\mu} - \frac{\Delta V_{TH}}{\eta V_T} \tag{1.4}$$

$\Delta\mu$ is generally smaller than ΔV_{TH}, so the current depends mainly on ΔV_{TH}. Equation (1.4) shows that a little variation in the threshold voltage will yield a current variation so the process sensitivity plays a main role at the moment to design a transistor in the weak inversion region. Additionally, the process sensitivity could be reduced by using large-sized transistors and analog layout techniques, and the temperature dependence can be used to compensate for temperature variation of a constant voltage [6].

1.1.4 Self-Cascode connection

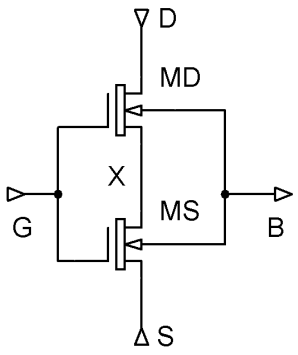


Fig. 1.5: Self-cascode connection

In some cases, the current needed for a circuit should be greater but the technology of the transistor does not allow to increase it. Fig (1.5) shows the implementation of this technique with two transistors. In practical cases, the ratio W/L of the transistor MD should be greater than the ratio in MS, i.e. m>1, to ensure the saturation regime in both. This structure can be treated as a complete transistor, which has a much

larger channel length thus a lower output conductance $(L_T = L_{MD} + L_{MS})$. The main advantages that this connection present is: it provides higher output impedance and it reduces the effect of Miller capacitance on the input of the amplifier [9]. The structure is driven by the same input signal. If MD and MS have similar W/L ratio, MS will work in the linear region while MD will operate in the saturation region, so the composite transistor will work like a common-source stage but with a higher voltage gain. If MD has a much higher aspect ratio than MS, then with an appropriate bias of voltage and current, MS is placed in strong inversion region while MD operates in the weak inversion region, so that the new gain will be increased too much.

If the MS threshold voltage, $V_{TH,MS}$, is greater than MD ,$V_{TH,MD}$, and the width of MD is equal to the MS transistor, MS will work in linear region and MD will work in saturation region. The above assumptions and a constant current along the composite transistor, all the transistors connected in series and tied to the same gate voltage, allow to reduce the channel resistance and the drain-source voltage in MD, $V_{DS,MD}$, and an increasing in the drain-source voltage in MS, $V_{DS,MS}$, so MD and MS can be operated in saturation regime [10]. In order to guarantee the self-cascode structure in saturation regime, the next condition will be reached when

$$V_{DS(sat),MD} \geq V_{TH,MS} - V_{TH,MD} \text{ where } V_{TH,MS} > V_{TH,D} \tag{1.5}$$

The drain-source voltage in MS is small so the saturation voltage of the composite transistor is similar for a normal transistor with similar dimensions, so a self-cascode can be used in a low voltage operation.

The self-cascode offers high output impedance, similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor. On the other hand, the advantages could be the limited input common mode range, small output swing and relatively high power supply requirements. Since this struc-

ture will be used to reduce the linear sensitivity in the implementation chapter, the small-signal analysis is necessary, Fig 1.6a represent the small-signal equivalent circuit. If the body and source voltage are equal to zero, $V_B = V_S = 0$, and the voltage supply input, drain node D, is grounded through a supply source, i.e current supply that provides Id, the circuit can be reduced as shown in Fig 1.6b.

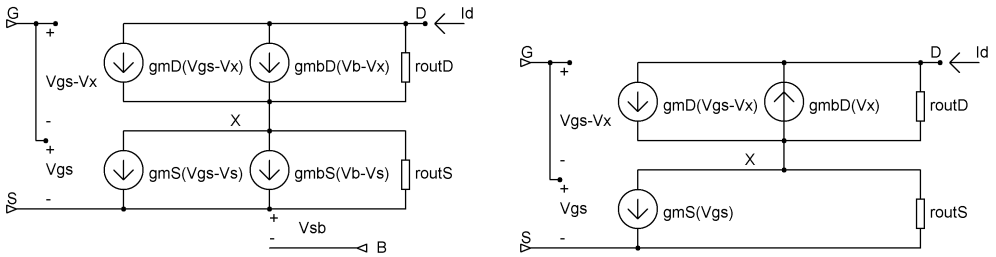


Fig. 1.6: Small-signal circuit equivalent and Small-signal reduced circuit

The drain current in MD and MS transistors is defined by

$$i_D = gm_{MD}\left(V_{GS} - V_{XS}\right) + \frac{0 - V_{XS}}{r_{out,MD}} - gmb_{MD}V_{XS} \tag{1.6}$$

$$i_D = gm_{MS}V_{GS} + \frac{V_{XS}}{r_{out,MS}} \tag{1.7}$$

where V_{GS} is the gate-source voltage for the composite transistor, V_{XS} the intermediate-node to source voltage, $r_{out,MS}$ and $r_{out,MD}$ are the on-resistance for the transistor connected in source S node and drain D node, respectively, gm_{MD} and gm_{MS} are the transconductance for MD and MS respectively and gmb_{MD} is the transconductance due to the body biasing. Equations (1.6) and (1.7) allows to have the transconductance of the composite transistor by

$$gm_{SC} = \frac{i_D}{V_{GS}}$$

Using (1.6) and (1.7) the above relation is reduced from

$$\frac{i_D}{V_{GS}} = \frac{gm_{MD} + gm_{MD}gm_{MS}r_{out,MS} + gm_{MS}\dfrac{r_{out,MS}}{r_{out,MD}} + gmb_{MD}gm_{MS}r_{out,MS}}{1 + gm_{MD}r_{out,MS} + \dfrac{r_{out,MS}}{r_{out,MD}} + gmb_{MD}r_{out,MS}}$$

$$\frac{i_D}{V_{GS}} = \frac{(gm_{MD} + gmb_{MD})\,gm_{MS} + \dfrac{gm_{MD}}{r_{out,MS}} + \dfrac{gm_{MS}}{r_{out,MD}}}{gm_{MD} + gmb_{MD} + \dfrac{1}{r_{out,MS}} + \dfrac{1}{r_{out,MD}}}$$

Since $r_{out,MS}$ and $r_{out,MD}$ are so large, the relation will be reduced and the composite transconductance will be driven by the transconductance of the transistor connected to the source of the composite transistor.

$$gm_{SC} = \frac{i_D}{V_{GS}} \approx gm_{MS} \tag{1.8}$$

Self-Cascode for n-transistors

If the number of transistors to create a composite transistor is greater than two, a similar analysis in small-signal can be done but the gm_{SC} will be approximately the transconductance of the bottom transistor in the cascode connection. In addition to the equivalent composite-transconductance, all the transistors in series connection must have the same dimensions at a specific technology, this helps to reduce variation in the process and the power needed to bias the composite transistor, with the below assumptions the composite-transconductance can be given by the relation:

$$\frac{i_D}{V_{GS}} = \frac{\dfrac{gm_2}{r_1} + gm_2gm_1 + gm_1gmb_2 + \dfrac{gm_1}{r_2} + \dfrac{gm_3}{(r_2r_1)\,(gm_3 + gmb_3 + 1/r_3)}}{\dfrac{1}{r_1} + gm_2 + gmb_2 + \dfrac{1}{r_2} + \dfrac{1}{(r_2r_1)\,(gm_3 + gmb_3 + 1/r_3)}}$$

The relation can be reduced only when the assumption of the all transistors on-resistance is so large. Second, the relation for a n-number of transistors can be

described by

$$\frac{i_D}{V_{GS}} \approx \frac{gm_M \prod (gm_N + gmb_N)}{\prod (gm_N + gmb_N)} \approx gm_M$$

where M index shows the transistor placed in the bottom of the cascode-connection and N index the number of transistors used to create the composite-transistor and counted from 2 to the total of transistor number. This composite transconductance can be modeled by the geometrical parameters on the transistor such as width and length.

$$\frac{\partial I_{DS,MS}}{\partial V_{GS}} = \frac{\mu_n C_{ox} \frac{W}{L} \frac{(V_{GS}-V_{TH})^2}{2}}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{TH}) = gm_{SC}$$

$$\frac{1}{gm_S} = R_{M1} = \frac{1}{\mu_n C_{ox} (V_{GS1} - V_{TH}) (W/L)_1}$$

If the transistors are the same type, the $\mu_n C_{ox} (V_{GS1} - V_{TH})$ can be omitted and the gain is proportional to W/L ratio, the equivalent ratio is given by:

$$\left(\frac{W}{L}\right)_{EQ} = \frac{\prod_{N=1}^{N} \left(\frac{W}{L}\right)_N}{\sum_{N=1}^{N} \left(\frac{W}{L}\right)_N}$$

The total channel length can be increased, $L_T = L_1 + L_2 + \cdots + L_N$, so the current used to bias the composite transistor will increase slowly in comparison to a simple transistor due to the channel length increasing, this effect can be used in low power applications where the linear or process sensitivity plays a main role to reduce the figures of merit.

1.2 Figures of Merit

The performance of the voltage reference designs has to be measured with normalized metrics, some of these metrics are explained below.

1.2.1 Temperature Coefficient

The variation in the output voltage from the voltage reference is defined by its temperature coefficient, which has units of parts per-million per degree Celsius (ppm/°C). The voltage is given by

$$V_{REF}(T) = V_{REF}I_{25°C}\left(1 + TC_1\left(\frac{T}{25°\text{C}}\right) + TC_2\left(\frac{T}{25°\text{C}}\right)^2 + \dots\right)$$

TC_1 is the first order temperature dependence, TC_2 is the second and so on. The TC is defined with the endpoint or box method and a specific temperature range which could be a commercial range (0 to 70 °C), a industrial range (-40 to 85 °C) and an extended range (-40 to 125 °C). The box method may underestimate the TC, if the temperature range of the application is smaller than the working range [11].

$$TC_{BOX} = \left(\frac{V_{REFMAX}I_T - V_{REFMIN}I_T}{V_{REF}I_{25°C}}\right)\left(\frac{1}{T_{MAX} - T_{MIN}}\right)10^6$$

$$TC_{ENDPOINT} = \left(\frac{V_{REF}I_{TMAX} - V_{REF}I_{TMIN}}{V_{REF}I_{25°C}}\right)\left(\frac{1}{T_{MAX} - T_{MIN}}\right)10^6$$

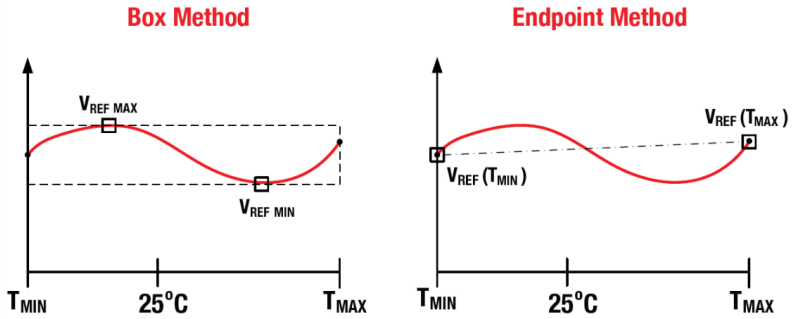


Fig. 1.7: TC by box and endpoint method [11]

In addition to the methods mentioned above, the temperature dependence in a current reference circuit in weak inversion region is measure by the current change in a specific temperature range, this parameter is given by:

$$TC = \left(\frac{I_{REF_{MAX}} - I_{REF_{MIN}}}{I_{REF_{MEAN}}}\right)\left(\frac{1}{T_{MAX} - T_{MIN}}\right) 10^6 \left[\frac{\text{ppm}}{^o\text{C}}\right] \tag{1.9}$$

where $I_{REF_{MAX}}$ and $I_{REF_{MIN}}$ are the maximum and minimum current, respectively in all the range at $(T_{MIN} - T_{MAX})$, the temperature range is bounded by T_{MAX} and T_{MIN}, in simulation case T_{MIN} is equal to 0°C, the room temperature is 25°C and T_{MAX} is 100°C.

$$I_{REF_{MEAN}} = \frac{I_{REF_{MAX}} + I_{REF_{MIN}}}{2} \tag{1.10}$$

In this thesis, the voltage supply is 1.5V, so a TC value of 20ppm/°C, represents

$$20\frac{\text{ppm}}{^\circ\text{C}} = \frac{1.5V}{10^6} = 30\frac{\mu\text{V}}{^\circ\text{C}}$$

The smaller temperature coefficient the smaller change in the reference current when there is a temperature variation.

1.2.2 Linear Sensitivity

In a voltage reference, is the variation in the reference voltage as a function of the input voltage. It allows to know the dependence as a function of the input supply.

It is suitable a 10% or less in its value, in order to decrease significantly to the total error.

Its value is given by

$$\text{LS} = \frac{I_{REF_{MAX}} - I_{REF_{MIN}}}{I_{REF_{MEAN}}\left(V_{DD_{MAX}} - V_{DD_{MIN}}\right)} \left[\frac{\%}{\text{V}}\right] \tag{1.11}$$

where $I_{REF_{MAX}}$ is the current given at $V_{DD_{MAX}}$ and $I_{REF_{MIN}}$ is the current given at $V_{DD_{MIN}}$, the supply voltage is bounded by $[V_{DD_{MAX}} : V_{DD_{MIN}}]$, where $V_{DD_{MAX}}$ is 1.5V and $V_{DD_{MIN}}$ is the minimum voltage where the curve present a high change in its linearity. $I_{REF_{MEAN}}$ is given by the average in the range bounced by $[V_{DD_{MAX}} : V_{DD_{MIN}}]$.

The smaller Liner Sensitivity the better independence of supply voltage.

1.2.3 Process Sensitivity

The process variations can be measured with the current tendency, lower percentage better independence of the process. This relation is given by:

$$\text{PS} = \frac{I_{REF_{MAX}} - I_{REF_{MIN}}}{I_{REF_{MEAN}}} \times 100\,[\%] \tag{1.12}$$

where $I_{REF_{MAX}}$ and $I_{REF_{MIN}}$ are the maximum and minimum currents used to bias the load.

The low power applications need circuits with a low power consumption and a stable output either in voltage or current. Nowadays, the current or voltage reference circuits are used to achieve a pW level in power consumption, in this section, the basic designs and quality parameters are explained.

1.2.4 Minimum Voltage Supply and Reference Current

This parameter is given by the minimum supply voltage to ensure a correct operation of the circuit. Low-power applications needs a $VDD_{MIN} < 1\text{V}$. Another parameter

is the output current which is measured at room temperature, 20°C and a fixed voltage supply, the applications need a reference current as stable as possible in order to reduce the power consumption and to guarantee the security of the circuit in critic situations like high temperature or a strong variation in the power supply.

1.3 Circuit References

1.3.1 Voltage reference

The voltage reference is a circuit used to generate a stable voltage in its output, V_{REF}, where the voltage supply should not play a main role, so this circuit has a significant independence of the supply, V_{DD}, temperature and process variation. In addition, always it is achieved a $V_{REF} < V_{DD}$ and the temperature dependence could be a concern to modify the reference voltage required. If V_{REF} increases with temperature, the reference is called *proportional to absolute temperature* or PTAT but if V_{REF} decrease with increasing temperature the reference is called *complementary to absolute temperature* or CTAT [12]. Fig 1.8 shows the tendency for a CTAT and PTAT voltage reference with increasing temperature.

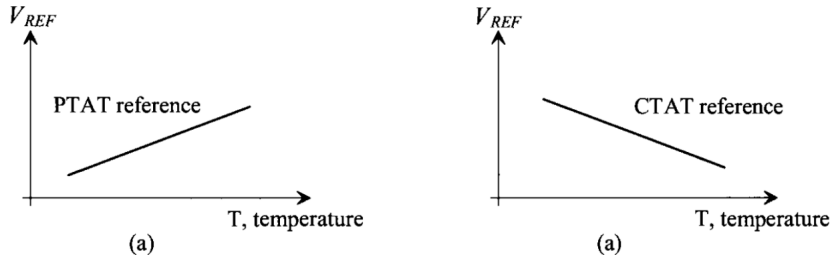


Fig. 1.8: (a) PTAT (b) CTAT V_{REF} vs *Temperature variation* [12]

Otherwise, Fig 1.9 shows the possible methods to design a voltage reference, the basic design is given by a voltage divider with two resistor where the power dissipation is the main problem because reducing consumption on the resistor must be large, larger resistor larger area. The next voltage divider between resistor and

nMOSFET has a current control by the resistor and variability control in the load by the transistor. Finally, the voltage divider between pMOSFET and nMOSFET, uses less area at the layout and a best control of the reference.

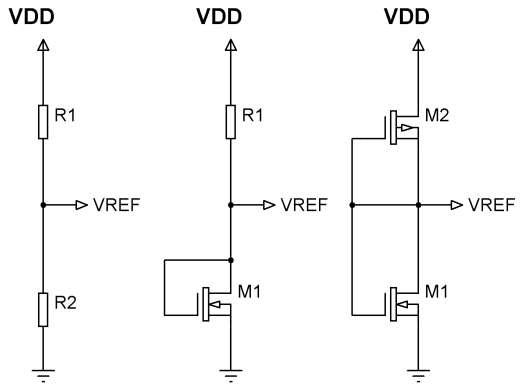


Fig. 1.9: Voltage dividers implemented from Only Resistors to Only MOSFET

The third voltage divider structure is the best option when a low power and voltage application is required, some variations are shown where the pMOSFET is changed by a nMOSFET, the driven voltage is given by the gates voltage with respect to ground. Since $I_{D3} = I_{D2}$.

$$\frac{\beta_1}{2}\left(V_{REF} - V_{THN}\right)^2 = \frac{\beta_2}{2}\left(VDD - V_{REF} - V_{THP}\right)^2 \tag{1.13}$$

$$V_{REF} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}} \times V_{THN}}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \tag{1.14}$$

where VDD is the supply voltage, $V_{THP/THN}$ are the threshold voltages and $\beta_{1,2}$ are the amplification coefficients.

Forcing the same current in the transistors is made with the current mirror concept, where the low-output resistance in the transistor gives a reference very sensitive to changes in *VDD,* this technique can be improved if is cascoding [12], where the current can be equal and sensitivity to *VDD* can be reduced.

The cascode structures allow to have the same bias current on a branch of the refer-

ence, and the reference current's variation with temperature is given by:

$$I_{REF}(T) = I_{REF}(T_o)(1 + TCI_{REF}(T - T_o)) \tag{1.15}$$

where TCI_{ref} is the temperature coefficient defined as:

$$TCI_{REF} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} \tag{1.16}$$

1.3.2 Voltage and current reference based on bandgap reference circuits

Figure (1.10) shows the circuits to get a bandgap voltage reference, which generate a voltage independent of the process, supply voltage and temperature. It is built with MOSFET transistor, substrate pnp bipolar transistors and resistors, their operation principle is given by the function of two circuits the voltage and current reference [6].

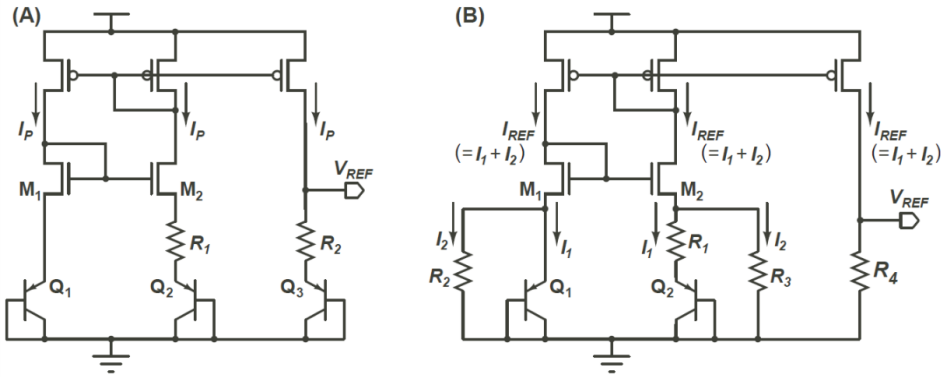


Fig. 1.10: (A) Conventional bandgap voltage reference circuit (B) Sub 1-V output bandgap voltage reference circuit [6]

Operation as voltage reference circuit

The collector current I_C of the bipolar transistor is given by

$$I_C = KI_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

where K is the transistor size, I_S the saturation current, and V_{BE} is the base-emitter voltage[12]. The operation current I_P in Fig 1.10(A) is given by Q_1 and Q_2 with different transistor sizes and the resistor R_1 as:

$$I_P = C\frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(K_2/K_1)}{R_1}$$

The current I_P is PTAT, the resistor R_2 and the transistor Q_3 accept the current through the current mirror circuit and produce the output voltage, given by:

$$V_{REF} = V_{B3} + I_p R_2 = V_{BE3} + \frac{R_2}{R_1} V_T \ln(K_2/K_1) \tag{1.17}$$

Equation 1.17 shows that V_{REF} is the sum of the base-emitter voltage and thermal voltage scaled by the resistor ratio. An output voltage V_{REF} with ZTC can be obtained by adjusting the resistor ratio. On the other hand, in Figure 1.10(B) the operation currents I_1 and I_2 are given by:

$$I_1 = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{V_T \ln(K_2/K_1)}{R_1} \quad I_2 = \frac{V_{BE1}}{R_2}$$

The resistor R_4 accepts the current $I_{REF}\,(= I_1 + I_2)$ through a current mirror and yields an output voltage which is given by:

$$V_{REF} = I_{REF} R_4 = \frac{R_4}{R_2} V_{BE1} + \frac{R_4}{R_1} V_T \ln(K_2/K_1)$$

To achieve the independent of temperature, the resistor ratio should be adjusted.

Operation as current reference circuit

The circuit in Figure 1.10(B) can be used as a current reference generator. The relation $R = R_0(1+\alpha T)$ gives the temperature dependence of them, where R_0 is the resistance value at absolute zero temperature, and α is the temperature coefficient of the resistor [6]. The temperature dependence is given by $V_{BE} = V_{BE0}(1-AT)$ and $\Delta V_{BE} = BT$, where A and B are the TC of V_{BE} and ΔV_{BE}, respectively, and V_{BE0} is the base-emitter voltage at absolute zero temperature, so the reference current is given by:

$$I_{REF} = I_1 + I_2 = C\frac{\Delta V_{BE}}{R_1} + \frac{\Delta V_{BE1}}{R_2} = \frac{BT}{R_{01}(1+\alpha T)} + \frac{V_{BE0}(1-AT)}{R_{02}(1+\alpha T)}$$

$$I_{REF} = \frac{1}{R_{01}}(BT) + \frac{V_{BE01}}{R_{02}}(1-(A+\alpha)T) \tag{1.18}$$

The two terms in equation (1.18) have negative and positive temperature dependence, respectively. The current reference can be independent of temperature with adjusting of resistor values. These circuits can give a stable current and voltage but the power consumption could become a drawback at the implementation moment.

1.3.3 Voltage references based on ΔV_{GS}

The circuits showed in Figure (1.11) operate in the strong inversion region and are based on the difference between the gate-source voltages. The drain current I_{DS} in the strong inversion and saturation region can be expressed as

$$I_{DS} = \frac{K\beta}{2}(V_{GS} - V_{TH})^2$$

where $K = W/L$ ratio, and $\beta\,(=\mu C_{OX})$ is the current gain factor.

The circuit (A) shows two transistors with different threshold voltage, where the reference voltage is given by

$$V_{REF} = V_{GS1} - V_{GS2} = (V_{TH01} - \kappa T) - (V_{TH02} - \kappa T) + \sqrt{\frac{2I_B}{\beta}} \left(\frac{1}{\sqrt{K_1}} - \frac{1}{\sqrt{K_2}} \right)$$

$$V_{REF} \approx V_{TH01} - V_{TH02} \tag{1.19}$$

I_B is a low bias current so that the temperature dependence of β can be ignored, so the reference voltage can be obtained with the approximation showed in equation (1.19). In addition, the dependence for a multiple-threshold voltage process leads to have different κ temperature coefficients, so the circuit is dependent of the process, to control this problem the two threshold voltages should have the same value in each MOSFET.

The circuit (B) shows a voltage reference using a standard CMOS process, where V_{REF} is given by

$$V_{REF} = \left(1 + \frac{R_1}{R_2} \right) V_{GSN} - V_{GSP}$$

The dependence of the threshold voltages can be canceled adjusting the resistor ration and the transistor sizing, and the temperature dependence only can be canceled at room temperature.

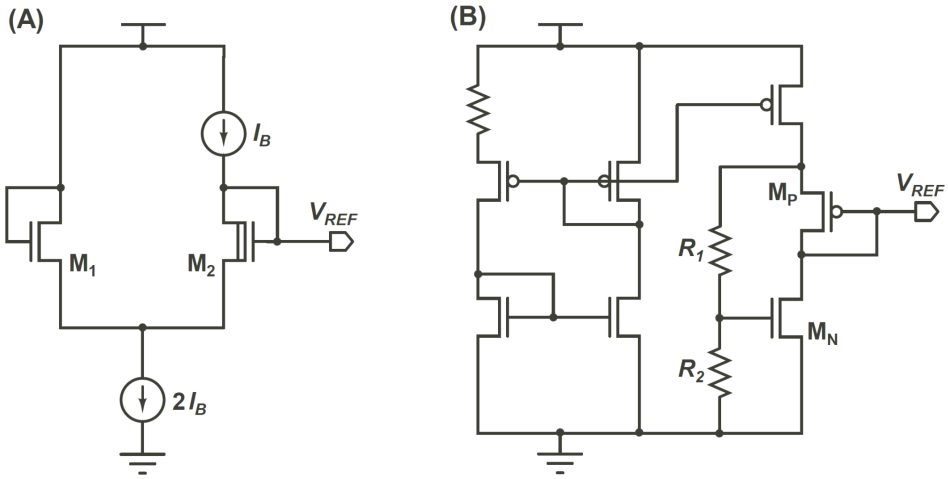


Fig. 1.11: Voltage reference circuits based on ΔV_{GS}

1.3.4 Current references based on weak and strong inversion regions

Fig (1.12) shows a circuit without resistors, where transistors M2-M11 operate in the subthreshold region, and M1 and M12 operate in the strong inversion region. Assuming that the body effects of M2 - M10 are neglected, the output current I_{REF} is given by

$$I_{REF} = \frac{\beta}{2}\eta^2 V_T^2 \ln^2\left(120\frac{K_{11}K_9K_7K_5K_3}{K_{10}K_8K_6K_4K_2}\right)\left(\frac{K_1K_{12}}{K_{12}-K_1}\right)$$

The TC of the reference current is given by

$$TC = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} = \frac{2-m}{T}$$

In a standard process the mobility temperature is $m(=1.5)$, so the output current has positive temperature dependence. The power dissipation in this circuit is large for use in sub-microwatt operation, the drawback is the sizing, a careful adjusting must be done to improve the circuit performance.

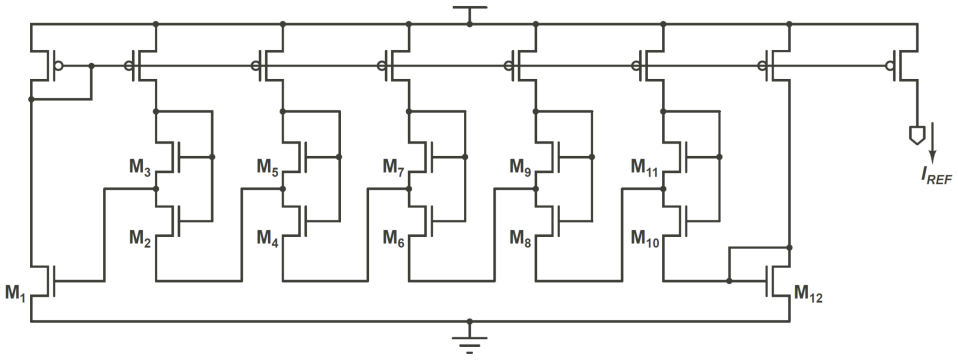


Fig. 1.12: Current reference without resistors

1.3.5 Current reference based on self-biasing technique

A PTAT current generator is shown in Fig 1.13-(A), where the circuit is self-biasing by a multiplier β. The large resistance needed to reduce the operation current becomes a drawback at implementation problem, so a new circuit was designed to solution this problem, Fig 1.13-(B), where M_3 operate as resistor. The V_{GS} at M_3 is generated by a diode-connected transistor M_4. M_1 and M_2 operate in the subthreshold region and M_4 operates in strong-inversion, saturation region. The drain current I_3 and I_4 in M_3 and M_4 are given by

$$I_3 = K_3\beta\left(V_{GS} - V_{TH}\right)V_{DS3}, \quad I_4 = \frac{K_4\beta}{2}\left(V_{GS} - V_{TH}\right)^2$$

The $V_{GS,M3} = V_{GS,M4}$ so the output current is given by

$$I_{REF} = K_3\beta\sqrt{\frac{2I_{REF}}{K_4\beta}}V_{DS} = \frac{2K_3^2\beta}{K_4}\eta^2 V_T^2 \ln^2\left(K_2/K_1\right)$$

The temperature coefficient of the reference current is given by

$$TC = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} = \frac{2-m}{T}$$

I_{REF} has a positive temperature dependence, so the TC will never be zero. In addition, $M_1 - M_4$ operate with the same current value (nanoamperes order), this design

needs a careful transistor sizing and transistor matching using large-sized transistors.

guaratee

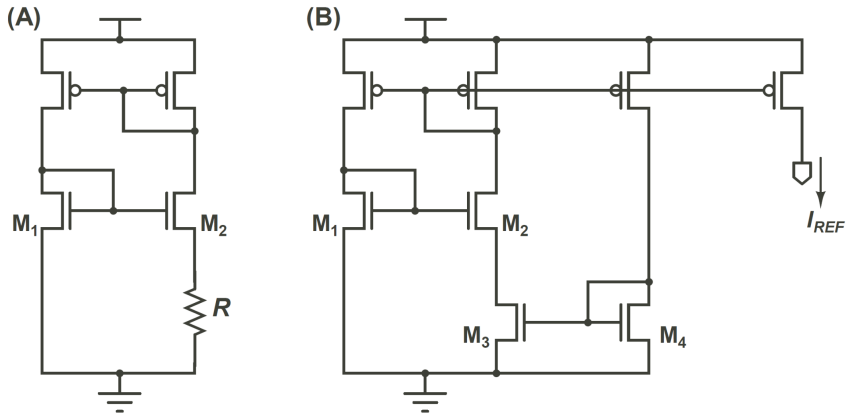


Fig. 1.13: Current reference based on self-biasing

1.3.6 Current references consisting of subthreshold MOSFETs

Fig (1.14) shows a current reference, which consists of a bias-voltage subcircuit and a current-source subcircuit. The first, is a self-biasing circuit with β multiplier, where V_B for transistor M_3 is generated by a diode-connected transistor M_4. The second, accepts the V_B and generates reference current I_{OUT} that is independent of temperature and supply voltage. All the transistor except for M_3 and M_4 operate in subthreshold region. The bias current I_B is given by the V_{GS} in M_1 and M_2, and the V_{DS} of M_3, the expression is

$$I_B = \frac{V_{DS3}}{R_{M3}} = K_3 \mu C_{OX} (V_B - V_{TH}) \eta V_T \ln (K_2/K_1) \tag{1.20}$$

and the drain current in M_4will be

$$I_B = \frac{K_4 \mu C_{OX}}{2} (V_B - V_{TH})^2 \tag{1.21}$$

Since I_B must be equal in M_3 and M_4, V_B is given by

$$V_B = V_{TH4} + \frac{2K_3}{K_4}\eta V_T \ln\left(K_2/K_1\right)$$

The output current I_{OUT} in the transistor M_5 is given by

$$I_{OUT} = K_5 I_0 \exp\left(\frac{V_B - V_P - V_{TH5}}{\eta V_T}\right)$$

V_P of M_5 operated in subthreshold region can be given by

$$V_P = V_{GS7} - V_{GS6} = \eta V_T \ln\left(2K_6/K_7\right) - \delta V_{TH76}$$

where δV_{TH76} is the difference between the threshold voltages of M_6 and M_7 with different transistor sizes. This way is possible obtain a reference current with nanoampere-order.

The temperature coefficient TC of the output current I_{OUT} is given by

$$TC = \frac{1}{I_{OUT}}\frac{dI_{OUT}}{dT} = \frac{2 - m - (\delta V_{TH0}/\eta V_T)}{T}$$

where δV_{TH0} is the difference between the threshold voltages at 0 K of transistors $M_4 - M_7$, so the condition for ZTC can be given by $2 - m - (\delta V_{TH0}/\eta V_T) = 0$, this difference is insensitive to temperature, adjusting δV_{TH0} to an appropriate value will provide a ZTC at room temperature.

The process variation of the output current I_{OUT} is given by

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \frac{1}{I_{OUT}}\left(\frac{\partial I_{OUT}}{\partial \mu}\Delta\mu + \frac{\partial I_{OUT}}{\partial \delta V_{TH}}\Delta\delta V_{TH}\right) = \frac{\Delta\mu}{\mu} + \frac{\Delta\delta V_{TH}}{\eta V_T}$$

The mobility variation μ is generally smaller than the threshold voltage variation $\Delta\delta V_{TH}$, so the I_{OUT} depends mainly of ratio $\Delta\delta V_{TH}/\eta V_T$, which is the variation of the threshold-voltage difference between transistors in a chip.

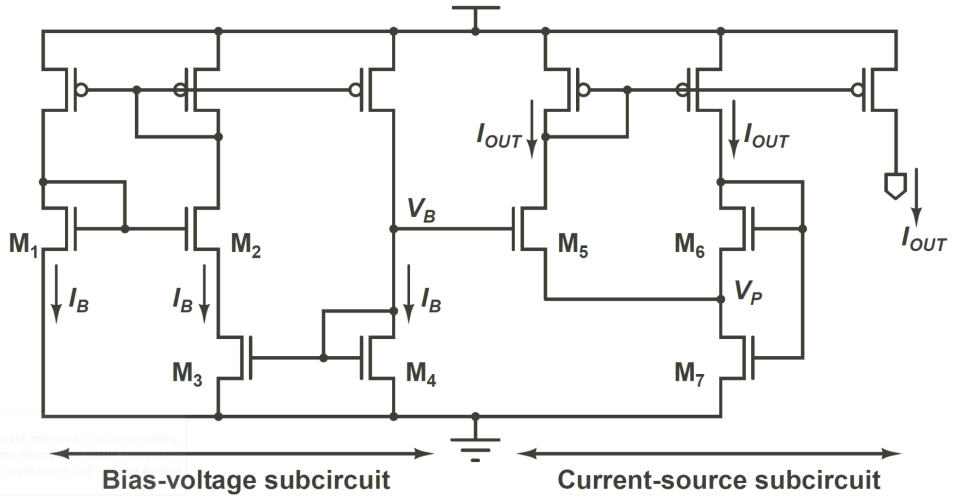


Fig. 1.14: Current reference based on subthreshold region

1.4 State of Art

An overview of the most recent researches about current references is shown in this section. First, the structure of each design is explained after that a comparison is make with the figure of merit explained below. Finally, this comparison is summarized in a table.

1.4.1 Actual solutions

A solution for the current reference is shown in Fig (1.15), this current reference is composed by a start-up circuit, a bias-voltage subcircuit, a current-source subcircuit and an offset-voltage generation subcircuit. The reference current is determined by the characteristics of the MOS resistor MR, operating in the strong inversion and deep triode regions, while all other transistors work in subthreshold region.

$$I_{REF} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DSR}$$

This expression is valid if V_{DSR} is small enough. So, if the drain-source voltage is made stable with temperature TC is low. This circuit can yield a current 95nA with

a total power consumption of 586nW, and temperature coefficient of 523 ppm/°C [13].

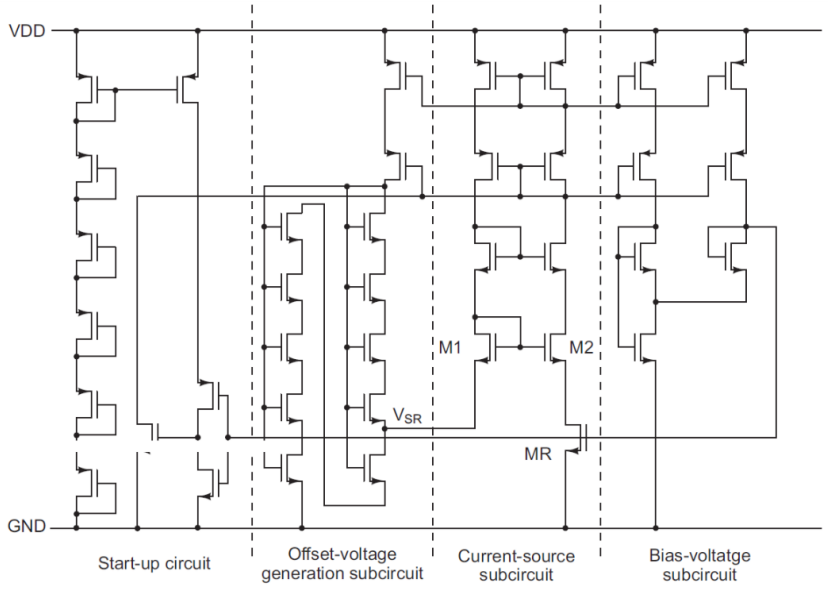


Fig. 1.15: Current Reference Circuit with Subthreshold MOS Resistor Ladder proposed in [13]

Another solution is shown in Fig (1.16), the circuit consists of bias-voltage subcircuit and a current source subcircuit. The bias-voltage subcircuit is a modified β multiplier self biasing circuit that uses a MOS resistor M_3, instead of instead of ordinary resistors. Bias voltage V_B for MOS resistor M_3 is generated by a diode-connected transistor M_4. The current-source subcircuit accepts bias voltage V_B and generates reference current I_{OUT} that is independent of temperature and supply voltage. All MOSFETs are operated in the subthreshold region, except for M_3 and M_4. A start-up circuit (not shown) is required to avoid the stable state in the zero bias condition. The circuit generates a reference current of 100nA. The temperature coefficient of the current is near 600ppm/°C. The line regulation was 0.2%/V. The power dissipation is 1μW, and the chip area is 0.015mm^2

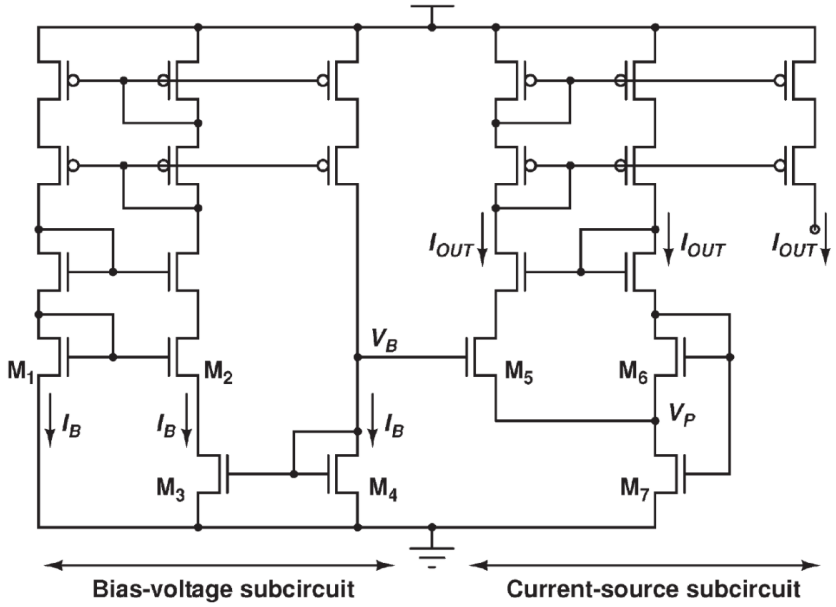


Fig. 1.16: Current Reference Circuit Consisting of Subthreshold CMOS Circuits proposed in [14]

Another solution is shown in Fig (1.17), the reference current is generated by exploiting a MOS transistor as current defining element, instead of a resistor. The two transistors M1 and M2 work in the subthreshold region while all the others transistors work in the saturation region. The sensitivity of such reference current to process variations, if matching errors are neglected, is due to carrier mobility. Mobility has a dispersion of about 5%, which is much smaller than that the tolerance of an integrated resistor, leading to a sensitivity to process variations much smaller than that of current reference circuits that use an integrated resistor as current-defining element. Even though the temperature coefficient is not temperature-independent for this circuit, it exhibits small variations around the reference temperature at which the condition of zero temperature coefficient has been enforced. The proposed circuit provides a reference current with a temperature coefficient of 44ppm/°C. The minimum supply voltage is 1.3V and the minimum supply current is 36nA. The line sensitivity is 0.569%/V. The chip area is 0.035mm^2[15].

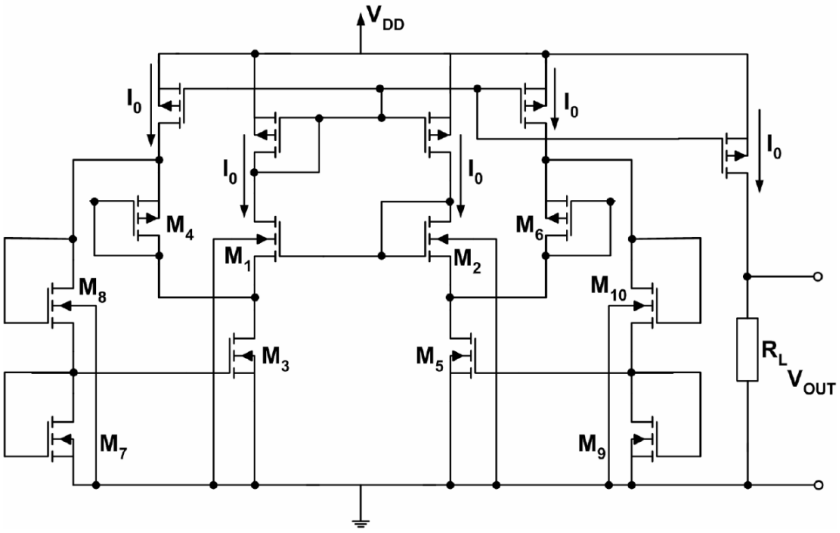


Fig. 1.17: CMOS Current Reference with Low Sensitivity to Process Variations proposed in [15]

A band gap current reference is shown in Fig (1.18) and proposed in [16]. This band gap reference has the transconductive factor was “anchored” to a diffusion resistor. It can be used instead of poly resistor and its advantages in terms of robustness to process sensitivity are due to the lower doping, large volume and mono crystalline material. The diffusion resistors were used in the implementation of a bipolar bandgap current generator, that provides the reference voltage with the lowest process sensitivity. Indeed, MOSFET-based generators introduce an additional important source of variability represented by the MOSFET threshold voltage. The threshold voltage is not "anchored" to a reference quantity while the base emitter voltage of a bipolar transistor is determined by the silicon energy gap. The circuit is based on the sum of two currents with opposite temperature coefficients. Large resistances are useful to reduce the power consumption, at the price of a large area occupation. Single-stage operational amplifiers biased with a current of few nA were used in order to reduce power consumption, and a pMOS voltage divider (whose current consumption is of only few pA, negligible with respect to the bandgap core current) was utilized in order to impose only a fraction $\frac{1}{\alpha}$ of the V_{be1} voltage on R_b. The voltage divider consists of diode-connected pMOSFETs in series, with each

well at source potential, in order not to have body effect. This solution is more complex from the architectural point of view with respect to a simple resistance divider, but leads to much lower power consumption. This solution presents a TC = 63ppm/°C, reference current 54.08nA for a power consumption of 290nW, line sensitivity of 0.21%/V and occupation area of 0.245mm^2 [16].

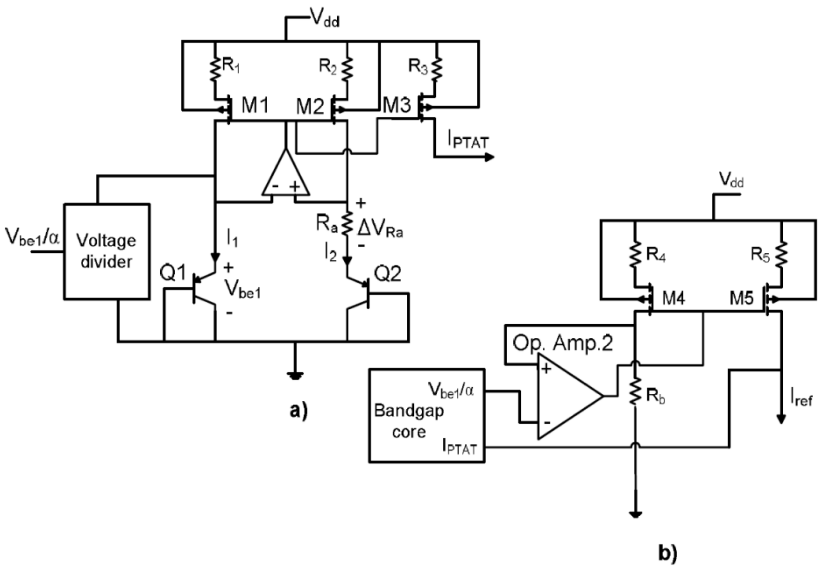


Fig. 1.18: Bandgap current reference proposed in [16] a) Bandgap core. b) Reference current circuit

Another solution is shown in Fig (1.19), the proposed design has three components: an ultra-low-power line regulator, a CTAT gate voltage generator, and a cascaded subthreshold MOSFET output stage. In addition, an optional current level selector (CLS) can be incorporated to provide a trimming range of current magnitudes. This kind of solution has a temperature coefficient of 780ppm/°C, a low reference current of 20pA likewise power consumption which equals to 23pW, line regulation of 0.58%/V and load regulation of 0.25%/V [17].

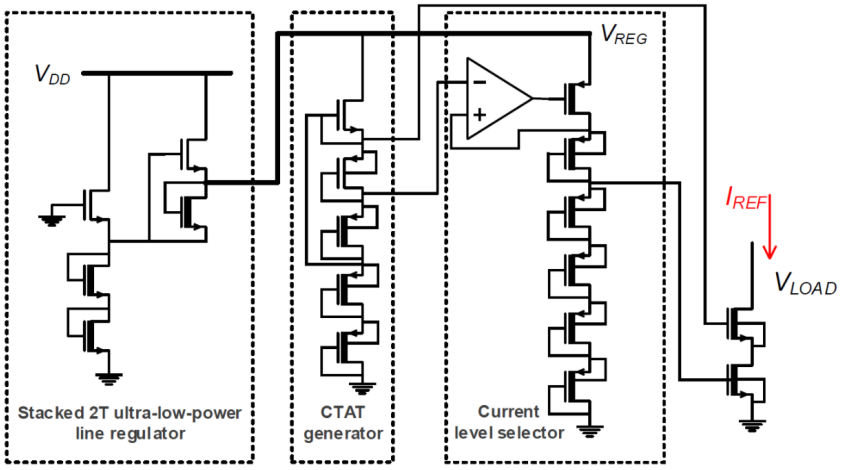


Fig. 1.19: CMOS Current Reference Without Resistance proposed in [17]

Fig (1.20) shows a current reference with three transistors and a sub-0.5 V operation. This circuit has two transistor (M_2, M_1) generates a proportional-to-absolute-temperature (PTAT) or a complementary-to-absolute-temperature (CTAT) voltage and the other as load transistor (M_3). The circuit was implemented in 0.18μm technology, this circuit exhibits figures of merit like as: a temperature coefficient (578 ppm/°C), line sensitivity (3.9%/V), power consumption (213nW), a minimum operating voltage (0.45V) and an area occupation (750μm^2) [2].

This circuit looks for working on the minimum-temperature-coefficient (MTC) point, which is the equivalent to the zero-temperature-coefficient and where the drain current I_D at a gate-to-source voltage V_{GS} does not change with the temperatures in all the temperature interval of working. The 2T voltage generator has an output voltage equal to the MTC voltage point (V_{MTC}) and the load transistor (M_3) converts the V_{MTC} at the gate terminal into the reference current at the drain terminal. In this solution the CTAT/PTAT circuit generates an output voltage (V_x) whose temperature dependence compensates to first order the one of the drain current of the output MOSFET (M_3). If $V_{GS} < V_{MTC} \approx V_x$, a CTAT block is required, while $V_{GS} > V_{MTC} \approx V_x$ a PTAT block is required, so the load transistor must be biased in the proximity of V_{MTC} to obtain a low TC values.

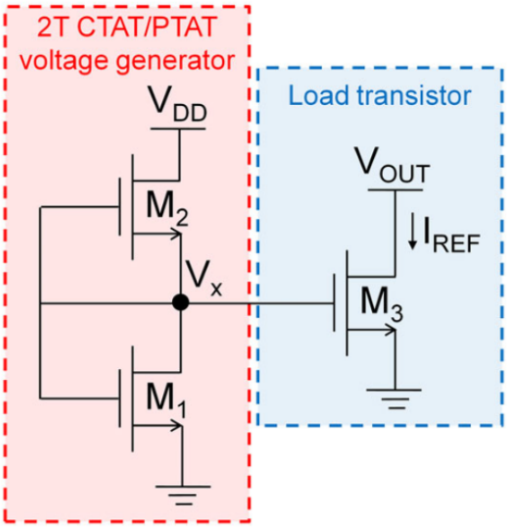


Fig. 1.20: Schematic of 3T current reference[2]

Another solution is shown in Fig (1.21) which is based in a regular voltage threshold (RVT) diode-connected NMOS (M_{N1}) and a dual-threshold voltage (DTV) current mirror composed by a high voltage threshold (HVT) PMOS (M_{P1}) and a RVT PMOS (M_{P2}). The circuit was implemented in 0.18μm technology and exhibits figures of merit like as: an output current reference (16 nA), a temperature coefficient (274 ppm/°C), line sensitivity (5.4 %/V), power consumption (20nW) and a minimum operating voltage (0.6 V).

The circuit is composed by a current mirror which generates a current equals to $I_2(T) = \alpha(T) I_1$, where α, is a ratio between I_2 and I_1, and depends on temperature. The aim of this circuit is to compensate this temperature dependence by multiplying this subthreshold current (I_1) for an exponentially decreasing function (α) provided by the current mirror. The final circuit uses two current mirrors because a single current mirror is not able to compensate the temperature dependence of M_{N1}, RVT NMOS transistors$(M_{N2,N3})$ work as current mirror too, which function is to deliver the current from the first to the second stage. This solution shows a sensitivity to the process variations, so a trimming process can be made to reduce the deviations, and present a great performance in operating voltage and area occupation factors. [18].

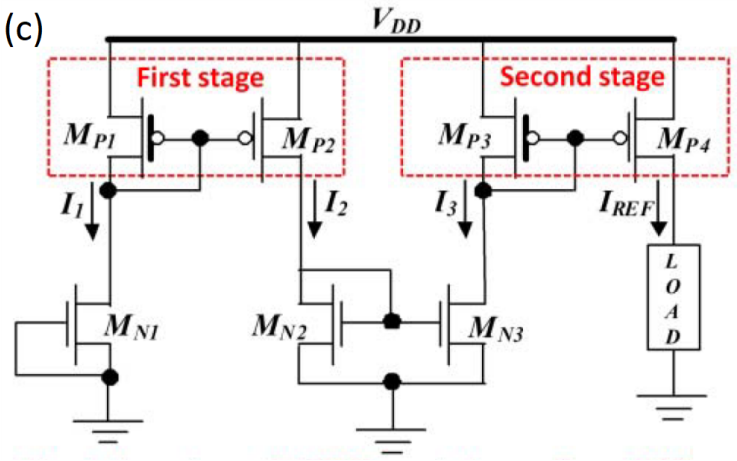


Fig. 1.21: Schematic of 7T current reference[18]

Another solution is shown in Fig (1.22), where the aim is to compensate the temperature dependence by subtracting two PTAT nature references with different slopes to get a zero temperature coefficient. The solution was implemented in 45nm CMOS technology, and presents figures of merit as: temperature coefficient (22 ppm/°C), temperature range from -40°C to 120°C, a line sensitivity (337 ppm/V) against supply variation of 0.6-18V and a power consumption of 135 uW from 1.8V supply and an area occupancy of 5184 um^2.

The α and β are the temperature coefficient for the first and second PTAT respectively, then by subtracting β times first reference current from α times the second current reference will give a perfect temperature compensation, *i.e. the zero temperature coefficient is obtained*, Since this technique depends on subtraction, any process variation which are common in PTAT circuit will cancel so a very stable reference is obtained. The PTAT current generator uses transistor in self-biased mode, the bottom transistor $(W/L)_N$ must be larger than its opposite $K_1 \times (W/L)_N$ (the transconductance will be larger due to the same current and larger size) so the difference in the gate-source voltage of bottom transistor dropped across R_{SX}. The circuit showed in Fig (1.22) has the complete implementation except start up circuits. PTAT-2 current is flowing through MN1 and six times scaled version of PTAT-1 current is flowing through MP1. MP1 and MN1 are connected in series to subtract

these two currents explained above, this difference introduce a low impedance node. A diode connected transistor MN2 is used to extract the difference current. This circuit provides attenuation again supply variation because the operational amplifier creates the same effect on PMOS transistors gate [19].

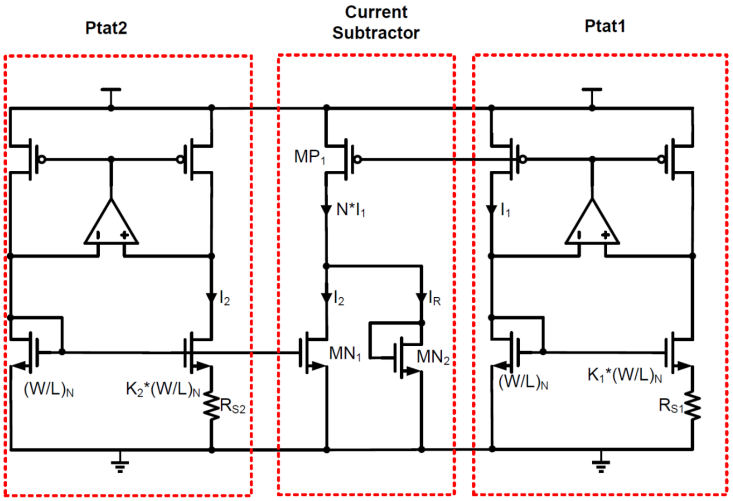


Fig. 1.22: Schematic of 28T current reference[19]

Another solution is showed in Fig (1.23), where a current reference with a self-regulated circuit is depicted, this circuit is composed by: a 2T push-pull VRG (voltage reference generator) is employed as line regulator for the other 2T push-pull VRG to obtain a temperature and supply-stabilized 4T reference voltage, then a low-power self-biased amplifier is used to bias a gate leakage array with the reference voltage. Finally, the result is a low-power, compact architecture with temperature and supply-stability circuit. The solution was implemented in 65nm CMOS technology, this circuit present result as: a power consumption 14.5 pW at a 0.5 V supply voltage, a temperature coefficient of 31 ppm/°C, a line sensitivity of 0.94%/V in 500 Monte Carlo samples [20].

The architecture employs a temperature- and supply-stabilized reference voltage driving a temperature-stabilized effective resistance, these circuit are generated via bandgap voltage reference generator (VRGs), to achieve a pW level in power consumption an ultra-low-power push-pull VRG generates a temperature-stable ref-

erence voltage while gate-leakage transistors are employed to serve as very large compact resistors. To compensate, standard-V_T (SVT) and low-V_T (LVT) PMOS transistor, which have opposite gate-leakage temperature coefficient, are employed to operate in parallel, so the temperature coefficient can be minimized.

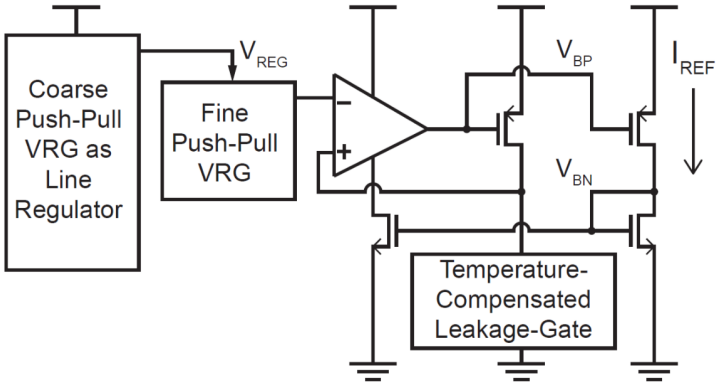


Fig. 1.23: Block diagram current reference with push pull Voltage Reference Generator[20]

Another solution shows a supply-stabilized pico-powered voltage and current reference (VCRG) as part of a relaxation oscillator, in this case the temperature- and line-stabilized reference voltage is generated via 4-transistor (4T) self-regulated structure, the output of which is used to bias a temperature-compensated gate-leakage transistor to generate a stabilized current reference. This design was implemented in 65 nm CMOS technology and was made 14 samples yield giving a reference voltage of 147.1 mV and figures of merit as: a temperature coefficient of 364 ppm/°C, line regulation of 0.21%/V and for the reference current a value of 10.2 pA and a temperature coefficient of 1077.3 ppm/°C, a line regulation of 2.4%/V, a minimum supply voltage of 0.4 V, a power consumption of 30.6 pW and an area occupancy of 4900 μm^2 [21].

The circuit, shown in Fig (1.24), is composed by 2-transistor in push-pull structure based on [22], in this case has used regular transistor instead of native devices. V_{REG} is the output of this 2T circuit and is used as supply for a second 2T circuit to produce V_{CWT} that is line-regulated [21].

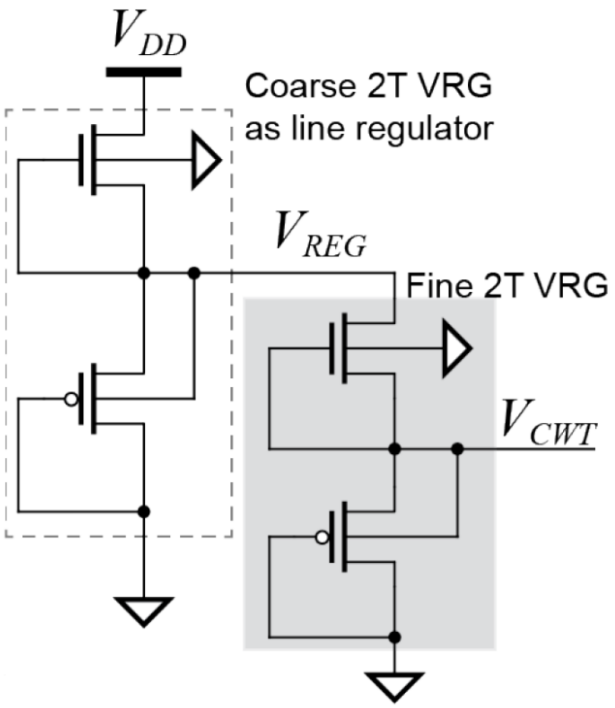


Fig. 1.24: Schematic of the self-regulated 4T voltage reference generator [21]

A near-zero power constant with temperature (CWT) current reference generator is depicted in Fig (1.25), where only five transistor in CMOS technology were used. One of these NMOS transistor works in off-state as a self-biased current source driving another NMOS transistor in the subthreshold region, a temperature stabilized voltage is created, which is then buffered by a third NMOS and applied to a gate-leakage transistor (fourth). The fifth transistor allows to improve the line regulation, which works in off-state, constructing a five-transistor (5T) I_{REF} generator. The results for this work were measured in 13 samples fabricated in 65 nm CMOS technology were the figures of merit reveled values as: temperature coefficient 469.3 ppm/°C from -20 to 60 °C at 0.4 V in supply voltage. A range from 0.4 to 1.2 V was used to get a line regulation of 2.5%/V, a power consumption of 3.4 pW at 20°C and area occupancy of 0.008 mm^2[23].

The circuit was implemented with three regular NMOS transistor for reference voltage generation and buffering, one regular NMOS for line regulation, and one gate-leakage transistor acting as a large resistor. First, a CWT reference voltage, V_{CWT},

is created by a stacking a low-threshold voltage (LVT) NMOS transistor, M_1, with its gate tied to its source, so operating as a self-biased current source, on top of a second NMOS transistor, M_2. This improvement is in contrast to the push-pull VRG in Fig 1.25(a) [21], where an off-state NMOS is used on a diode-connected PMOS. When the circuit works in the saturated subthreshold region, V_{CWT} can be derived following the same procedure as in [21]. The generation of a proper V_{CWT} requires a different type of NMOS for M_2 than M_1, a high threshold voltage (HVT) transistor is used for M_2 with negligible gate-leakage than a regular-threshold voltage transistor of the same size considering that the M_2 gate is tied in parallel to the gate-leakage transistor as shown in Fig 1.25(b). M_3 serves as voltage buffer so a CWT reference current, I_{REF}, by biasing the gate leakage transistor with V_{CWT} without the power overhead of the op-amp used in [21]. M_3 is a HVT transistor to avoid any disturbance to I_2 otherwise introduced by the leakage through M_3 gate. Finally, M_{REG} is a self-regulation transistor and is used to improve the line regulation, this circuit presents a low operating DC current on pA level so the flicker noise is reduced [23].

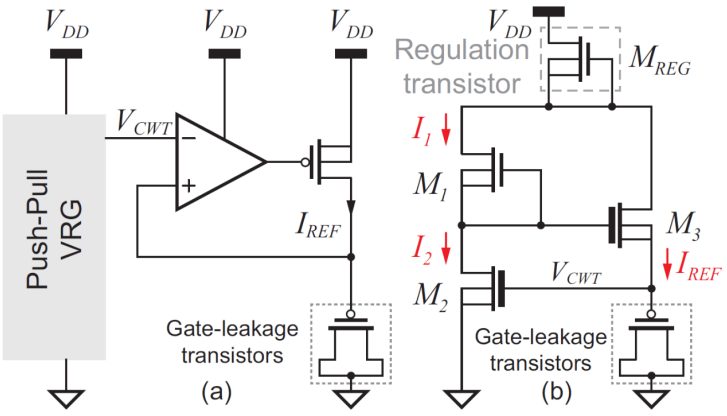


Fig. 1.25: (a) Simplified block diagram of prior art[21](b) Simplified schematic of the I_{REF} generator[23]

Another solution with a circuit self-biased current source (SBCS) is showed in Fig (1.26), where an advanced compact MOSFET (ACM) model and the concept of

inversion level are used. The solution was implemented in 1.5μm CMOS technology, and presents figures of merit in the best case as: minimum supply voltage 1.1 V, power consumption at 1.1 V of 1.5 nW, a line sensitivity between V_{ref} and V_{DD} of 0.9%/V, sensitivity between V_{ref} and T of 0.32%/°C, sensitivity between I_{ref} and V_{DD} of 4.7%/V and a sensitivity between I_{ref} and T of +0.047%/°C.

The core of this circuit is the self-cascode MOSFET, *i.e, SCM blocks in figure,* whose V-I characteristic is very appropriate for building low-voltage analog blocks such current references. In the circuit V_{S9} can be either zero or $V_{X(WJ)}$, this approach allows to replace the resistor given by a SCM block in moderate inversion to achieve the requirements of low voltages. When M_8 and M_9 are biased in weak inversion there is a PTAT voltage shift (KJ>1) between the two MOS devices. If the switch is connected to ground, the PTAT voltage is given by $V_{ref} = V_{S9} + \phi_t \ln(JK)$, ($J = S_7/S_9$ and ϕ_t is the thermal voltage) with $V_{S9} = 0$. This topology is stable for KJ>1 and for KJ>10 is very accurate. When the switch between $M_3 - M_4$ is connected, then V_{S9} is given by $V_{S9} = \phi_t \ln\left[1 + (1+J)\frac{S_4}{S_3}\right]$, this approach allows to have results when there is a symmetry (for K=J=1) and matching structure [24].

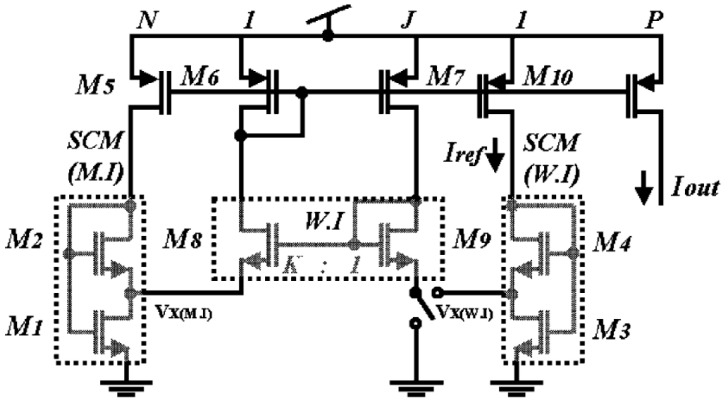


Fig. 1.26: Self-Biased current source (SBCS) [24]

In addition to the current reference circuits, a voltage reference study is shown in [22] and is depicted in Fig (1.27), this circuit eliminates the use of amplifiers and saturated MOSFETs so the scalability is improved and the output insensitivity to

temperature and supply voltage are maintained. The 2T voltage reference showed in the figure, where two different devices types are used, M1 is a native device and M2 is a thick oxide device. The output voltage V_{ref} is modeled by the drain current equation in the subthreshold region. This solution was implemented in three technologies 65nm, 0.13μm and 0.18μm, and achieves a great performance with figures of merit as: a temperature coefficient of 16.9 ppm/°C, a line sensitivity of 0.033%/V, a power consumption of 2.22 pW, a area occupancy of 1350 μm^2 and a minimum power supply of 0.5V. At $V_{dd} = 3$ V and 80°C, it consumes 243 pW, giving a factor 2 of magnitude power savings over existing nanopower voltage reference at comparable voltage and temperature points. This circuit does not need a start-up issues, the design uses subthreshold-biased devices with distinct V_{th} levels. A single temperature point digital trimming is allowed for this circuit, where an improvement of temperature coefficient and output voltage is possible. The portability of this design allows to implement with different CMOS technologies and a 2-3 order of magnitude improvement in power consumption to prior the basic voltage reference designs.

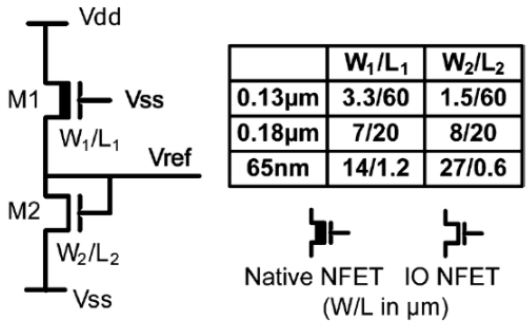


Fig. 1.27: Voltage reference with two transistors[22]

1.4.2 Resume

The solutions resume for the current references that were explained above, are shown in Table (1.1), the first column, study [2], shows the results that will be taken as a reference to improve the actual work, because this design has a small transis-

tor number and uses the voltage reference methodology viewed in [22], so the area usage is smaller than the other cases. On the other hand, figure of merit like line and process sensitivity show a small value, but the temperature coefficient is greater than the other cases. The results show a trade-off between the figures of merits, it is not possible increase or decrease a parameter without affect the performance of another, this consideration will be always in mind at the design moment.

Reference	**[15]**	**[14]**	**[13]**	**[16]**	**[17]**
Technology, μm	0.35	0.35	0.35	0.18	0.18
I_{REF}, nA	9.14	96	94.9	54.08	0.02
T range, °C	0 to 80	0 to 80	-20 to 100	0 to 80	-40 to 80
TC, ppm/°C	44	520	523	63	780
Power, nW	334	1000	586	54	0.023
V_{MIN}, V	1.5	1.8	1.8	0.8	1.2
Line sensitivity, %/V	6.5	0.2	1	0.21	0.58
Process sensitivity, σ/μ	–	–	–	1.4	–
# Samples	–	–	–	–	–
Die area, μm^2	35k	15k	55k	245k	452k
N° of elements	16T	23T	38T	–	18T

Reference	**[2]**	**[18]**	**[19]**	**[20]**	**[21]**	**[23]**
Technology, μm	0.18	0.18	0.45	0.65	0.65	0.65
I_{REF}, nA	338	15.8	30000	0.005	0.010	0.0012
T range, °C	0 to 80	0 to 80	-40 to 125	0 to 100	-40 to 120	-20 to 60
TC, ppm/°C	578	274	22	31	1037	469.3
Power, nW	213	17.4	135000	0.0145	0.030	0.0034
V_{MIN}, V	0.45	0.6	0.6	0.5	0.4	0.4
Line sensitivity, %/V	3.9	5.4	337	0.94	2.4	2.5
Process sensitivity, σ/μ	2.7%	–	0.1	–	–	–
# Samples	45	–	200	–	13	13
Die area, μm^2	750	130000	5184	176	4900	8000
N° of elements	3T	7T	28T	–	4T	5T

Table 1.1: Comparison Previous Current Reference Designs

Chapter 2

Experimental Details

A brief explanation about the Cadence®Virtuoso interface is showed, this software uses different technologies to simulate electronic circuits before the construction of them, in this work the technology of 180nm from TSMC was used. In order to implement the circuits of current reference different transistors with different oxide thickness were used.

2.1 Cadence®Virtuoso Interface

2.1.1 Principal Views

Fig (2.1) shows the schematic view from the Cadence software Virtuoso, where the different schematics were implemented, the 180nm library from TSMC was used to test the different circuits, these will be explained in the next chapter. The interface allows to introduce transistors, sources, labels, and instance a particular design inside one block for an easy manage in difficult and large circuits. Fig 2.1 shows the implementation of the 3T current reference studied in [2], in this case a *nmosmvt2v* transistors were used, this figure allow illustrate the main view of the schematic interface in Virtuoso, the geometric parameter can be set with values or variables in order to simulate after a parametric test.

On the other hand, Fig (2.2) shows the simulation interface from Virtuoso, where the circuits implemented in the schematic were tested. This interface allows to do some different simulation types, in this work the simulation interface ADEXL was used, since the parametric simulation is easier in this kind of interface. This interface allows to introduce the sizing parameters like the MOSFET width and length, the power supply, the temperature range and mainly the figure of merit equations to compare the designs of this work with the previous showed in state-of-art.

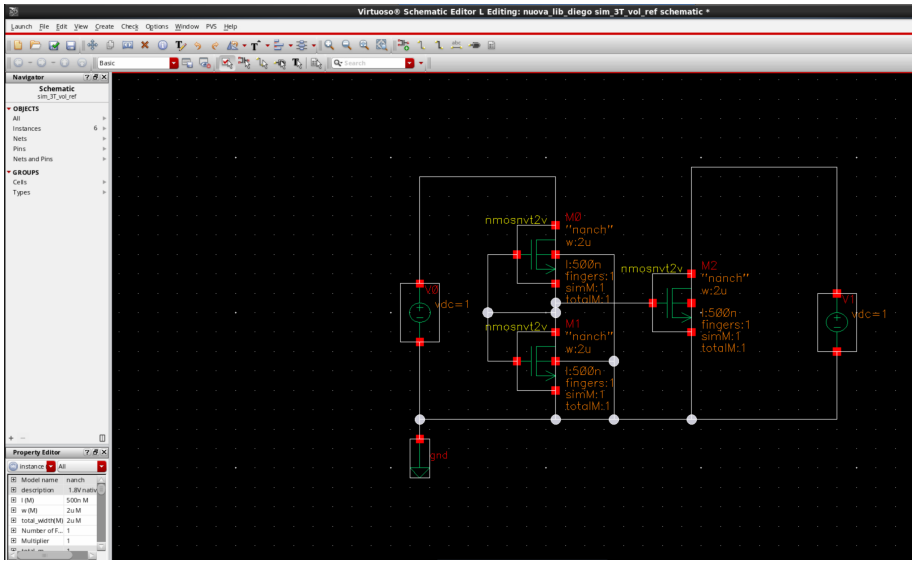


Fig. 2.1: Schematic view

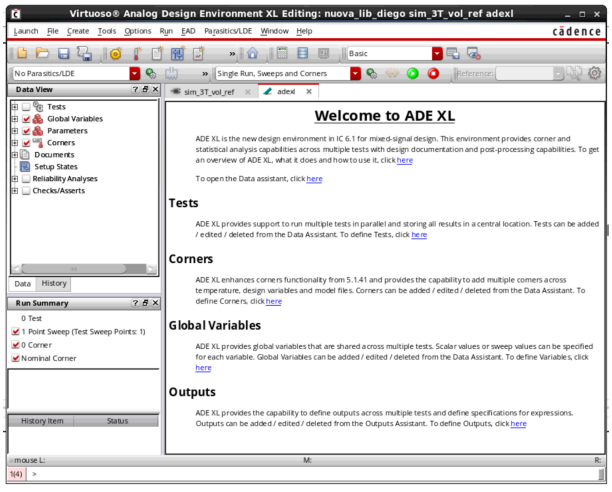


Fig. 2.2: ADEXL view

2.2 Circuit implementation and simulation

Fig (2.3) shows the circuit implementation of 3T voltage reference, Fig (1.20), where three transistor and two voltage supply were used. In this case, the transistors have the dimensions explained in the analysis by [2]. The dimension can be parametric where a label instead of a numerical value is needed (l1,l2,l3,w1,w2,w3). Additionally, the wires can be identified with a label (Vx).

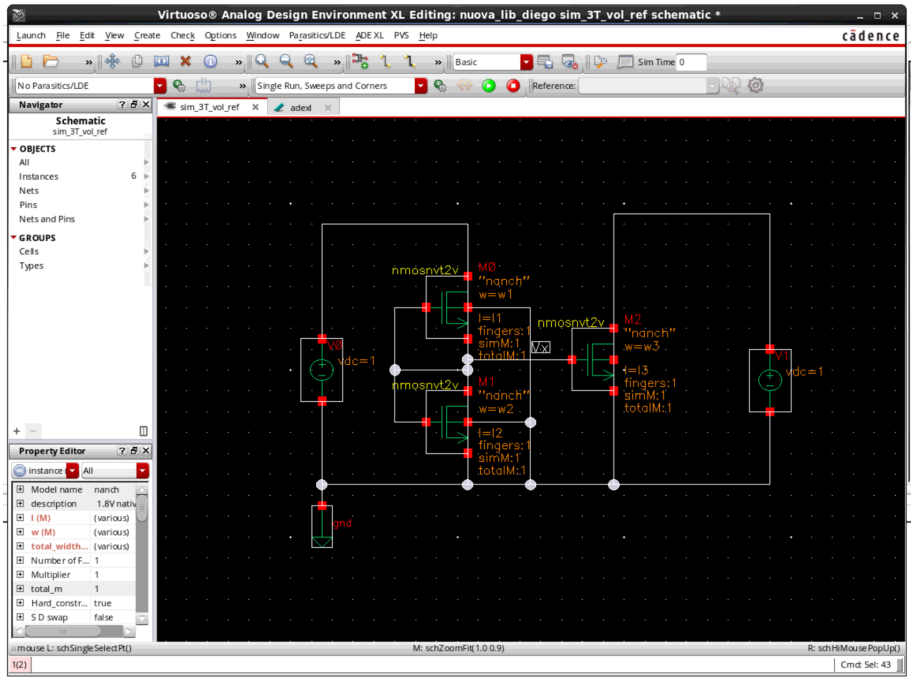


Fig. 2.3: Simple implementation in Schematic-L interface

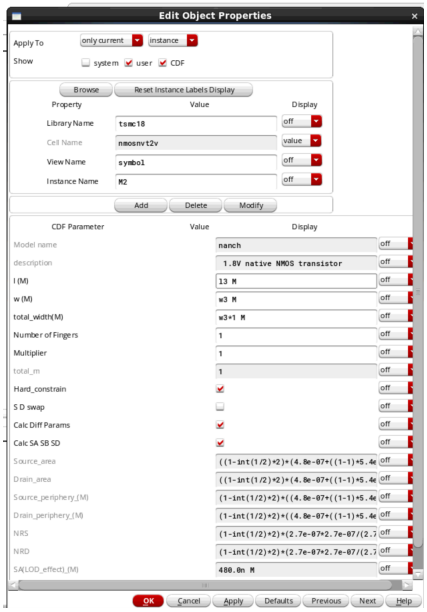


Fig. 2.4: Parametric configuration to test a circuit

Fig (2.4) shows the *"Edit Object Properties"* window where an element can be configured. In this case, the MOSFET dimensions were set with labels instead of numerical values. After, these labels can be copied from the *cellview* by the ADEXL tool, where they must be set with a numerical value in order to simulate a certain test.

Fig (2.5) shows the view to configure the analysis in a ADEXL simulation, the analysis DC must be selected, the tool allows to configure the Sweep Variable and its range must be set.

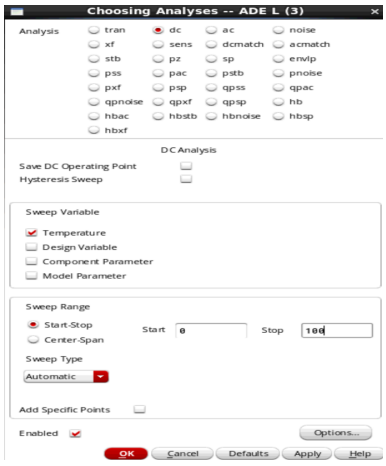


Fig. 2.5: Test configuration view

Additionally, the expressions to evaluate the figures of merit can be typed on the calculator tool, the this expressions can be copied to the *Outputs* section in the *Test Editor* view as shows in Fig (2.6). These expressions depend on the name of the node and the identified number element inside the schematic, these expressions are given by:

Temperature Coefficient

$$\text{TC}=\frac{ymax\left(IDC\left(M_3\right)\right)-ymin\left(IDC\left(M_3\right)\right)}{average\left(IDC\left(M_3\right)\right)\times 100}\times 10^6$$

where *ymax* and *ymin* are the maximum and minimum calculator functions, respectively, $IDC(M_3)$ is the DC current in the transistor M3 drain, i.e, load transistor for the configuration 3T current reference. In order to find this value, a Test with temperature variation must be done, the average must be calculated along the temperature variation. In this case a box-method is used to measure the TC.

Load Sensitivity

$$\text{LS}=100\times\frac{\left(value\left(IDC\left(M_{TOP}\right)VDD_{MAX}\right)-value\left(IDC\left(M_{TOP}\right)\right)VDD_{MIN}\right)}{I_{MEAN}\times\left(VDD_{MAX}-VDD_{MIN}\right)}$$

$$I_{MEAN}=\frac{value\left(IDC\left(M_{TOP}\right)VDD_{MAX}\right)+value\left(IDC\left(M_{TOP}\right)VDD_{MIN}\right)}{2}$$

where $\text{IDC}(M_{TOP})$ is the current measure on the top transistor in the block that works as load, because this transistor is the first in receiving the voltage supply, however the measure can be taken at any drain-transistor in the series connection when this exists. In order to find this value a DC simulation must be done, in this case the VCC, voltage supply, can be modified in a linear increasing. The average current must be calculated in the range from minimum VDD to maximum VDD, in this case the VDD maximum always be 1.5V and the minimum is a measure

parameter that depends on the strong change in the current reference in order to set a stable response in its output.

Current and Voltage at 20°C

$$V_X = \text{value}(VDC(V_x)\,20)$$

$$I_{REF} = \text{value}(IDC(M_2)\,20)$$

where VDC(V_x) is the calculator function to evaluate the V_x node at 20°C, with the same function the other voltages can be measured and evaluate at a certain temperature.

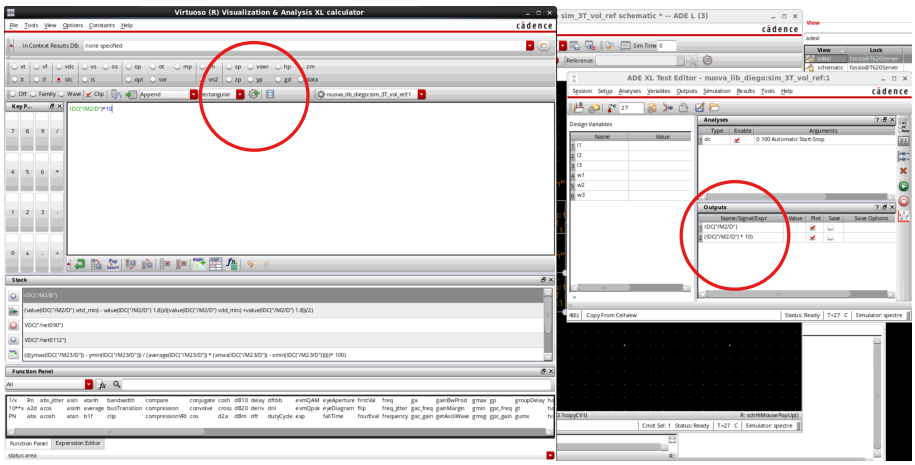


Fig. 2.6: Calculator view and Test Editor

Finally, the simulation can be presented neither as a numerical value, when an expression was entered, or a signal plot, when a node was selected and the *Output* is presented as signal type. Fig (2.7) shows the solution to the command IDC(M_2).

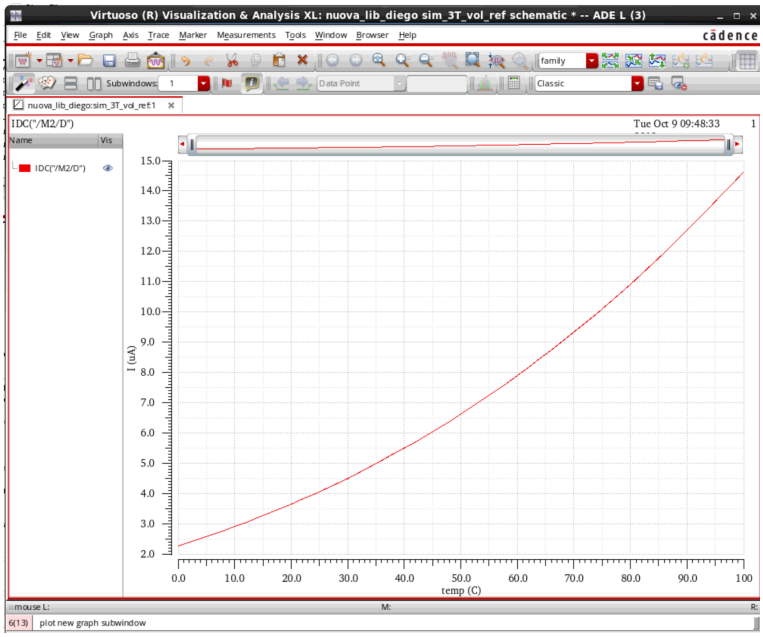


Fig. 2.7: Plot Simulation Result

2.2.1 Current Reference Circuits

In this section the circuits that were implemented with the transistor specifications are explained, the simple structures to improve the figures of merit are explained too, in Figure (2.8) is depicted the first current reference, where all the transistor are the same type, i.e, nmosmvt2v device, but with different gate oxide thickness. This allows reducing the process sensitivity in the proposed circuit, whereas the channel doping concentration represents the major source of process variability. In particular, the M2 and M3 are implemented by transistors with a greater gate oxide thickness, i.e. nmosmvt3v device, than the transistors used in M0 and M1 (i.e, nmosmvt2v). The nMOSFETs with a greater oxide thickness features a higher VTH with respect to the others, thus allowing one to achieve the desired value of Vx with a smaller number of stacked diode-connected transistors in M2 - M3, according to relation $V_x \approx k \times (V_{TH0,2} - V_{TH0,1})$.

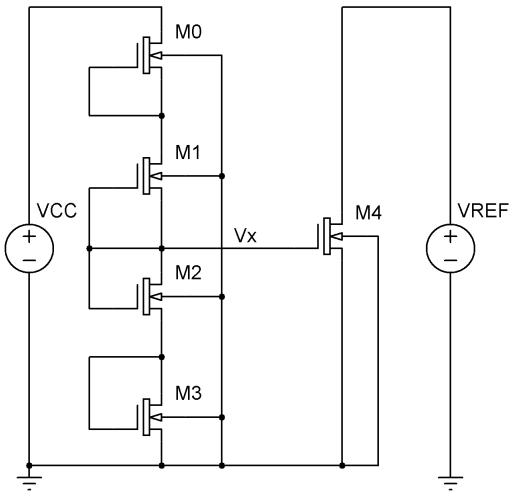


Fig. 2.8: First improvement implemented

The second circuit is depicted in Fig (2.9), in this case M2 and M3 transistors are the same of the above case, M1 and M0 are implemented through two series-connected nMOSFETs whose body terminal is connected to the corresponding source terminal, and the M4 - M11 (i.e, nmosmvt2v) transistors are implemented by using the circuit variant, i.e. by the series of the seven transistors, to increase its effective channel length. Again, as in the first circuit, all the nMOSFETs are implemented by LVT devices (i.e, nmosmvt2v), but with a greater oxide thickness for the transistors M2 and M3 (i.e, nmosmvt3v).

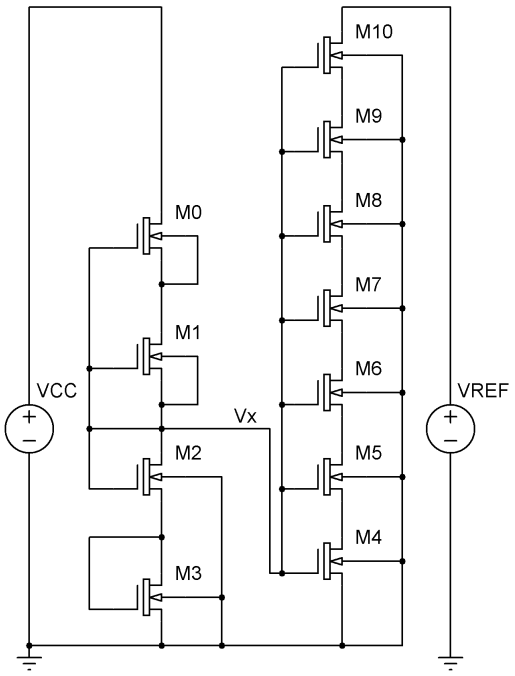


Fig. 2.9: Second improvement implemented

The third circuit is depicted in Fig (2.10) and Fig (2.11) with the difference in T2 and T3 blocks where the bulk must be biased with a certain voltage, body-bias voltage. The first circuit has the T2-block is tied to the first path of the circuit whose goal is providing the biasing voltage for the body of M8 transistor, all the transistors of the first path (M0-M4) are nmosmvt2v, T1 block is composed by nmosmvt2v-type transistors is series-connection and T2 block by nmosmvt3v in diode-connected mode, finally T3 block is composed by nmosmvt2v transistors in series connection. The use of the mvt-type transistors allows to minimize the process sensitivity, all the transistors in this path are the same channel doping and oxide thickness. For this reason, according to $V_x \approx k \times (V_{TH0,1} - V_{TH0,2})$, an increased number of stacked diode-connected transistors is required in M10 - M14 to reach the desired value of Vx, thus translating into a greater area occupancy.

Fig (2.11) shows the same structure explained above but the body-bias generator is tied to all the bulk-transistor of T3 block, T2 block transistors will have the bulk-node tied to ground. The T3 block keeps the series connection in order to increase

the channel length by the creation of a composite transistor.

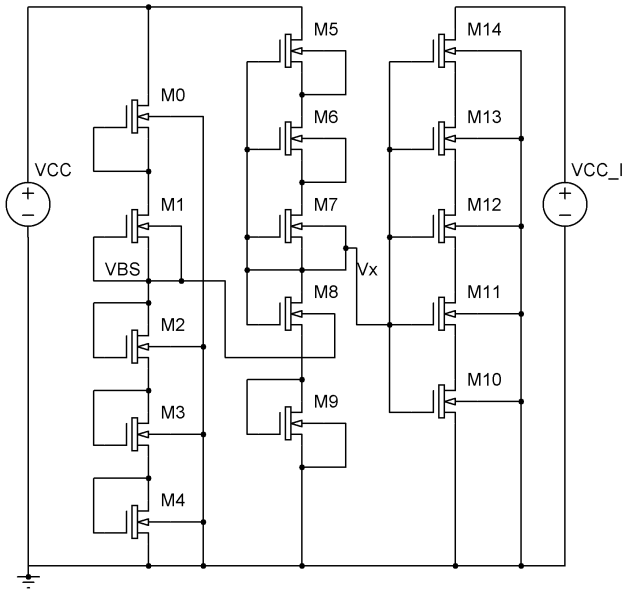


Fig. 2.10: Third improvement implemented - Body-bias generator for T2-block

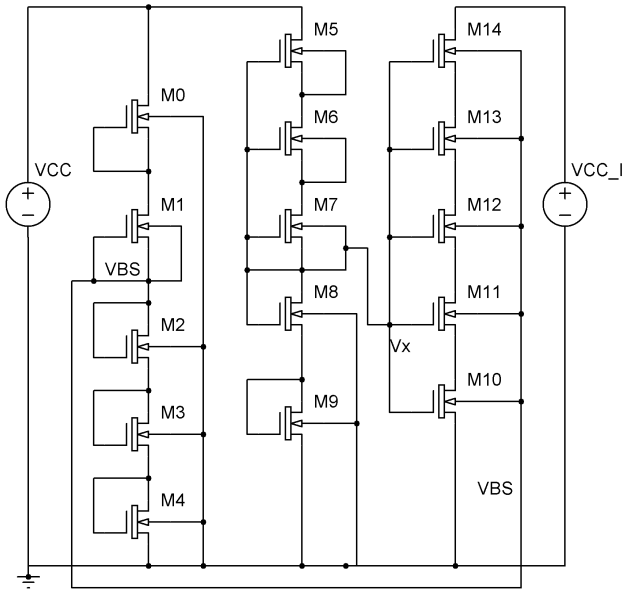


Fig. 2.11: Third improvement implemented - Body-bias generator for T3-block

2.2.2 Dimensions and model-transistors

The first two designs have the same parameters, in the simulations, this values has been trimmed but can be modified in order to improve the figure of merit, the ratio

W/L always should be kept in order to avoid harder variations. Table (2.1) shows the dimensions for the first and second design, and the voltage that have been settled in ADEXL file, this dimensions can be entered in a corner in order to look for a better result in a step-to-step process. The Table (2.2) shows the parameters and values for the third improvement, where the body-bias generator was implemented, the dimensions for this new path have increased the area occupancy of the circuit. In this case the dimensions can be modified as the above explanations.

Design	1st Design		2nd Design		Transistor
parameter	case I	case II	case I	case II	
l1[um]	1.5	1.8	3.06	2.88	M1,M0
w1[um]	4	3.6	5.4	4.5	
l2[um]	7	9	9	9	M2,M3
w2[um]	90	80	80.1	80.1	
l3[um]	1.2	1.08	9.9	10.08	M4-M10
w3[um]	1	1.26	1.44	1.44	
VCC[V]	1.5				
VREF[V]	1.5				
Temperature Range	0 to 100				

Table 2.1: Dimensions for 1st and 2nd design

Design	VBS T2 Block		VBS T3 Block		Transistor
parameter	case I	case II	case I	case II	
l1[μm]	1.95	1.77	5	1	M8,M9
w1[μm]	2.38	1.3	10	1.3	
l2[μm]	9.3	9.66	9	8	M5-M7
w2[μm]	100	100	100	80.1	
l3[μm]	10	10	10	9	M10-M14
w3[μm]	1.5	1.5	1.5	1.44	
lb[μm]	0.3	0.3	0.3	1.2	M2-M4
wb[μm]	0.58	0.49	0.58	0.6	
lp[μm]	4	5	5	3	M0-M1
wp[μm]	10	10	7	14	
VCC[V]	1.5				
VREF[V]	1.5				
Temperature Range	0 to 100				

Table 2.2: Dimensions for 3rd design with VBS

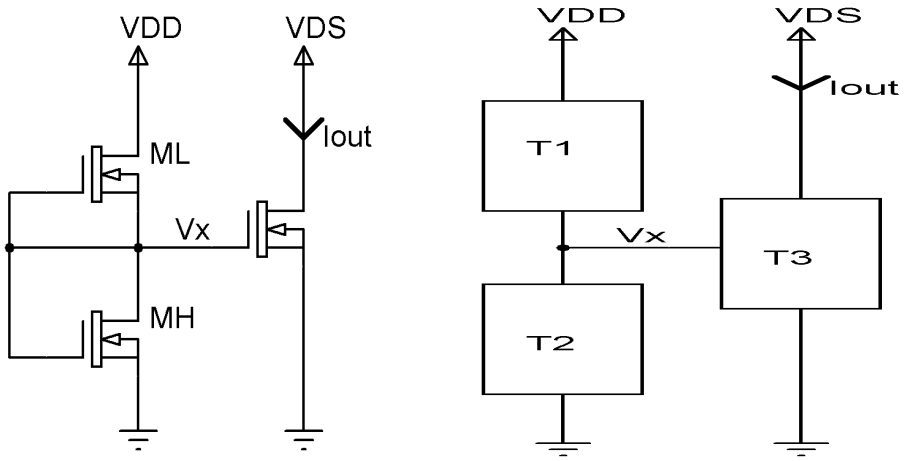
Chapter 3

Discussion and Results

This chapter shows the circuits used to implement different current references, each of them with a specific configuration. Firstly, a brief description about the improvements, in comparison with the 3T current reference, is done. Secondly, three solutions to reduce the power consumption and process sensitivity are shown, where each configuration is explained with its pros and cons. Finally, the results of each configuration are shown and compared between them in a chart, in order to identify the best option to implement the current reference.

3.1 Current reference block structure

Fig (3.1) shows the 3T current reference, studied in [2], and its block representation. These blocks can be composed by one or more MOSFETs tied to a same reference point or not, the aim of these new topologies is optimizing the figure of merit of the circuit in comparison to the results obtained in the previous research.



(a) (b)

Fig. 3.1: 3T current reference and its block representation

The block-T1 goal is to reach the best line sensitivity and reduce the power consumption of the CTAT/PTAT voltage reference. The block-T2 goal is to have a greater Vx in absolute value and a temperature dependency, using the less possible MOSFETs number, since the number of transistor has a direct relation with the temperature dependency. The block T3 aim is to reduce the line sensitivity and the temperature coefficient.

In Fig (3.1a),V_X can be considered like the difference between the $V_{TH,MH}$ and $V_{TH,ML}$, this V_X must to be near to MTC point in the load transistor, when this fact does not happen, a double MOSFET in diode and series connection allows to have a double V_X compared with only one MOSFET. A standard approach consists of designing current reference circuits able to reach and maintain the MTC point as operating point for a load transistor (M_{LOAD}) to ensure TC lower than 100 ppm/C° [25].

The reference current could decrease, if the block T3 and T2 are composed by one or more MOSFETs, with a series connection, e.g, self-cascode mode.

In the current reference proposed by [2], all the body transistor are tied to ground node, so the body effect is neglected. If it considers the body effect, the threshold

voltage could be changed, this fact increases the variable to control at the design time compared to the simple 3T current reference.

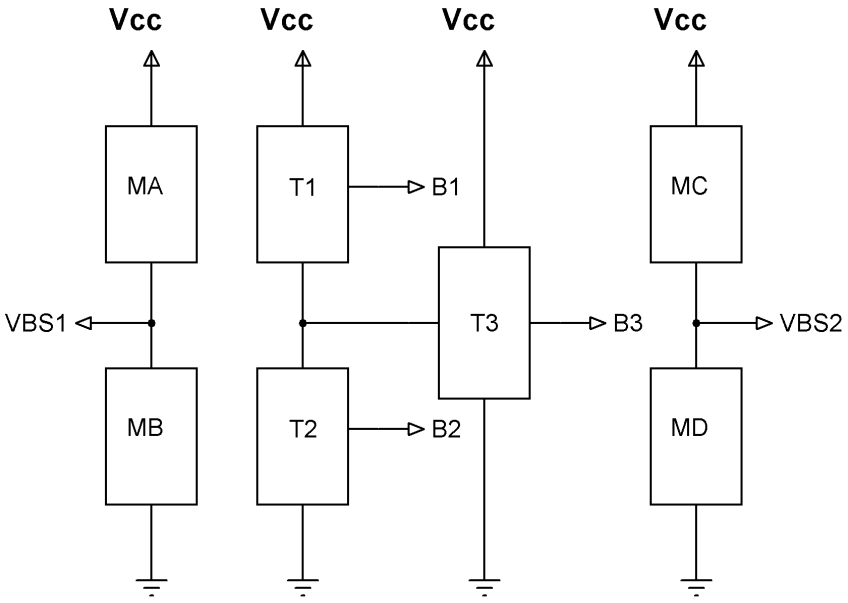


Fig. 3.2: Conceptual Diagram of the current reference

Fig (3.2) shows the conceptual diagram of the current reference implemented in this work. If it considers the body effect, the blocks T1, T2 and T3 could control this effect, since each T-block can have a different voltage applied to their body. The quantity to compose each block can become a drawback, this is the reason that some topologies were implemented in this work, in order to reduce the figures of merit (FOM) and the number of transistors to use and hence the area occupancy.

The labels B1, B2, B3 indicate the body output-node of each block and can be connected to some references, Table (3.1) shows the possible cases where the bodies could be connected, these connection allow to cancel the body effect and either reduce or increase the FOM so this connection must be studied at a small-signal level to understand their use at a specific circuit.

BODY	BODY CONNECTION CASES				
	I	II	III	IV	V
B1	SOURCE	SOURCE	SOURCE	VBS	VBS
B2	VBS	GND	VBS1	GND	GND
B3	GND	VBS1	VBS2	GND	GND

Table 3.1: Body connections to improve the characteristics of the current reference

With the above assumptions, when the body node is connected to its respective source, the body effect will be canceled, else if the body is connected to another node, e.g., ground or non-zero voltage, the body effect should be assumed in the calculus. Some analysis will be done with the assumption that the internal resistance of the transistors is so large that the transconductance due to the gate-source and body-source voltage can be neglected in the calculus but the designer has to understand their role in the circuit.

3.1.1 3T-current reference analytical description

The drain current in subthreshold region for the transistor MH and ML, Fig (3.1)(left), is given by:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{3.1}$$

where I_0 is a technology parameter, W and L the device width and length, respectively, V_{DS} the drain-source voltage, and n is the subthreshold factor.

The reference voltage will be given by the equating the two currents through MH and ML

$$V_X = \frac{V_{TH,MH} - \frac{n_{MH}}{n_{ML}} V_{TH,ML} + n_{MH} V_T \ln\left(\frac{I_{ML} W_{ML} L_{MH}}{I_{MH} W_{MH} L_{ML}}\right)}{1 + \frac{n_{MH}}{n_{ML}} \lambda_{B,ML}} \tag{3.2}$$

where $\lambda_{B,ML}$ is the body effect coefficient and is given by

$$\lambda_B = \frac{\sqrt{2\varepsilon_s q N_a}}{C_{ox}}$$

where ε_s is the dielectric constant, q is the elementary charge, N_a is the intrinsic carrier density and C_{ox} is the oxide capacitance given by the relation between the dielectric constant and the oxide thickness, ε_{ox}/t_{ox}, so this coefficient is not temperature dependent, with these assumptions the ΔV_X can be modified if the oxide thickness is different either the MH or ML transistor and for the temperature dependency showed in the previous chapters.

3.1.2 Internal block structure

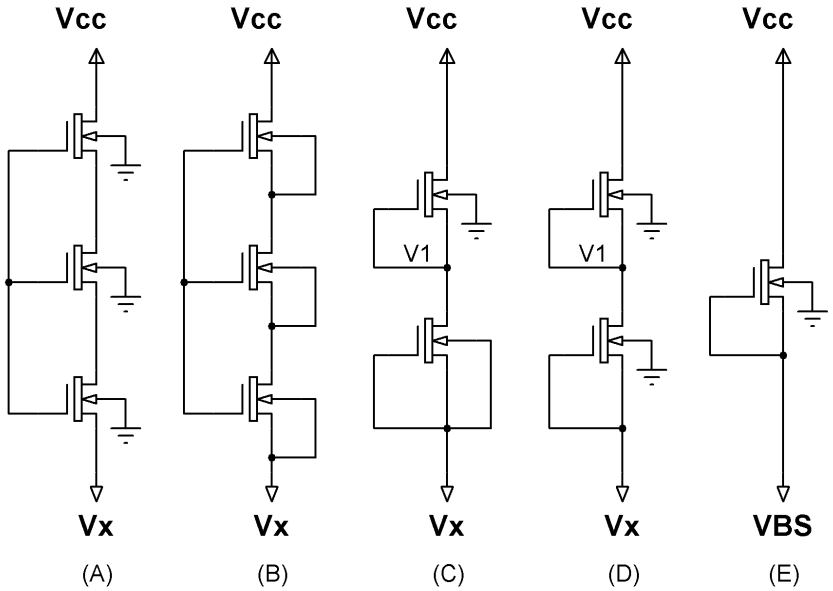


Fig. 3.3: Schematics for block T1

Different topologies to implement each block will be considered in this section. First, Fig (3.3) shows the possible circuits used to form the block T1. Solution (A) is composed by three transistors where their body are tied to ground, so the body-effect can not be neglected, the same gate-source voltage is tied to all the gate

of the transistors, this connection is known as self-cascode connection and has a representation as a unique transistor, solution (B) is similar but the body nodes are tied to their respective source so the body effect is neglected, $gm_{SC} \approx gm_1$, where gm_1 is the transconductance of the transistor placed on the bottom, it is important that the transistors in these connection , e.g, A or B, have the same dimensions and technology.

On the other hand, solutions (C) and (D) are similar between them, these solutions always have the upper transistor connected to ground in its body. If it considers a power supply V_{DD} increase, the node V_x and V_1 will increase their values and the body voltage in the upper transistor will increase with a negative tendency, so the current at the upper transistor will decrease. If the current decreases, it will attenuate the increasing of the value in V_1 and decrease the line sensitivity value. Finally, the structure in case (E) will be used when the line sensitivity is not a critical requirement.

In the solutions (C) and (D), the current that flows on the CTAT/PTAT voltage reference will be compromised when the MOSFETs body is connected either to ground or source node (excluding the upper MOSFET) since the ground connection decreases the current, so that the no-low voltages MOSFETs could not operate and the entire circuit could not work, because the leakage current will be similar to the current through the CTAT/PTAT voltage reference therefore there is not current to drive the transistors.

The T1 block body could be connected to the circuit that yields VBS1, but the voltage reached will not be satisfactory to lead a correct operation, so the body voltage must be greater than V_X. This requirement will need of a MOSFET large amount at the block MB which leads to increase the chip area and the minimum voltage supply since the body-source voltage must be 300mV greater than V_X to yield an increase in the merit factor related with the area usage. The VBS generator to feed the block T1 must have a small line sensitivity, because if the power supply

voltages increases, the VBS will increase and the MOSFETs threshold voltage will decrease in the block T1. A positive feedback loop is created, that increases the line sensitivity value, when the current through the CTAT/PTAT voltage reference increases, the V_X and the output current increases too.

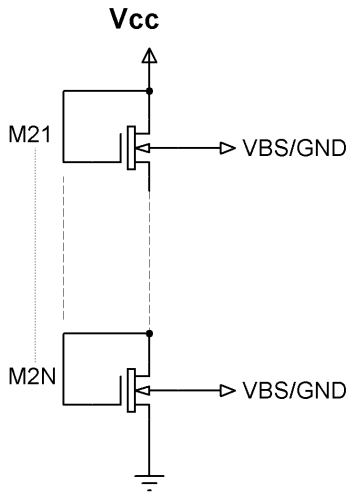


Fig. 3.4: Schematics for block T2

The T2 block implementation is composed by one or more transistor in stack connection, as shows Fig (3.4), and the MOSFETs body can be connected to ground or VBS generator. The transistor number depends on the MTC point at the output of block T3. When the VBS generator is connected to this block, the line sensitivity must have a value around 10% (weak value) and compensate the process variation with a change in its value by a corner adjusting in the V_X, where the gate voltage overdrive of the output in block T3 and the output current should be constant over the corner. The body-voltage-generator line sensitivity has to be around 10% because a power supply voltage increasing will give a VBS and V_X increase. If the VBS increases, the MOSFETs, with their bodies connected to VBS generator, will decrease their threshold voltages and the V_X value. This feedback will increase the line sensitivity of the CTAT/PTAT voltage reference and the reference current, consecutively. The number of MOSFETs usually is around 7, a greater number will increase the line sensitivity line since the block T2 equivalent resistance depends on

the MOSFETs number.

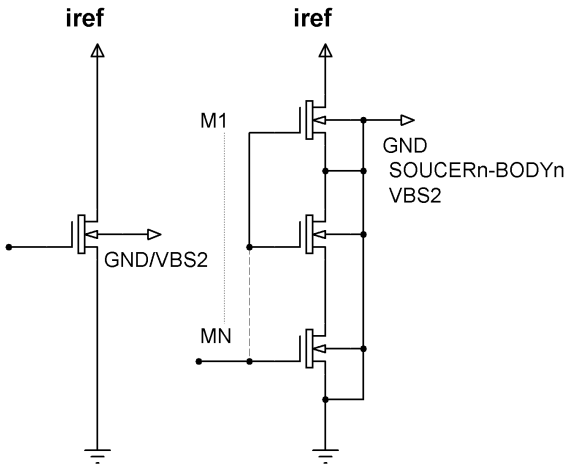


Fig. 3.5: Schematics for block T3

The block T3 can be implemented with one or more transistor connected in series, as shows Fig (3.5), this connection allows to have a reference current with a low value, whereas a connection between body and source at the same MOSFET shows a great load sensitivity instead of a body and ground connection.

Connecting the body generator to the MOSFETs body in block T3 allows reducing the MOSFETs threshold voltage and the MTC point voltage value. If the body bias generator is connected to block T3, the line sensitivity must have a great value (around 1%-2%), because there is a positive feedback that increases the line sensitivity. On the other hand, if the power supply increases, the VBS will increase whereas the MOSFETs threshold voltage will decrease and so the reference current will increase. The use of the body bias generator in the T3-block is needed when the line sensitivity is a critical parameter to control in the requirements of the design.

3.2 Improved current reference circuit

Based on the above ideas, Fig (3.2), each block can be designed with a different topology. In this section, a explanation about each improvement is done, after that the dimensions to get their respective results are shown. These improvements are shown the best results and circuits like the body bias generator was not used to implement all the blocks, only the third improvement has required the using of that to implement the T2-block.

3.2.1 First Improvement

Description

The first circuit is showed at Fig (3.6), where a structure (C), Fig (3.3), is used for the T1 block and two MOSFETs for the T2 block are used. The upper MOSFET of T1 block reduces the line sensitivity, the two MOSFETs of the T2 block allow to have a greater V_X and use a non-native MOSFET for the load transistor of the T3 block. The drawback in this design is the process sensitivity since the native transistors present a critical value of this.

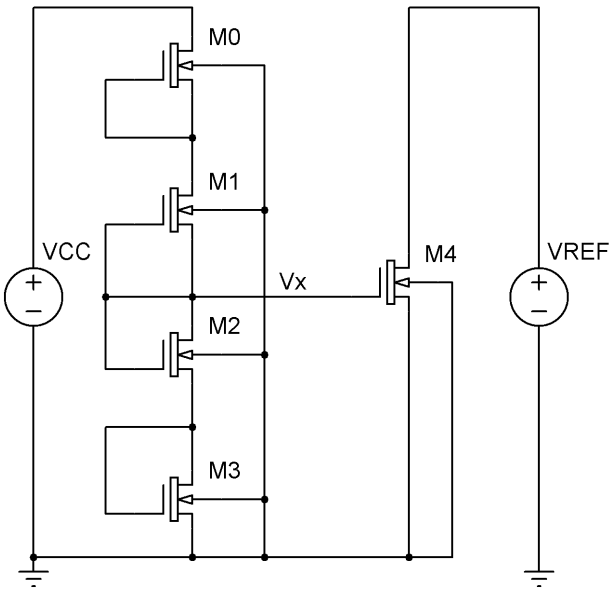


Fig. 3.6: First model improved current reference

Small-Signal Analysis

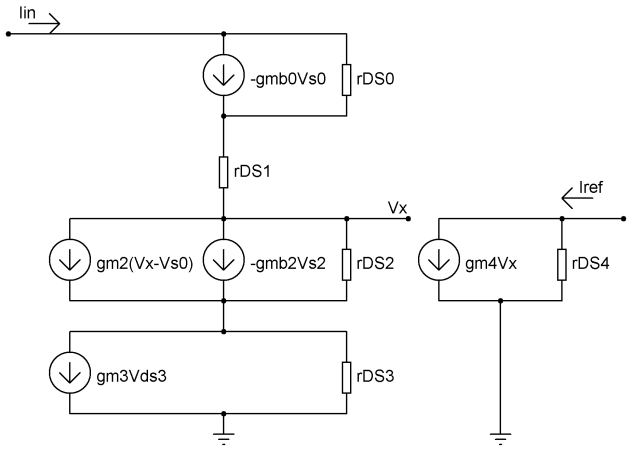


Fig. 3.7: Small-signal representation of first improvement

$$Vx = V_{DS2} + V_{DS3} = \left(\left(\frac{1}{gm_2} + \frac{gmb_2}{gm_2 gm_3} \right) + \frac{1}{gm_3} \right) I_{in}$$

$$\Delta I = \frac{I_{ref}}{I_{in}} = \frac{gm_4 V_x}{I_{in}} = gm_4 \left(\frac{1}{gm_2} + \frac{gmb_2}{gm_2 gm_3} + \frac{1}{gm_3} \right) \tag{3.3}$$

Eq. (3.3) shows that the current variation is directly proportional to the transconductance in the load transistor and it can be driven with the transistors in the block T2 (M2 and M3), so if the current variation on the M2 and M3 is reduced, the line sensitivity of the circuit will be stable along the temperature variation. M3 is in diode-connected mode so it always is in saturation region and presents a constant behavior. M2 and M3 are the same type of transistor so equation (3.3) could neglect the body effect and the ΔI can be directly driven by a high width in the transistors.

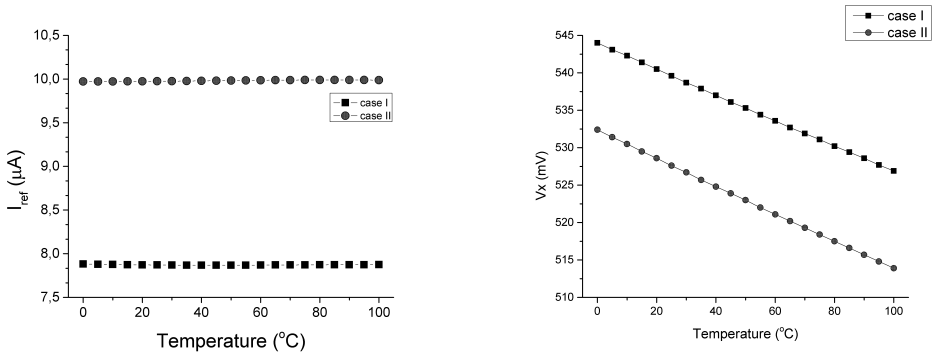
Results

The best results were obtained with the dimensions showed in Table (3.2). On the other hand, Fig (3.8) and (3.9) shows the response of the voltage reference used to bias the current reference for a temperature and voltage variation, respectively. Such as was explained in the previous chapter, the biasing voltage should be near

to 500mV. The current reference present a stable current and a voltage variation approximately equals to 20mV for the temperature variation. Fig (3.9) shows the response for a voltage variation in the supply, and the minimum voltage is obtained, 0.6V. The figure of merit (FOM) are shown in Table (3.2).

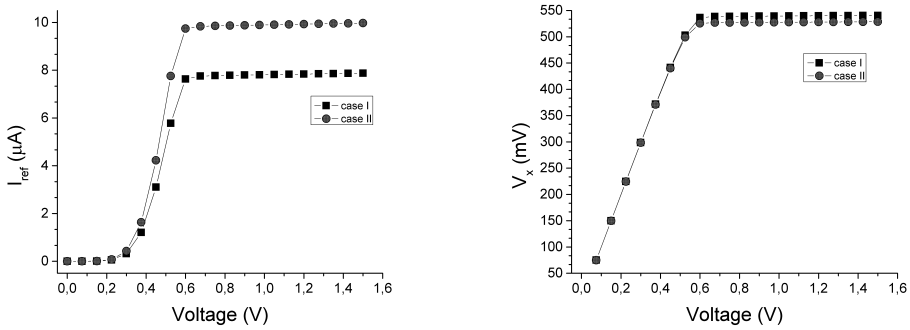
parameter	case I	case II
l1[μm]	1.5	1.8
l2[μm]	7	9
l3[μm]	1.2	1.08
w1[μm]	4	3.6
w2[μm]	90	80
w3[μm]	1	1.26
TC[ppm/°C]	16	18
LS[%/V]	3.45	2.64
VDD_{MIN}[V]	0.6	0.6
V_{REF}@20°C [V]	0.54	0.52
I_{REF}@20°C[uA]	7.85	10
PS[%]	3.73	2.34
Power Total[uW]	11.77	15

Table 3.2: Dimensions and FOM for simulation in 1st improvement



(a) (b)

Fig. 3.8: First Improvement: Current and Voltage reference versus Temperature



(a) (b)

Fig. 3.9: First Improvement: Current and Voltage reference versus Voltage Supply

3.2.2 Second Improvement

Description

The second circuit is showed in Fig (3.10), where the T3 block uses seven MOSFETs in self-cascode connection, where the dimensions of the all transistors are the same, this improvement allows to increase the channel length of the composite transistor and reduce the changes due to the variation in the gate-source voltage, Vx. If the equation (3.3) is assumed in this circuit, the parameter gm_4 will represent the equivalent transconductance of the composite transistor. In this case, an analysis of this transconductance allows to show the incidence of the dimensions of these transistors in the response of the current reference.

$$gm_4 \approx \mu_n C_{OX} \left(V_X - V_{TH}\right) \frac{W}{L} \approx K_N \frac{W}{L}$$

The equivalent resistance of this composite transistor will be given by

$$R_4 \approx \frac{1}{gm_4} \approx \frac{1}{K_N \dfrac{W}{L}} \approx \frac{L}{K_N W} \tag{3.4}$$

Equation (3.4) shows that the larger width smaller resistance, so in the next results the parameter to size the load transistors will get a high width and a small length in order to reduce the variation on the current, equation (3.3).

In addition to this modification on the load transistors, a structure (B), Fig (3.3), is used to implement the T1 block and the block T2 is implemented with two transistors in diode-connected mode.

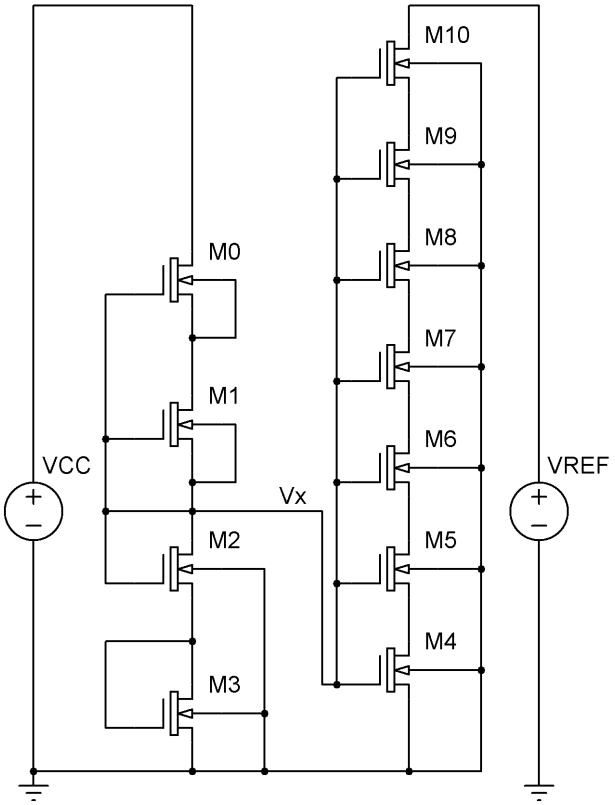
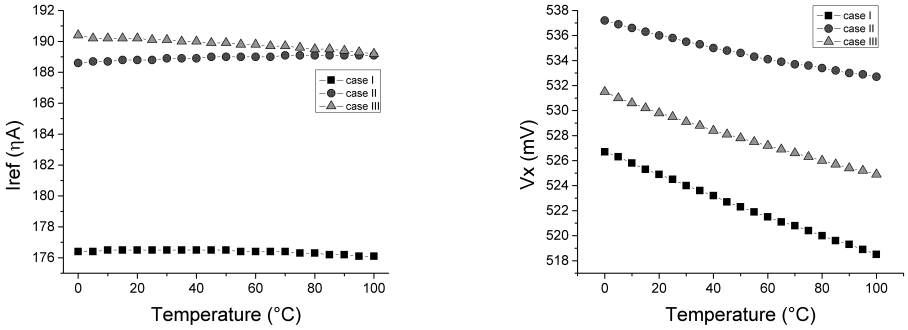


Fig. 3.10: Second model improved current reference

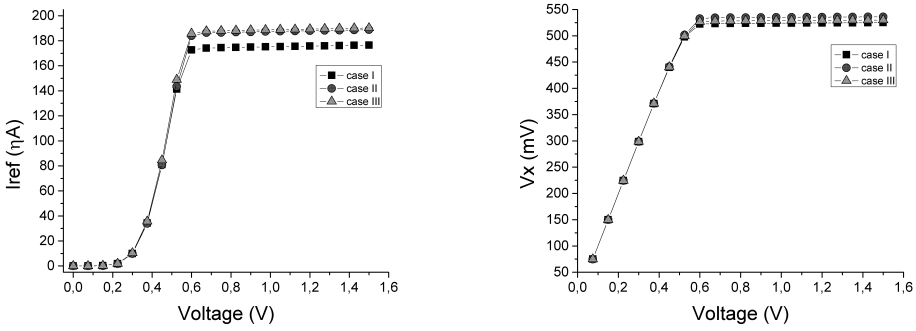
Results

The best results were obtained with the dimensions showed in Table (3.3). Fig (3.11) shows the results for the three cases when there is a temperature variation, the reference current present a reduction towards to nanoamperes range instead of microamperes as was showed in the first improvement. In addition, the voltage reference presents a voltage as stable as possible since the deviation is around a few millivolts at unit scale. Fig (3.12) shows the results for the cases when the circuit is supplied with a variable supply, the minimum voltage is obtained and this is fixed as the previous design in 0.6V. In this case, the reference current is reduced since the transconductance of the composite transistor in the load, allows to drive the current along the voltage variation.



(a) (b)

Fig. 3.11: Second Improvement: Current and Voltage reference versus Temperature



(a) (b)

Fig. 3.12: Second Improvement: Current and Voltage reference versus Voltage Supply

parameter	case I	case II	case III
l1[μm]	3.06	2.88	3
l2[μm]	9	9	9
l3[μm]	9.9	10.08	10
w1[μm]	5.4	4.5	5
w2[μm]	80.1	80.1	80
w3[μm]	1.44	1.44	1.5
TC[ppm/°C]	25	23	62.23
LS[%/V]	2.41	2.89	2.58
VDD_{MIN}[V]	0.6	0.6	0.6
V_{REF}@20°C[V]	0.524	0.535	0.529
I_{REF}@20°C[nA]	176	188	190
PS[%]	2.18	2.63	2.34
Power[nW]	263	282	285

Table 3.3: Dimensions and FOM for simulation in 1st improvement

3.2.3 Third improvement

This section introduces the concept to bias the body of the blocks, Fig (3.2), this body-biasing was done at T2 and T3 blocks, T1-block was neglected since their body always needs to be tied to their own source in order to accomplish the concept of 3T-current reference showed in the first section of this chapter, where the goal is reduce the temperature-dependency of the circuit, so T1-block does not use the voltage from the body-bias generator.

Body-biasing of T2-block

Description Fig (3.13) shows the current reference circuit compose by: a body-bias generator which provides the VBS signal to M8 inside T2-block, a second path is composed by T1 and T2-block and the last by the T3-block which is composed by transistors in series connection. T1-block is composed by three transistors in (B) type connection, Fig (3.3), T2-block is composed by two transistor, one of them is biased by the body-bias generator and the last is in diode-connected mode, T3 block is composed by five transistors in series connection. All the transistors have the same technology-parameters with exception of M8 and M9 whose the oxide thickness is greater, in order to guarantee the 3T-currente reference concept.

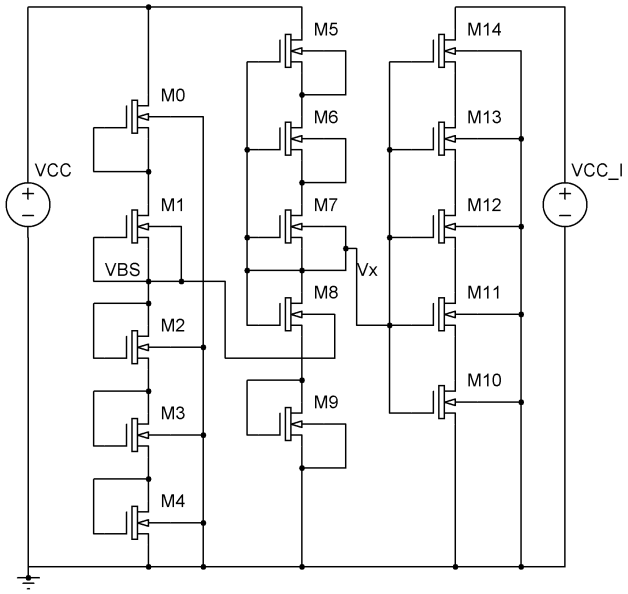


Fig. 3.13: Body-biasing on T2-block

Small Signal Analysis The advantages of this connection are analyzed in base on small-signal model. All the transistor used to build this circuit, own to the same type to exception of M8 and M9, these are a greater voltage threshold than the others. In this case, the input current is in function of the two paths, $i_{IN} = i_{IN1} + i_{IN2}$, the input resistance can be driven by the internal resistance of M0 and M1, and the transconductance of M2-M4, in this case the body effect was neglected. Analytic analysis is in (B).

$$r_{in} = \frac{V_{IN}}{i_{IN1}} = \left(r_0 + r_1 + \frac{1}{1 + gm_2} + \frac{1}{gm_3} + \frac{1}{gm_4} \right) \tag{3.5}$$

Either r_0 or r_1 can drive the internal resistance of the path, so these resistance works as a current regulator while the slight current changes can be driven by the transconductance $gm_2, gm_3,$ and gm_4.

From the concept of 3T-current reference [2], the currents to drive the path are in M1 and M2, given by eq. (3.1), are

$$I_{D2} = I_{02}\frac{W_2}{L_2}\exp\left(\frac{V_{BS} - V_{TH,02}}{n_{02}V_T}\right)$$

$$I_{D1} = I_{01}\frac{W_1}{L_1}\exp\left(\frac{-V_{TH,01} - \lambda_{B1}V_{BS}}{n_{01}V_T}\right)$$

, equating the previous equations the V_{BS} can be calculated as:

$$V_{BS} = \frac{V_{TH,02} - \frac{n_{02}}{n_{01}}V_{TH,01} + n_{02}V_T \ln\left(\frac{I_{D1}}{I_{D2}}\frac{W_1L_2}{W_2L_1}\right)}{1 + \frac{n_{02}}{n_{01}}\lambda_{B1}} \tag{3.6}$$

In order to avoid a high variation at V_{BS} the device dimensions on M2 and M1 must be greater than the dimensions looked in M7 and M8, because the goal of this path is reduce the temperature dependency of the body of M8.

On the next path, the reference voltage is given by the equating currents on M8 and M7 transistors but body-M8 is tied to V_{BS} provided by the previous path so the currents will be given by

$$I_{D8} = I_{08}\frac{W_8}{L_8}\exp\left(\frac{V_X - V_{TH,08} - \lambda_{B8}V_{BS}}{n_{08}V_T}\right)$$

$$I_{D7} = I_{07}\frac{W_7}{L_7}\exp\left(\frac{-V_{TH,07} - \lambda_{B7}V_X}{n_{07}V_T}\right)$$

Vx is given by equation (3.7), where $V_T = kT/q$, k is the Boltzmann constant, T the absolute temperature and q the elementary charge. n_{08} and n_{07} are the subthreshold factor, W and L are the device dimensions, and V_{BS} is the voltage provided by the previous stage, which functions is helping to keep the temperature variations as small as possible.

$$V_x = \frac{V_{TH,08} - \frac{n_{08}}{n_{07}} V_{TH,07} + \lambda_{B8} V_{BS} + n_{08} V_T \ln\left(\frac{I_{07} W_7 L_8}{I_{08} W_8 L_7}\right)}{\left(1 + \frac{n_{08}}{n_{07}} \lambda_{B7}\right)} \tag{3.7}$$

By assuming n_{08}/n_{07}, I_{07}/I_{08}, λ_{B7}, λ_{B8} temperature-independent, the variation of Vx in the temperature range will be given by

$$\Delta V_x = \frac{\Delta V_{TH,08} - \frac{n_{08}}{n_{07}} \Delta V_{TH,07} + \lambda_{B8} \Delta V_{BS} + n_{08} \frac{k\Delta T}{q} \ln\left(\frac{I_{07} W_7 L_8}{I_{08} W_8 L_7}\right)}{\left(1 + \frac{n_{08}}{n_{07}} \lambda_{B7}\right)} \tag{3.8}$$

The variations over V_X are taken by $V_{GS10...14}$, V_X present a stable signal along the temperature variation so output current will be stable too.

Finally, the path of load transistor from M10 to M14 is driven by V_X and the number of transistors presents a transconductance equivalent to $\frac{i_D}{V_{GS}} \approx gm_{10}$ since the series connection allows to increase the length channel and the arrangement can be equal to a composite transistor with better electric characteristics.

Results The temperature coefficient, TC, can be driven by the voltage applied to the M8-body since as shown in (3.8) the variation on voltage reference can be driven slightly with the body effect of the transistor M8, whose threshold voltage was modified by the adding of VBS. Table (3.4) shows the TC improvement with the VBS increasing, the measures were measured at 20°C.

$V_{BS}\,[mV]$	$V_X\,[mV]$	TC	LS	$I_{REF}\,[nA]$
0	551	33	0.93	313
25	542	191	0.89	292
50	532	42	0.81	272
60	528	25	0.83	263
70	525	84	0.85	256
80	521	150	0.859	249

Table 3.4: Parameter variations in function to voltage applied at M8-transistor

Fig. (3.14) shows the response of the electric parameters in function of the supply variations, the minimum voltage can be assumed at 600mV like the previous improvement and the current reference is set at 220nA, Figure (3.14a), the voltage reference shows a response close to the MTC-point of the T3-block at 500mV, Figure (3.14b), the body-bias generator shows a stable response after its biasing at 200mV, after this value the response of the bias generator increases slightly in function of the voltage supply. Figure (3.14c).

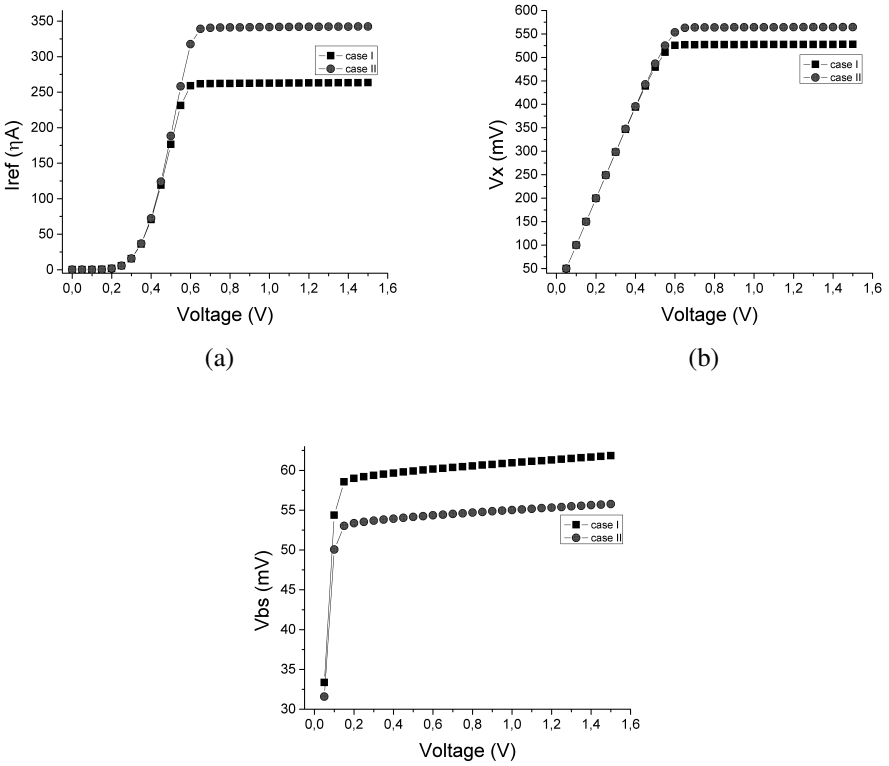


Fig. 3.14: (a) Current reference curve (b) Voltage reference curve (c) Body-Voltage generator, all of them in function of voltage supply

Fig. (3.15) shows the response of the electric parameters in function of the temperature variations, Fig. (3.15a) shows the current reference changes from 0 to 100 degrees, at the minimum temperature there is a current since the circuit was biased to 1.5V at the voltage supply, the current present a variation around the 1.2uA. Fig. (3.15b) shows the voltage reference response where there is a difference 6mV along the temperature variations. Fig. (3.15c) shows the compensation did by the first path of the circuit, this curve present a difference at 1mV along the changes so the temperature coefficient does not have a weighty change.

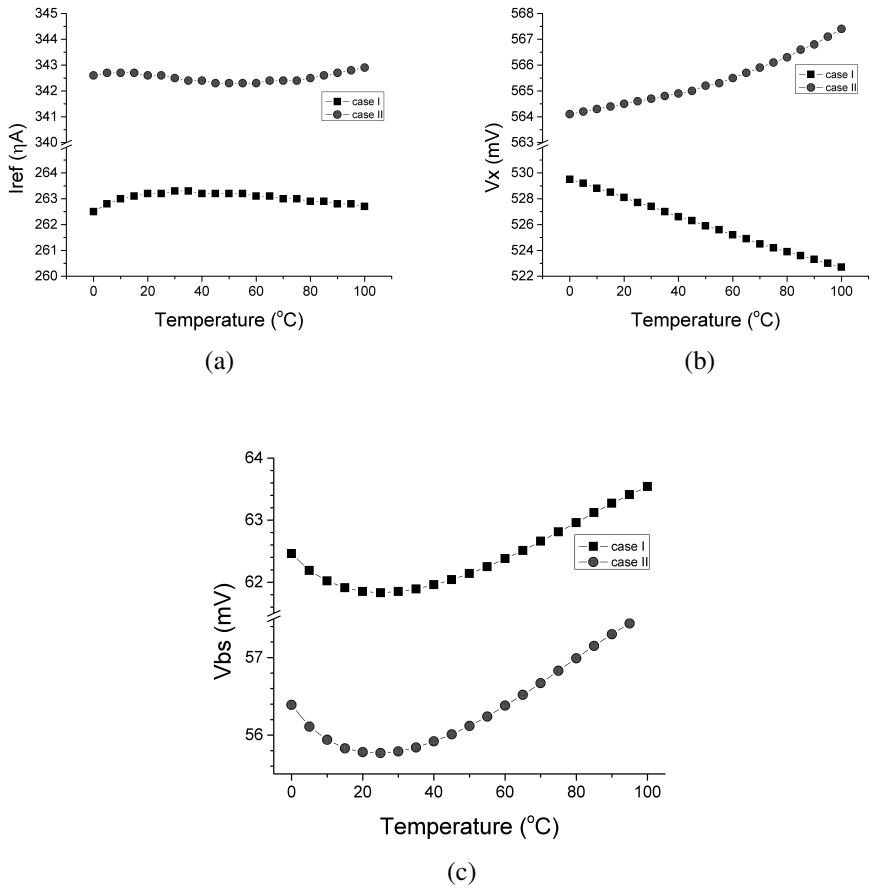


Fig. 3.15: (a) Current reference curve (b) Voltage reference curve (c) Body-Voltage generator, all of them in function of temperature variation

Finally, Table (3.5) shows the results for the body-bias to the T2-block, two cases are shown in order to compare the changes at the size level.

parameter	case I	case II
l1[μm]	1.95	1.77
l2[μm]	9.3	9.66
l3[μm]	10	10
lb[μm]	0.3	0.3
lp[μm]	4	5
w1[μm]	2.38	1.3
w2[μm]	100	100
w3[μm]	1.5	1.5
wb[μm]	0.58	0.49
wp[μm]	10	10
TC[ppm/°C]	28	17
LS[%/V]	0.66	0.99
VDD_{MIN}[V]	0.6	0.6
V_{REF}@20°C[V]	528	564
I_{REF}@20°C[nA]	263	342
PS[%]	1.94	7.87
Power Total[nW]	394	513
V_{BS}@20°C[V]	62	55

Table 3.5: Dimensions and FOM for T2-block with body-bias

Body-biasing of T3-block

Description Fig (3.16) shows the current reference circuit compose by: a body-bias generator which provides the VBS signal to all the transistors at T3-block, a second path is composed by T1-block and T2-block and the last by the t3-block which is composed by transistors in series connection. T1-block is composed by three transistors in (B) type connection, Fig (3.3), T2-block is composed by two transistor in diode-connected mode, T3 block is composed by five transistors in series connection. All the transistors have the same technology-parameters with exception of M8 and M9 whose the oxide thickness is greater, in order to guarantee the 3T-currente reference concept.

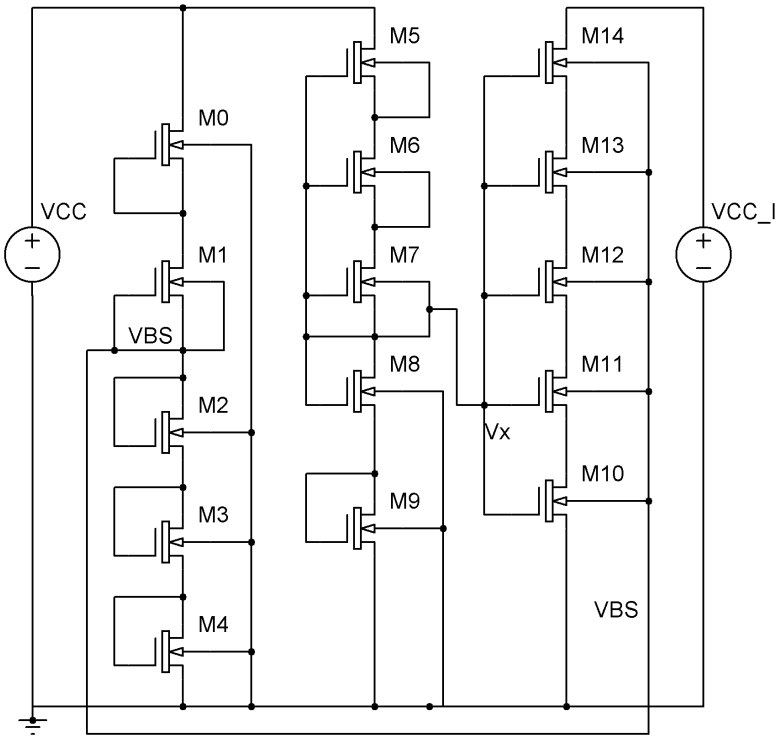


Fig. 3.16: Body-biasing on T3-block

Small-signal analysis From the concept of 3T-current reference [2], the V_{BS} can be obtained by equation (3.2) with the equating of the drain currents in M7 and M8 given by (3.1), this value was calculated previously and is given by

$$V_{BS} = \frac{V_{TH,02} - \frac{n_{02}}{n_{01}} V_{TH,01} + n_{02} V_T \ln\left(\frac{I_{D1}}{I_{D2}} \frac{W_1 L_2}{W_2 L_1}\right)}{1 + \frac{n_{02}}{n_{01}} \lambda_{B1}}$$

The second path provides a voltage given by the relation at (3.2), so the voltage reference, V_X can be obtained by the equating of the currents (3.1) for M7 and M8 and taking in account (1.1).

$$I_{D7} = I_{07} \frac{W_7}{L_7} \exp\left(\frac{-V_{TH,07} - \lambda_{B7} V_X}{n_{07} V_T}\right)$$

$$I_{D8} = I_{08} \frac{W_8}{L_8} \exp\left(\frac{(V_X - V_{DS9}) - (V_{TH,08} + \lambda_{B8} V_{DS9})}{n_{08} V_T}\right)$$

$$V_x = \frac{V_{TH,08} + (1 + \lambda_{B8}) V_{DS9} - \frac{n_{08}}{n_{07}} V_{TH,07} + n_{08} V_T \ln\left(\frac{I_{07} W_7 L_8}{I_{08} W_8 L_7}\right)}{\left(1 + \frac{n_{08}}{n_{07}} \lambda_{B7}\right)} \tag{3.9}$$

In this case the body of M8 is tied to ground but the source is tied to a voltage greater than the bulk so the intrinsic-threshold of M8 is greater than the M7, this yields an increasing at V_X.

Results In this circuit, two cases were studied, one of then presents a high TC but the V_X reaches a value approximately equal to the MTC point of the load, whereas the other case shows a TC low but the V_X and LS have increased their values. Fig. (3.17a) shows that the VD$D_{MIN}$is reduced for the second case where the TC was reduced, whereas the first case has a VDD_{MIN}equal to the previous cases. Fig. (3.17b) shows how long is the distance between the two cases from the MTC point of the transistors placed at the load. Fig. (3.18a) shows the I_{REF} variations along the temperature changes, the curve does not have a non-stable behavior that means the first path of the circuit is working well. Fig. (3.18b) shows the voltage reference

presents a better behavior for the first case where the voltage difference is slightly smaller than the other case. Fig. (3.18c) shows the behavior of the body-bias voltage, the main difference is that for the first case the value is approximately a half than the second case, this is due to the V_X which feed the composite transistor at the load. Finally, Table (3.6) shows the results for the simulation cases, for the first case the worst value is the temperature coefficient and for the second the minimum voltage and the process and linear sensitivity, that is the reason why this method can be used if the temperature coefficient is not a main parameter to improve.

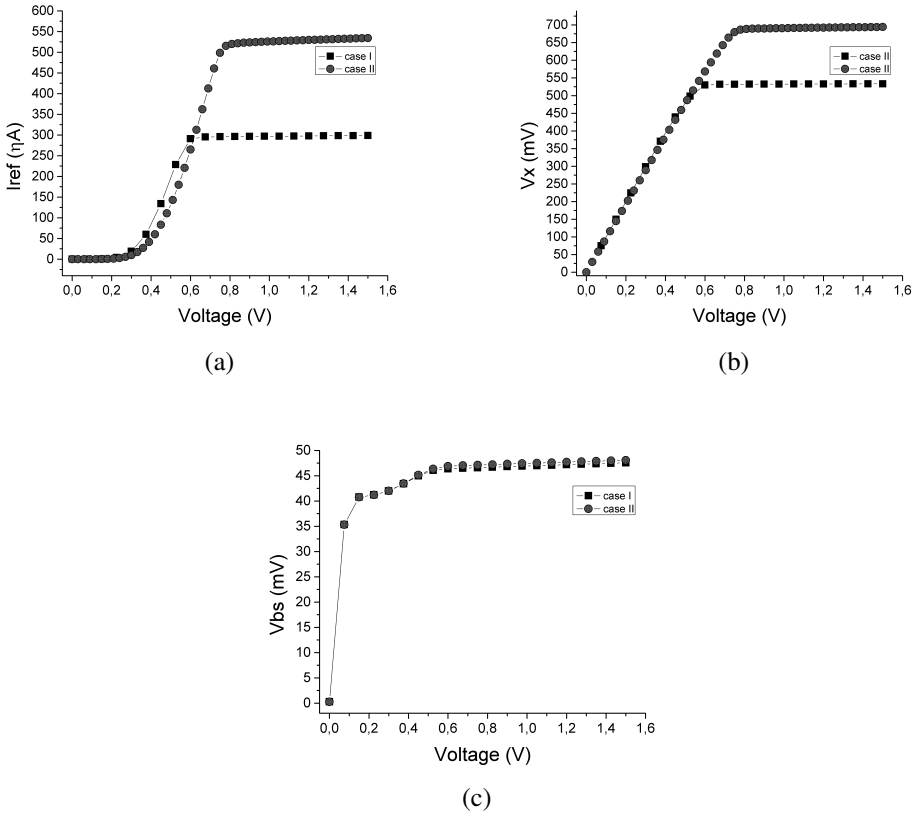


Fig. 3.17: (a) Current reference curve (b) Voltage reference curve (c) Body-Voltage generator, all of them in function of voltage supply

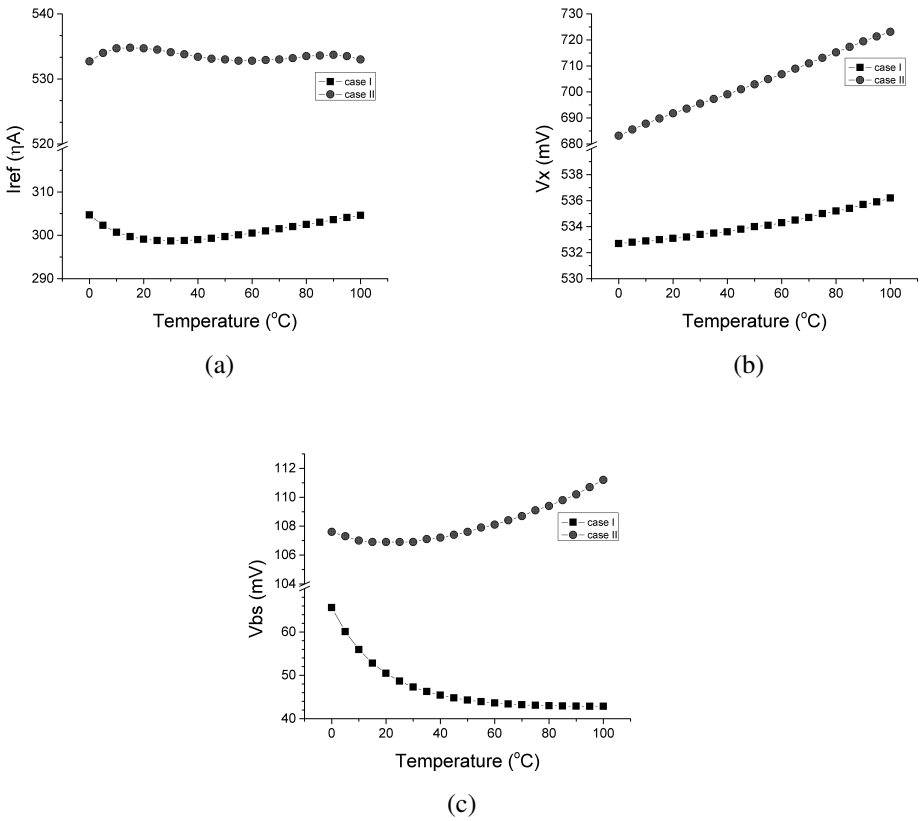


Fig. 3.18: (a) Current reference curve (b) Voltage reference curve (c) Body-Voltage generator, all of them in function of temperature variation

parameter	case I	case II
l1[μm]	5	1
l2[μm]	9	8
l3[μm]	10	9
lb[μm]	0.3	1.2
lp[μm]	5	3
w1[μm]	10	1.3
w2[μm]	100	80.1
w3[μm]	1.5	1.44
wb[μm]	0.58	0.6
wp[μm]	7	14
TC[ppm/°C]	198	40
LS[%/V]	1.51	6.03
VDD_{MIN}[V]	0.6	0.77
V_{REF}@20°C[V]	0.533	0.691
I_{REF}@20°C[nA]	298	534
PS[%]	1.36	3.81
Power Total[nW]	447	801
V_{BS}@20°C[V]	0.50	0.106

Table 3.6: Dimensions and FOM for T3-block with body-bias

Chapter 4

Conclusions

4.1 Confronting

The proposed current reference circuits were implemented in a 180nm CMOS technology, the area usage depends on the topology. The circuit can operate from a supply voltage from 0.6V to 0.77V as VDD_{MIN}, the I_{REF} can achieve in the best case 177 nA and 10uA for the worst case, the cases, where the body-bias generator was used, always have a nanoampere response whereas the first circuit present a power consumption very large in comparison to the others. The temperature coefficient in all the cases always is smaller than 50, the line sensitivity is smaller than 5 and the best results are present when the body-bias was used in the T2-block.

Table 4.2 shows the result for the three circuits implemented in this work, it is needed to know that the cases with body-bias generator present the best solution for the current reference implementation.

The first circuit, Fig 3.6, the minimum power supply voltage increases since the circuit uses different output MOSFET and the structure of the T1 block, the reference current is high because only one MOSFET is used as load transistor in the T3 block and the TC achieves a low value in the corner TT (typical-typical)

The second circuit, Fig 3.10, achieves a current reference smaller (factor 5) than

the first case and the line sensitivity is smaller than the results in [2], these results depends on the transistor sizing to implement the T2 block, the TC present a similar value and the voltage obtained from CTAT/PTAT voltage generator is under the value of state of art.

The third circuit, Fig 3.13, is the complete solution for this work, the results obtained in this circuit present the best figures of merit.

	Proposed configuration				
	1st	2nd	3rd		
Technology, nm	180	180	TT	SS	FF
I_{REF}, nA	737	145	366	355	367
T range, °C	0 to 100	0 to 100	0 to 100		
TC, ppm/°C	SS=474; TT=47; FF=392	SS=360;TT=48;FF=324	71	1000	282
Power, pW	570	460	640	220	1800
$V_{VDD_{MIN}}$, V	0.6	0.6	0.75	0.79	0.72
Line sensitivity, %/V	2.2	2.2	3.1	3.3	3
Process sensitivity, σ/μ	4.2	3.5	3.3		
Die area, μm^2	–	–	9k		
N° of elements	5T	11T	22T		

Table 4.1: Current references results

parameter	1st Improv.		2nd Improv.		VBS to T2-block		VBS to T3-block	
FOM	case I	case II	case I	case II	case I	case II	case I	case II
TC[ppm/°C]	16	18	25	23	28	17	198	40
LS[%/V]	3.45	2.64	2.41	2.89	0.66	0.99	1.51	6.03
VDD_{MIN}[V]	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.77
V_{REF}@20°C[V]	0.54	0.52	0.524	0.535	528	564	0.533	0.691
I_{REF}@20°C[nA]	7.85	10	176	188	263	342	298	534
PS[%]	3.73	2.34	2.18	2.63	1.94	7.87	1.36	3.81
Power Total[W]	11.77u	15u	263n	282n	394n	513n	447n	801n
V_{BS}@20°C[mV]	–	–	–	–	62	55	50	106

Table 4.2: Figure of Merits for all the improvements

4.2 Findings

Figure (4.1) shows the output current of all the designs, where the first of them has the greater power consumption in order of micro-amperes since the active load was implemented with one transistor only, so its sizing was wider than the others designs. The best solution was reached in the second design, where the active load was implemented with seven transistors in self-cascode mode since the transconductance is better controlled and the channel length is the adding result of the length-transistor which allows to reduce the power consumption by keeping the same gate-source voltage used to bias the active load.

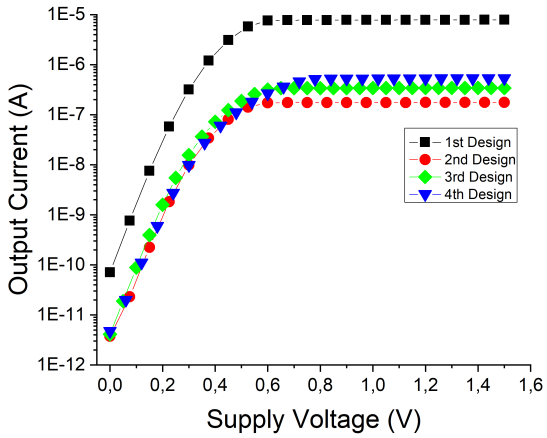


Fig. 4.1: Output Current in function of the power supply variation for all the designs

Figure (4.2) shows the output voltage from the voltage reference, the first path for the first and second design and second path for the third design, in this case the initial requirement, $V_{REF} \approx 500[mV]$, was reached by all the designs, the minimum voltage for the power supply was reached at 0.6 V, it will be possible reduce this if the initial requirement for the voltage reference is lower than the fixed in this thesis.

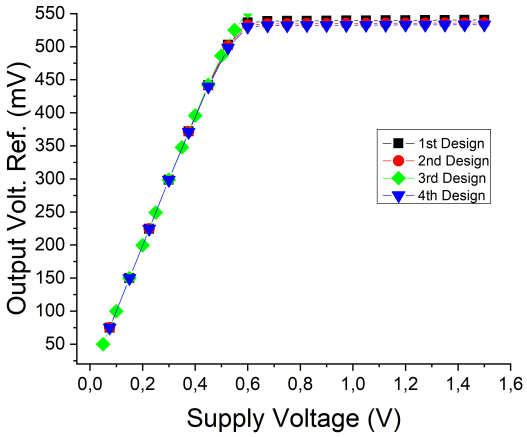


Fig. 4.2: Voltage reference response to power supply variations

Figure (4.3) shows the line sensitivity along the voltage supply variations, from 0.6 V to 1.5 V, for all these the LS was lower than 4 %/V. The best solution is given by the design where the body-bias generator was used to provide voltage to the T2-Block, since higher body-source voltage lower reference voltage, MTC point, in the active load yields a slight variation at the output current so the linear sensitivity is reduced too. When the body-bias generator is used in T3-block the reference voltage is not reduced but the body effect can be reduced in the active load, this provides an improvement at the output current.

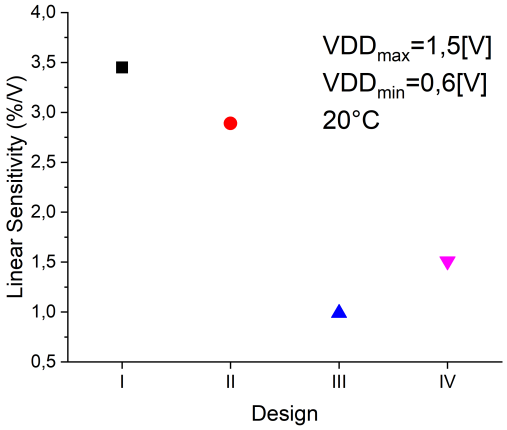


Fig. 4.3: Line sensitivity results

Figure (4.4) shows the temperature coefficient of the all designs, the first three im-

plementations show a TC lower than 20 ppm/°C, the third implementation shows the worst result due to the output current reached at the minimum voltage supply, this value is slightly greater than 0.6 V, and the temperature variations can not be driven by the active load where the body-bias is working.

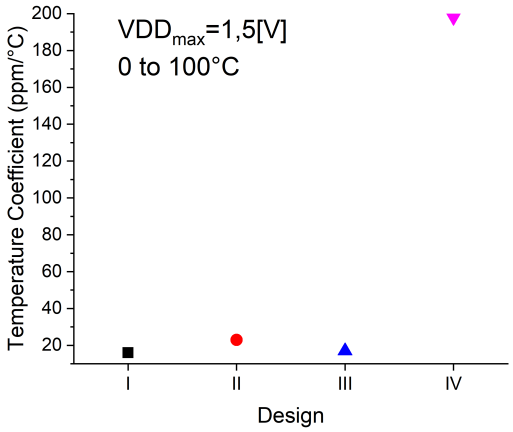


Fig. 4.4: Temperature coefficient results

Figure (4.5) shows the total power consumption of the implementations, the second circuit shows the better result since the active load is driven by seven transistors in self-cascode connection and the channel length allows a better driving the output current. In addition to the current driving, the SC connection allows to reduce the power since the bias voltage to power the active load is lower than a simple transistor with same composite channel length.

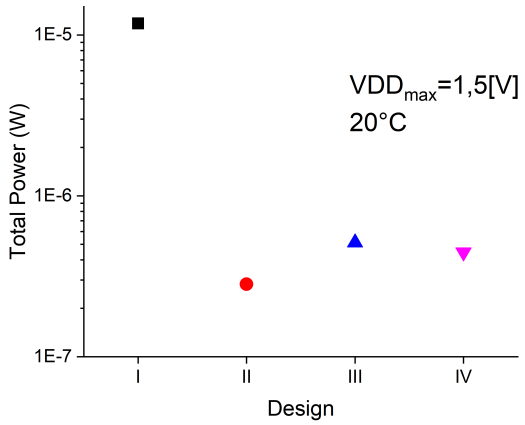


Fig. 4.5: Total Power of the current reference

Figure (4.6) shows the power consumption of the voltage reference which work is providing the reference, MTC point, to the active load, the best result is given by the design where the body-bias generator was used to bias the bulk of T2-block, for this reason the path consumes a low power since a part of the power was driven by the generator, in this path the power consumption is reduced because the sizing of the voltage reference used to generate the VBS has a low value.

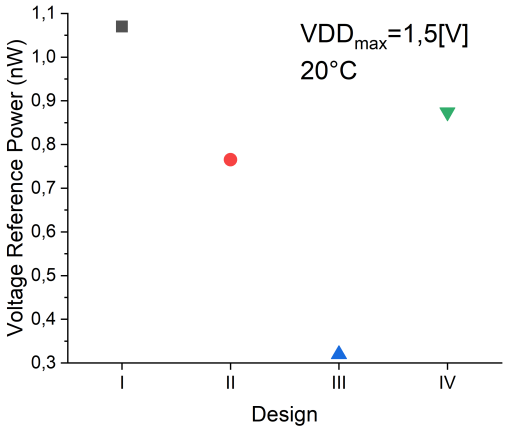


Fig. 4.6: Power of the voltage reference

4.3 Conclusions

In comparison to the 3T current reference showed in [2], these improvements need a greater area occupancy, but this increment trades off the improvements of load and process sensitivity and power consumption mainly. The conclusions are based on the improvements in the block structure showed in Fig (3.2).

- T1 block aim is controlling the line sensitivity, larger length channel, smaller line sensitivity and conductivity thus leading to reduce the impact of V_{DD} on V_x variations and consequently on I_{REF}. T1 can be implemented with different structures, shown in Fig (3.3), from a simple transistor which works in subthreshold regime since $V_{GS} = 0$, a series-connected MOSFETs where their body can either be connected to a bias voltage or ground point, this improvement allows to the body-source voltage becomes more negative so the V_{TH} and T1 block conductivity is reduced. The body to the source connection is used to avoid the body effect.

- The gate-drain connection was used to increase the threshold voltage in T2 block and consequently has a V_x more stable since a low V_{MTC} guarantees a current reference with a low voltage and low power consumption. Stacking the transistors in the T2 block leads to amplifying the difference of threshold voltages of the transistors used in the block T1 and T2.

- The T3 block improvements used series-connected transistors in order to increase the effective channel length, a larger channel, a smaller load sensitivity of the circuit. The output current can be set with the number of transistors used to implement this block. a greater number of transistors, a smaller output current I_{REF}.

- The final implementation showed in Figure (3.13), has three self-biased transistors in stacking, $M_5 - M_7$, in block T1, two transistors in diode-connected

(gate to drain), $M_8 - M_9$ in block T2 and five series-connected transistors, $M_{10} - M_{14}$for the block T3. In addition to these transistors there are a body-bias circuit with five transistors, $M_0 - M_4$, to bias the upper transistor, M8, of block T2. The number of transistor in block T2 is due to reach the V_x required. This implementation shows all the possible cases where the circuit can be controlled by the body connection, so exploiting the transistor sizing, the designer can potentially use transistors of the same type in all the three main blocks T1, T2, and T3, thus reducing significantly the process sensitivity of the current reference. The body connection can be used as a key to control the threshold voltage when the transistor works in weak region and consequently the temperature coefficient, the line sensitivity and the minimum voltage supply can be improved. If the body transistor load is biased with a voltage different to zero the V_{MTC} can be minimized so the V_x required is reduced too. The increase in the number of body connections in the circuit means a more difficult circuit to control and more area occupancy.

- If the power consumption of the voltage reference and the linear sensitivity requirements are not relevant for the aim circuit for biasing, the design depicted in Figure (2.9), can be used with the advantages that this circuit will use a smaller area occupancy and the temperature coefficient should be lower than 20 ppm/°C and the linear sensitivity will be approximately 3 %/V thus an output current dependency of the voltage supply is guaranteed.

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Appendix A

Small-signal analysis of first improvement

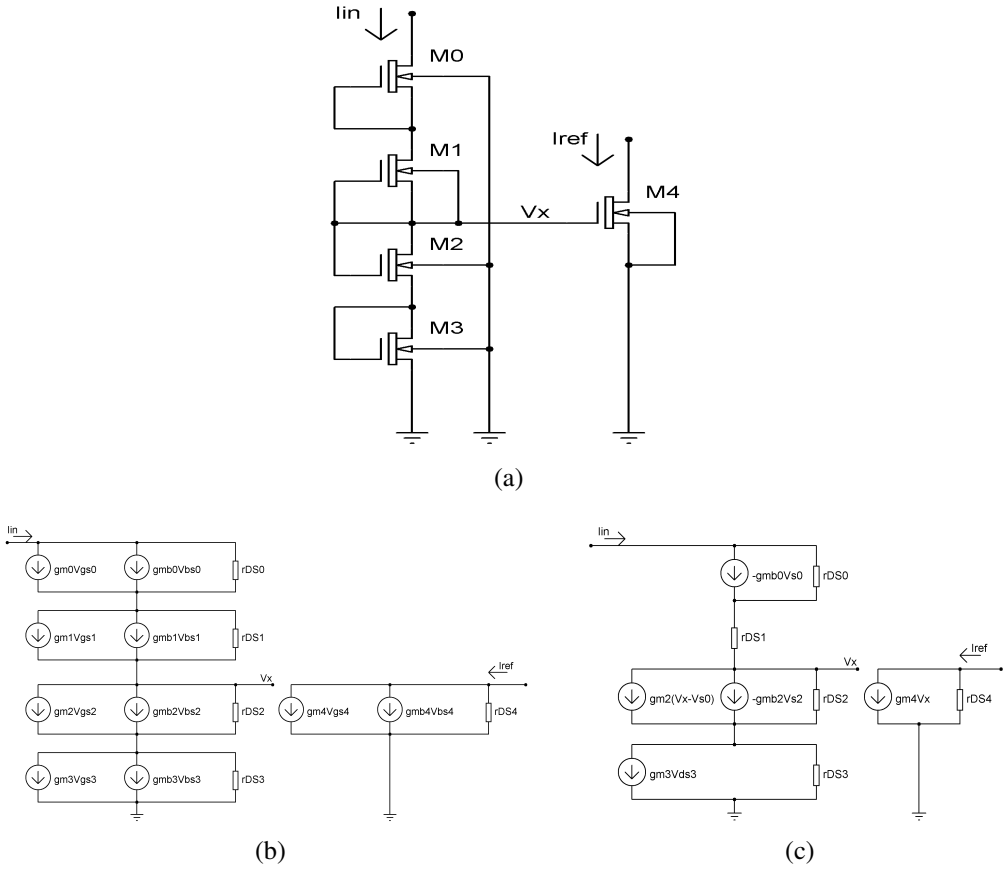

Fig. A.1: Small-signal analysis for 1st and 2nd Improvement

Since transitor M4 is driven by gate-source voltage given by the voltage reference, V_X, the voltage is calculated from the small signal circuit

$$V_X = V_{DS2} + V_{DS3}$$

$$V_{DS2} = I_{IN} r_{DS2} - gm_2 V_{DS2} r_{DS2} + gmb_2 V_{DS3} r_{DS2}$$

$$V_{DS2}\left(1 + gm_2 r_{DS2}\right) = I_{IN} r_{DS2} + gmb_2 V_{DS3} r_{DS2}$$

$$V_{DS2} = \frac{r_{DS2}}{1 + gm_2 r_{DS2}} I_{IN} + \frac{gmb_2 r_{DS2}}{1 + gm_2 r_{DS2}} V_{DS3}$$

$$V_{DS3} = I_{IN} r_{DS3} - gm_3 V_{DS3}$$

$$V_{DS3}\left(1 + gm_3\right) = I_{IN} r_{DS3}$$

$$V_{DS3} = \frac{r_{DS3}}{1 + gm_3} I_{IN}$$

$$V_X = \frac{r_{DS2}}{1 + gm_2 r_{DS2}} I_{IN} + \frac{gmb_2 r_{DS2}}{1 + gm_2 r_{DS2}} V_{DS3} + V_{DS3}$$

$$V_X = \frac{r_{DS2}}{1 + gm_2 r_{DS2}} I_{IN} + V_{DS3}\left(1 + \frac{gmb_2 r_{DS2}}{1 + gm_2 r_{DS2}}\right)$$

$$V_X = \frac{r_{DS2}}{1 + gm_2 r_{DS2}} I_{IN} + \frac{r_{DS3}}{1 + gm_3}\left(1 + \frac{gmb_2 r_{DS2}}{1 + gm_2 r_{DS2}}\right) I_{IN}$$

$$\frac{V_X}{I_{IN}} = \frac{r_{DS2}}{1 + gm_2 r_{DS2}} + \frac{r_{DS3}}{1 + gm_3}\left(\frac{1 + gm_2 r_{DS2} + gmb_2 r_{DS2}}{1 + gm_2 r_{DS2}}\right)$$

If the body effect in M2 is neglected and $gm_2 r_{DS2} \gg 1$

$$\frac{V_X}{I_{IN}} = \frac{r_{DS2}}{gm_2 r_{DS2}} + \frac{r_{DS3}}{1 + gm_3}\left(\frac{gm_2 r_{DS2}}{gm_2 r_{DS2}}\right)$$

$$\frac{V_X}{I_{IN}} \approx \frac{1}{gm_2} + \frac{r_{DS3}}{1 + gm_3}$$

The output voltage for the current reference is V_{DS4}

$$V_{DS4} = r_{DS4}\left(I_{REF} - gm_4 V_X\right)$$

the ΔI_{REF} depends on the $gm_4 V_X$ variation

$$\Delta I_{REF} = I_{REF} - \left(\frac{gm_4}{gm_2} + \frac{gm_4 r_{DS3}}{1 + gm_3}\right) I_{IN}$$

$$V_x = V_{ds2} + V_{ds3}$$

$$V_{in} = V_{ds0} + V_{ds1} + V_{ds2} + V_{ds3} = V_{ds0} + V_{ds1} + V_x$$

$$V_{ds0} = I_{in} r_{ds0} - gm_0 V_{gs0} r_{ds0} - gmb_0 V_{bs0} r_{ds0}$$

$$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{g0} - V_{s0}\right) r_{ds0} - gmb_0 \left(V_{b0} - V_{s0}\right) r_{ds0} \tag{A.1}$$

Eq. (A.8) can be reduced with the table showed below.

CASE	g0	b0
I	s0	Gnd
II	g1	Gnd
III	s0	s0
IV	g1	s0

CASE I

$V_{g0} = V_{s0}$ and $V_{b0} = 0$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{g0} - V_{s0}\right) r_{ds0} - gmb_0 \left(V_{b0} - V_{s0}\right) r_{ds0}$

$V_{ds0} = I_{in} r_{ds0} + gmb_0 V_{s0} r_{ds0} = I_{in} r_{ds0} + gmb_0 r_{ds0} \left(V_{ds1} + V_{ds2} + V_{ds3}\right)$

$$V_{ds0} = \left(r_{ds0} + gmb_0 r_{ds0} \left(r_{ds1} + \frac{1}{gm_2} + \frac{gmb_2}{gm_2 gm_3} + \frac{1}{gm_3}\right)\right) I_{in} \tag{A.2}$$

CASE II

$V_{g0} = V_{g1} = V_{s1} = V_{ds2} + V_{ds3}$ and $V_{b0} = 0$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{g0} - V_{s0}\right) r_{ds0} - gmb_0 \left(V_{b0} - V_{s0}\right) r_{ds0}$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{ds2} + V_{ds3} - V_{ds1} - V_{ds2} - V_{ds3}\right) r_{ds0} + gmb_0 V_{s0} r_{ds0}$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(-V_{ds1}\right) r_{ds0} + gmb_0 V_{s0} r_{ds0}$

$V_{ds0} = I_{in} r_{ds0} + gm_0 V_{ds1} r_{ds0} + gmb_0 \left(V_{ds1} + V_{ds2} + V_{ds3}\right) r_{ds0}$

If eq (A.6), (A.9), (A.10) are assumed, V_{ds0} is

$$V_{ds0} = I_{in} r_{ds0} + gm_0 I_{in} r_{ds1} r_{ds0} + gmb_0 \left(r_{ds1} + \frac{1}{gm_2} + \frac{gmb_2}{gm_2 gm_3} + \frac{1}{gm_3}\right) I_{in} r_{ds0}$$

$$V_{ds0} = \left(r_{ds0} + gm_0 r_{ds1} r_{ds0} + gmb_0 \left(\frac{r_{ds1} gm_2 gm_3 + gm_3 + gmb_2 + gm_2}{gm_2 gm_3} \right) r_{ds0} \right) I_{in} \tag{A.3}$$

CASE III

$V_{g0} = V_{s0}$ and $V_{b0} = V_{s0}$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{g0} - V_{s0} \right) r_{ds0} - gmb_0 \left(V_{b0} - V_{s0} \right) r_{ds0}$

$$V_{ds0} = I_{in} r_{ds0} \tag{A.4}$$

The voltage depends on current flowing through the internal resistance of the transistor, a higher W implies a small resistance and greater variation in the current, while a lower W implies a large resistance and therefore less changes in the current but reduction in the working range of tension.

CASE IV

$V_{g0} = V_{g1} = V_{s1} = V_{ds2} + V_{ds3}$ and $V_{b0} = V_{s0}$

$V_{ds0} = I_{in} r_{ds0} - gm_0 \left(V_{ds2} + V_{ds3} - V_{ds1} - V_{ds2} - V_{ds3} \right) r_{ds0}$

$V_{ds0} = I_{in} r_{ds0} + gm_0 V_{ds1} r_{ds0}$

If eq (A.6) is assumed, V_{ds0} is

$$V_{ds0} = \left(r_{ds0} + gm_0 r_{ds0} r_{ds1} \right) I_{in} \tag{A.5}$$

In this case, the voltage difference depends on the internal resistance and the change in the transconductance and internal resistance of the down transistor linked in the itself source.

$V_{ds1} = I_{in} r_{ds1} - gm_1 V_{gs1} r_{ds1} - gmb_1 V_{bs1} r_{ds1}$

$V_{ds1} = I_{in} r_{ds1} - gm_1 \left(V_{g1} - V_{s1} \right) r_{ds1} - gmb_1 \left(V_{b1} - V_{s1} \right) r_{ds1}$

$V_{g1} = V_{s1}$ and $V_{b1} = V_{s1}$

$$V_{ds1} = I_{in} r_{ds1} \tag{A.6}$$

$V_{ds1} = I_{in} r_{ds1}$

$V_{ds2} = I_{in} r_{ds2} - gm_2 V_{gs2} r_{ds2} - gmb_2 V_{bs2} r_{ds2}$

$V_{ds2} = I_{in} r_{ds2} - gm_2 \left(V_{g2} - V_{s2}\right) r_{ds2} - gmb_2 \left(V_{b2} - V_{s2}\right) r_{ds2}$

$V_{g2} = V_{d2} \rightarrow V_{gs2} = V_{ds2}\,; V_{b2} = 0\,; V_{s2} = V_{ds3}$

$V_{ds2} = I_{in} r_{ds2} - gm_2 V_{ds2} r_{ds2} + gmb_2 V_{ds3} r_{ds2}$

$$V_{ds2} = \frac{r_{ds2}}{1 + gm_2 r_{ds2}} I_{in} + \frac{gmb_2 r_{ds2}}{1 + gm_2 r_{ds2}} V_{ds3}$$

$$V_{ds2} = \frac{r_{ds2}}{1 + gm_2 r_{ds2}} I_{in} + \frac{gmb_2 r_{ds2}}{1 + gm_2 r_{ds2}} \frac{gm_3 r_{ds3}}{1 + gm_3 r_{ds3}} I_{in}$$

$$V_{ds2} = \left(\frac{r_{ds2}}{1 + gm_2 r_{ds2}} + \frac{gmb_2 r_{ds2}}{1 + gm_2 r_{ds2}} \frac{r_{ds3}}{1 + gm_3 r_{ds3}} \right) I_{in} \tag{A.7}$$

$V_{ds3} = I_{in} r_{ds3} - gm_3 V_{gs3} r_{ds3} - gmb_3 V_{bs3} r_{ds3}$

$V_{ds3} = I_{in} r_{ds3} - gm_3 \left(V_{g3} - V_{s3}\right) r_{ds3} - gmb_3 \left(V_{b3} - V_{s3}\right) r_{ds3}$

$V_{g3} = V_{d3} \rightarrow V_{gs3} = V_{ds3}\,; V_{b3} = V_{s3} = 0$

$V_{ds3} = I_{in} r_{ds3} - gm_3 \left(V_{d3} - V_{s3}\right) r_{ds3} = I_{in} r_{ds3} - gm_3 V_{ds3} r_{ds3}$

$$V_{ds3} = \frac{r_{ds3}}{1 + gm_3 r_{ds3}} I_{in} \tag{A.8}$$

If r_{ds2} and r_{ds3} are very large, eq (A.7) and eq (A.8) can be shown as:

$$V_{ds2} \approx \left(\frac{1}{gm_2} + \frac{gmb_2}{gm_2 gm_3} \right) I_{in} \tag{A.9}$$

$$V_{ds3} \approx \frac{1}{gm_3} I_{in} \tag{A.10}$$

Appendix B

Small-signal analysis of third improvement

Fig. (B.1) shows the third-improvement with modification in all the blocks and body-bias generator for T2-block.

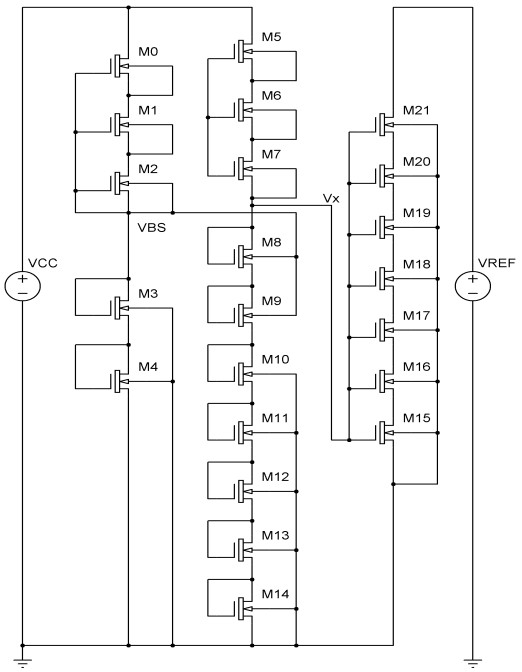

Fig. B.1: Current-reference

Small-signal for body bias generator

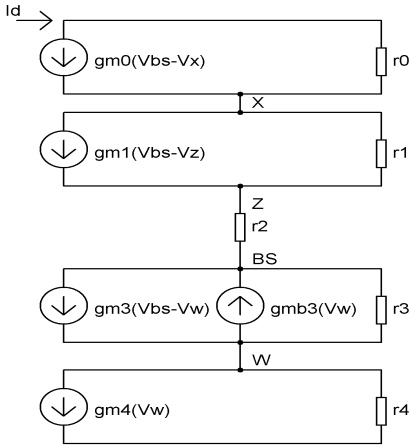

Fig. B.2: Small-signal for body bias generator

$$i_D = gm_0 V_{BS} - gm_0 V_X - \frac{V_X}{r_0} \rightarrow i_D r_0 = gm_0 r_0 V_{BS} - (gm_0 r_0 + 1) V_X$$

$$V_X = \frac{gm_0 r_0 V_{BS} - i_D r_0}{gm_0 r_0 + 1} (A)$$

$$i_D = gm_1 V_{BS} - gm_1 V_Z + \frac{V_X - V_Z}{r_1} \rightarrow i_D r_1 = gm_1 r_1 V_{BS} - (gm_1 r_1 + 1) V_Z + V_X$$

$$V_Z = \frac{gm_1 r_1 V_{BS} + V_X - i_D r_1}{gm_1 r_1 + 1} (B)$$

$$i_D = \frac{V_Z - V_{BS}}{r_2} \rightarrow i_D r_2 = V_Z - V_{BS} \rightarrow V_Z = V_{BS} + i_D r_2 (C)$$

$$i_D = gm_3 V_{BS} - gm_3 V_W - gmb_3 V_W + \frac{V_{BS} - V_W}{r_3}$$

$$i_D r_3 = gm_3 r_3 V_{BS} - gm_3 r_3 V_W - gmb_3 r_3 V_W + V_{BS} - V_W$$

$$V_W = \frac{i_D r_3 - V_{BS}(gm_3 r_3 + 1)}{1 - gm_3 r_3 - gmb_3 r_3} (D)$$

$$i_D = gm_4 V_W + \frac{V_W}{r_4} \rightarrow i_D r_4 = gm_4 r_4 V_W + V_W \rightarrow V_W = \frac{i_D r_4}{gm_4 r_4 + 1} (E)$$

A, B and C to find the relation i_D / V_{BS} when the transistor are connected in cascode mode (M0, M1 and M2)

$$V_{BS} + i_D r_2 = \frac{gm_1 r_1 V_{BS} + V_X - i_D r_1}{gm_1 r_1 + 1} \rightarrow (V_{BS} + i_D r_2)(gm_1 r_1 + 1) + i_D r_1 - gm_1 r_1 V_{BS} = V_X$$

$$(V_{BS} + i_D r_2)(gm_1 r_1 + 1) + i_D r_1 - gm_1 r_1 V_{BS} = \frac{gm_0 r_0 V_{BS} - i_D r_0}{gm_0 r_0 + 1}$$

$$V_{BS}(gm_1 r_1 + 1 - gm_1 r_1) + i_D (gm_1 r_1 r_2 + r_2 + r_1) = \frac{gm_0 r_0 V_{BS}}{gm_0 r_0 + 1} - \frac{i_D r_0}{gm_0 r_0 + 1}$$

$$i_D \left(gm_1 r_1 r_2 + r_2 + r_1 + \frac{r_0}{gm_0 r_0 + 1} \right) = V_{BS} \left(\frac{gm_0 r_0}{gm_0 r_0 + 1} - 1 \right)$$

$$i_D\left(\frac{(gm_0r_0+1)(gm_1r_1r_2+r_2+r_1)+r_0}{gm_0r_0+1}\right)=V_{BS}\left(\frac{gm_0r_0-gm_0r_0-1}{gm_0r_0+1}\right)$$
$$\frac{i_D}{V_{BS}}=-\frac{1}{(gm_0r_0+1)(gm_1r_1r_2+r_2+r_1)+r_0}$$

The transistor M2 does not have a direct relation with its transconductance because this is canceled with the connection gate-source and body-source, so its behavior is entirely resistivity, that means when there is an increasing in the drain node the current will decrease, a positive feedback loop is created. This resistance plays a main role in order to reduce the current variation when there is a voltage change on the supply. If the resistance of the transistors are so large, the current variation will be zero, ideal case, so the line sensitivity can be reduced with this part of the circuit.

D and E to find the relation i_D/V_{BS} when the transistor are connected in diode mode (M3 and M4)

$$\frac{i_Dr_4}{gm_4r_4+1}=\frac{i_Dr_3-V_{BS}(gm_3r_3+1)}{1-gm_3r_3-gmb_3r_3}$$
$$\frac{(gm_3r_3+1)}{1-gm_3r_3-gmb_3r_3}V_{BS}=i_D\left(\frac{r_3}{1-gm_3r_3-gmb_3r_3}-\frac{r_4}{gm_4r_4+1}\right)$$
$$\frac{i_D}{V_{BS}}=\frac{\dfrac{(gm_3r_3+1)}{(1-gm_3r_3-gmb_3r_3)}}{\dfrac{r_3(gm_4r_4+1)-r_4(1-gm_3r_3-gmb_3r_3)}{(1-gm_3r_3-gmb_3r_3)(gm_4r_4+1)}}$$
$$\frac{i_D}{V_{BS}}=\frac{(gm_3r_3+1)(gm_4r_4+1)}{r_3(gm_4r_4+1)-r_4(1-gm_3r_3-gmb_3r_3)}$$
$$\frac{i_D}{V_{BS}}=\frac{r_3r_4\left(\frac{1}{r_3}+gm_3\right)\left(\frac{1}{r_4}+gm_4\right)}{r_3r_4\left[\left(gm_4+\frac{1}{r_4}\right)-\left(\frac{1}{r_3}-gm_3-gmb_3\right)\right]}$$
$$\frac{i_D}{V_{BS}}=\frac{\frac{1}{r_3r_4}+\frac{gm_4}{r_3}+\frac{gm_3}{r_4}+gm_3gm_4}{-\frac{gm_4}{r_3}+gm_3gm_4+gmb_3gm_4-\frac{1}{r_3r_4}+\frac{gm_3}{r_4}+\frac{gmb_3}{r_4}}$$

If the resistances r_3 and r_4 are so large the relation can be approximated by

$$\frac{i_D}{V_{BS}}\approx\frac{gm_3gm_4}{gm_4(gm_3+gmb_3)}\approx\frac{gm_3}{gm_3+gmb_3}$$

So the transconductance showed for the M3 and M4 transistors depends on mainly of the transistor 3, remember this definition because in the next stage this transistor represents the T2-block of the voltage reference which provides the MTC point to

the load stage. On the voltage reference, this block is in function of the temperature, so the less quantity of transistor should be used.

Small-signal for voltage reference

Remark: the bias voltage for transistor M8 and M9 is give by $V_{BS} \approx i_D \frac{gm_3 + gmb_3}{gm_3} \approx i_D + i_D \frac{gmb_3}{gm_3}$ to reduce the variation the change due to the gate-source voltage should be greater than the body-source variations, so if the body effect changes the threshold voltage in a relation given by $gmb \approx \chi gm$, the voltage provided to M8 and M9 will be $(\approx i_D + i_D\chi)$, where χ is given by $\frac{\partial V_{TH}}{\partial V_{SB}}$, so a change in the body voltage, it will increase the drain current of the transistors, the variation given to this node must be small and slow along the temperature variation.

The second stage is composed by a second voltage reference, M5-M7 in series connection and M8 and M9 in diode-connected mode the next transistors were neglected in the implementation. In this case the conductivity of the block can be driven with the body-bias generator since the VBS generated in the previous stages helps to reduce the voltage reference so the MTC point can be reduced and the linear sensitivity on the load too.