

**UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ**

**Colegio de Ciencias e Ingenierías**

**On the Implementation of Proportional Resonant Controller  
for a Three-Leg Voltage Source Converter**

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**Ingeniería Electrónica**

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DE TRABAJO DE INTEGRACIÓN CURRICULAR**

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Controller for a Three-Leg Voltage Source Converter**

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## RESUMEN

Este artículo informa sobre el diseño y la implementación de un sistema de control para un inversor de voltaje trifásico de tres ramales para operación autónoma con cargas balanceadas y desbalanceadas. El inversor de voltaje es modelado en el plano estacionario  $\alpha\beta$ . El diseño del controlador es un compensador de corriente y voltaje proporcional resonante. La validación del controlador es realizada por simulación e implementación. La simulación se realiza en PLECS, y la implementación se realiza en una nano-red. Los resultados se obtienen probando el controlador en un prototipo en funcionamiento autónomo.

Palabras clave: Inversor de voltaje, controlador proporcional resonante, convertidor trifásico,

## ABSTRACT

This paper reports the design and implementation of a control system for a three phase three-leg voltage source inverter operating in autonomous operation under balanced and unbalanced loads. The voltage source inverter is modeled in the  $\alpha\beta$  stationary frame. The designed controller is a proportional resonant current and voltage compensator. Validation of the controller is done by simulation and implementation. The simulation is performed in PLECS, and the implementation is performed in a nano-grid. Results are obtained by testing the controller in a prototype on autonomous operation.

Key words: Voltage source inverter, proportional resonant controller, three phase converter.

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# On the Implementation of Proportional Resonant Controller for a Three-Leg Voltage Source Converter

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**Abstract**—This paper reports the design and implementation of a control system for a three phase three-leg voltage source inverter operating in autonomous operation under balanced and unbalanced loads. The voltage source inverter is modeled in the  $\alpha\beta$  stationary frame. The designed controller is a proportional resonant current and voltage compensator. Validation of the controller is done by simulation and implementation. The simulation is performed in PLECS, and the implementation is performed in a nano-grid. Results are obtained by testing the controller in a prototype on autonomous operation.

## I. INTRODUCTION

In the last years voltage source inverters (VSI) have become an important part in electric and electronic development. Part of these developments are focused in distributed generation. Distributed generation (DG) is defined as a small source of electric power generation that is not a part of a large central power. Examples of distributed generation are photo voltaic solar panels and wind-power turbines. Benefits of distributed generation is less environmental impact and cheaper electricity [1]. DG requires power converters, in particular power inverters. An example of this are some renewable energy generators such as photovoltaic generator, in this case we need an inverter to link it to the grid.

Electric systems have some characteristics such as frequency, amplitude, phases, phase and sequence. All of which have to be regulated in order to obtain an effective power transfer from the source to the load. The pulse width modulation (PWM) voltage source inverter (VSI) has been one of the most used blocks for electric power systems [2]. It was developed due to advances in semiconductor technology, which allows us to have higher switching frequency, and higher voltage and current management.

In order to control the VSI different compensators could be employed, one of the most common is the proportional integral compensator (PI). PI compensators exhibit certain problems in the steady state performance, if we want to achieve good results with the PI controller with voltage feedforward in the synchronous frame, modifications are required which can be difficult to implement using a low-cost digital processor [3]. The proportional resonant compensator(PR) is a good alternative in the stationary frame control, getting the same transient and steady-state performance as the PI with feedforward path regulator in the synchronous  $dq$  frame. [4]

This paper is organized in the following way: Section II explains the model and the design of the controller. Section III presents and describes the simulation results of the converter in autonomous operation under balanced and unbalanced loads. Section IV describes the implementation performed, the software programming and the materials used. Section V describes the results under balanced and unbalanced load for the implementation. finally in section VI conclusions are presented.

## II. SYSTEM MODEL AND CONTROL DESIGN

The model of this system has been presented in the paper [2], so only the main representative equations are shown in this section. The system model is shown in Figure (1b). The modulation technique used for simulations and implementation is the well-known Sinusoidal Pulse With modulation (SPWM) technique. The two level three-leg VSI is composed by two semiconductor transistors per leg, with a total of 6 devices. These will allow to have in the terminal voltage  $v_t$  either  $V_{dc}/2$  or  $-V_{dc}/2$  on each leg depending on which of the power devices is active.

Furthermore, this section focuses on design of a P+Resonant compensator for the 3-Leg VSI Control algorithms as PI, PID are not the best alternatives tracking sinusoidal reference in a stationary frames, this problem is due to the dynamics of the integral term. This inability to track the sinusoidal reference present the need to use the grid voltage as a feed-forward term to obtain a good dynamic response helping the controller to reach steady state faster. The PR controller provides gain at a specific frequency, the resonant frequency, limiting the gain almost only for these frequency. These will help us to conceptually achieve zero tracking error. In [5] we may observe a comparison between PI and PR controllers. PI controller with voltage feed-forward suffers from an steady state error that was approximately 9% following the current reference, on the other hand PR controller this error is reduced to 0%.

### A. System Model

The System Equation in alpha-beta reference frame in the time dome is described by equation (1). For detail description of the model see [2]

$$\mathbf{v}_{t\alpha\beta} = R\mathbf{i}_{\alpha\beta} + L\frac{d\mathbf{i}_{\alpha\beta}}{dt} + \mathbf{v}_{L\alpha\beta} \quad (1)$$

## B. P+Resonant Controller

The PR controller transfer function is shown in equation (2). As it is mentioned in [6], the PR compensator introduces an infinite gain at a certain resonant frequency  $\omega_0$  which eliminates the steady state error at  $\omega_0$ . It is similar to an PI compensator, in which the infinite DC gain forcing the steady-state error to zero.

$$G_c(s) = K_p + \frac{2K_r s}{s^2 + \omega_0^2} \quad (2)$$

The ideal PR compensator presents stability problems due to the infinite gain. To avoid stability problems a non-ideal PR controller may be used. The gain of the resonant frequency is now finite, but high enough to follow the reference with practically zero steady-state error. The non ideal PR controller is described in equation (3). Another feature of (3) is that unlike (2), the band-width can be widened by setting  $\omega_c$ , which can be useful sensibility towards small frequency variation in utility grid [6].

$$G_c(s) = K_p + \frac{2K_i \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (3)$$

## C. Current Controller

The closed loop current control system can be described by the equation (4) in the alpha-beta reference frame in the frequency domain.

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \frac{G_d(s)G_{CC}(s)}{R + sL + G_d(s)G_{CC}(s)} \begin{bmatrix} I_\alpha^* \\ I_\beta^* \end{bmatrix} \quad (4)$$

Where  $G_{CC}(s)$  is the proportional resonant current controller and  $G_d(s) = 1/(T_d s + 1)$  is the time delay transfer function that consider the PWM delay and the computation delay

## III. SIMULATION OF THE CONTROLLER

This section presents the controller simulation made in PLECS. From figure (1) We can see the models of the power system and the power controller in the Alpha-Beta frame. The simulations are made for autonomous operation, it consists of the three-leg voltage source inverter connected to an RLC branch. simulations will be done for balanced and unbalanced loads, and voltage value will variate in order to see the controllers response. From figure (1b) we can see the power controller in the  $\alpha\beta$  frame designed in Plecs. The reference voltage is compared to the voltage measured in the load, after that the PR compensator sends the signal which is compared to the measured current, at last the current controller sends the signal to the PWM generator block which controls the VSI.

The  $\alpha$  and  $\beta$  voltage compensator is presented in equation (5), it is designed based in the non ideal PR compensator presented in equation (3).

$$G_{c_{\alpha\beta}}(s) = 1.05 + \frac{800s}{s^2 + 10s + 142122.3} \quad (5)$$

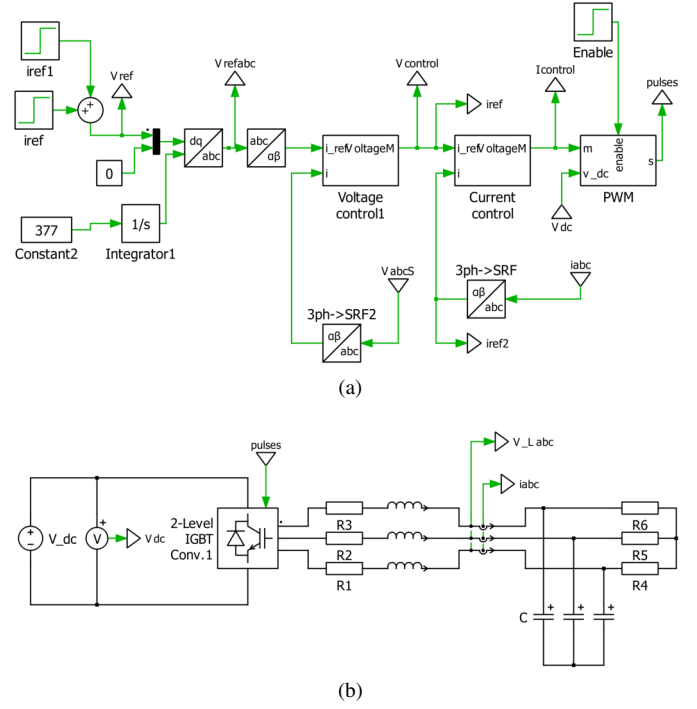


Fig. 1: Closed loop Voltage control - Autonomous Operation: (a) Power system model (b) Controller model

These compensator is designed for  $\omega_0 = 60H_z$  frequency, it has a high gain for these frequency.

### A. Case Study 1

This simulation is based on the power system shown in figure (1), considering the following parameters: The DC link voltage is  $V_c = 50[V]$ , the RLC branch has values of  $L = 1330[\mu H]$ ,  $C = 100[\mu f]$ ,  $R = 10[\Omega]$ . The inductor resistance is also considered with a value of  $0.2\Omega$ .

In this simulation the magnitude of the voltage reference is stepped in order to test the voltage controller. At time  $t = 0$  the voltage is set in  $20[V]$ , at time  $t = 0.1$  the voltage is  $25[V]$ , finally at time  $t = 0.2$  setpoint is set at  $15[V]$ .

The results of the simulation are shown in figures (2), (3) and (4). As we can see in the results the voltage source inverter has a small time response to the reference variation. So the results are as expected. The controller works just as fine when the voltage reference increases as when it decreases.

### B. Case Study 2

This case study examines the behavior of the converter under balanced load variation but it is requested to maintain a constant voltage value of  $V = 20[V]$ . The example employs the same parameters as the case study 1. At tome  $t = 0.15$  resistance load switches from  $R = 10\Omega$  to  $R = 15\Omega$ .

The results of the simulation case 2 are shown in figures (5), (6) and (7). In figure (5) at the time loads variate it is shown a variation that is stable in a small period of time. In figure (7) it is shown the current variation. The variation in current is as expected when voltage is constant. The resistance load increases so the current decreases.



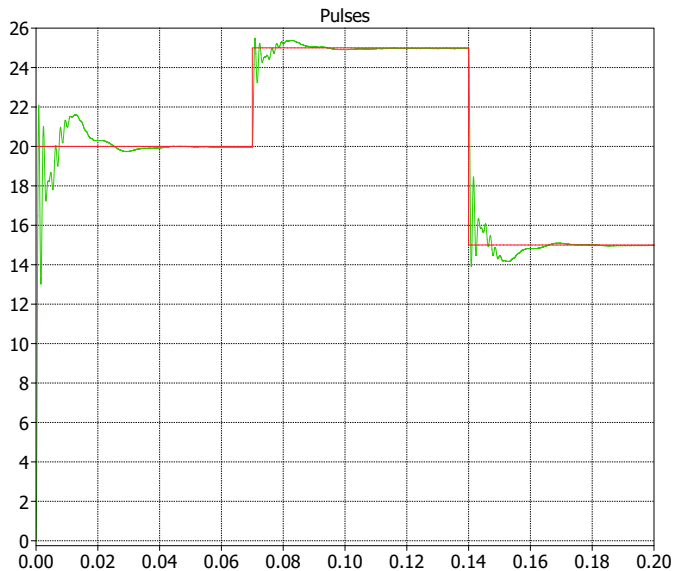


Fig. 2: Voltage time Response  $dq$  frame case study 1

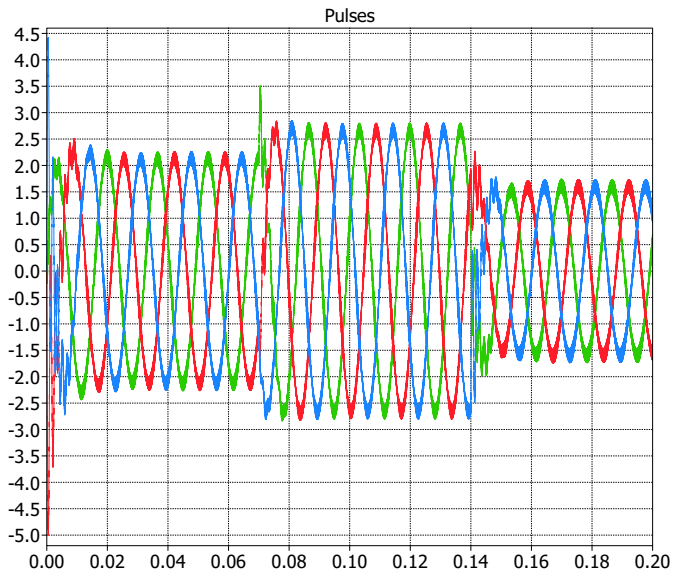


Fig. 4: Current time response in the  $abc$  stationary frame case study 1

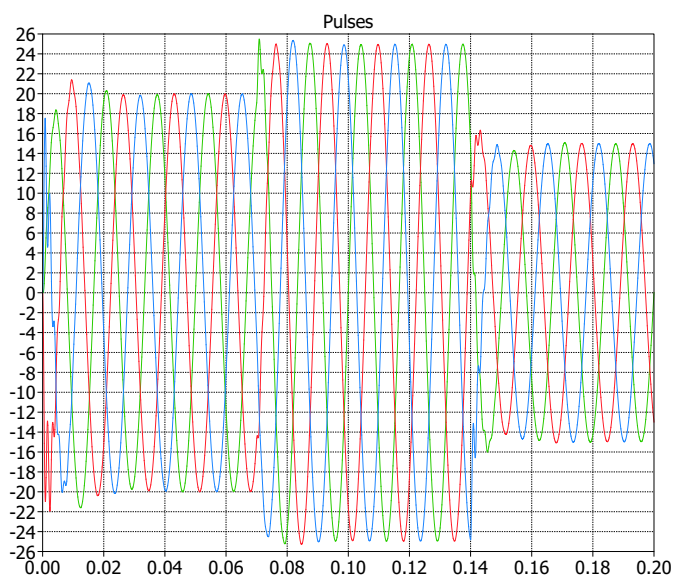


Fig. 3: Voltage time response in the  $abc$  stationary frame case study 1

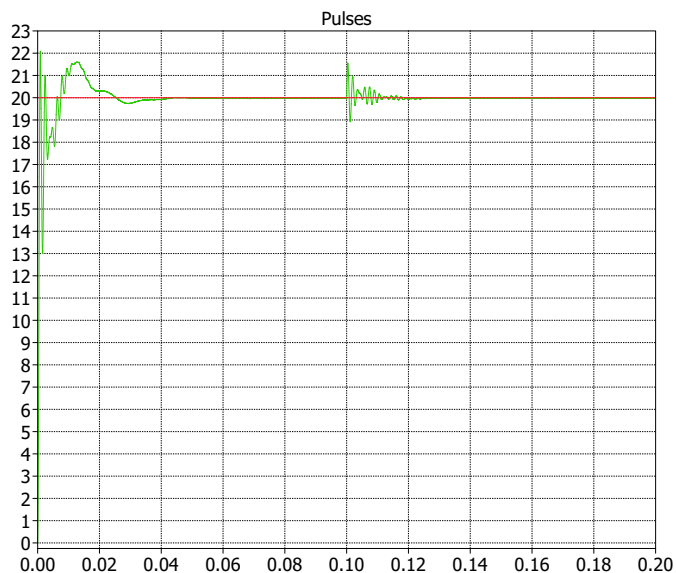


Fig. 5: Voltage time Response  $dq$  frame case study 2

TABLE I: Load Variation

Time[s]	Load	Value
0	$R_1$	$10\Omega$
0	$R_2$	$10\Omega$
0	$R_3$	$10\Omega$
0.15	$R_1$	$15\Omega$
0.15	$R_2$	$10\Omega$
0.15	$R_3$	$10\Omega$

#### IV. IMPLEMENTATION

This section presents the implementation of the 3 leg VSI. For the implementation there was used a electronic power equipment from Francecol shown in figure(11). This equipment is build with an Texas Instruments DSP F2808. The

#### C. Case Study 3

The following case studies the voltage control model will be tested under sudden changes in one of their loads. The simulation is based on the table (1). The load variation is described in table (I). The variation changes the loads from balanced to unbalanced.

The results of the simulation are shown in figures (8), (9) and (10). As it is shown in the results, when load changes from balanced to unbalanced loads, the controller manages voltage to maintain constant. Current changes in all of the branches to compensate the unbalanced loads showing the correct response to the variation.

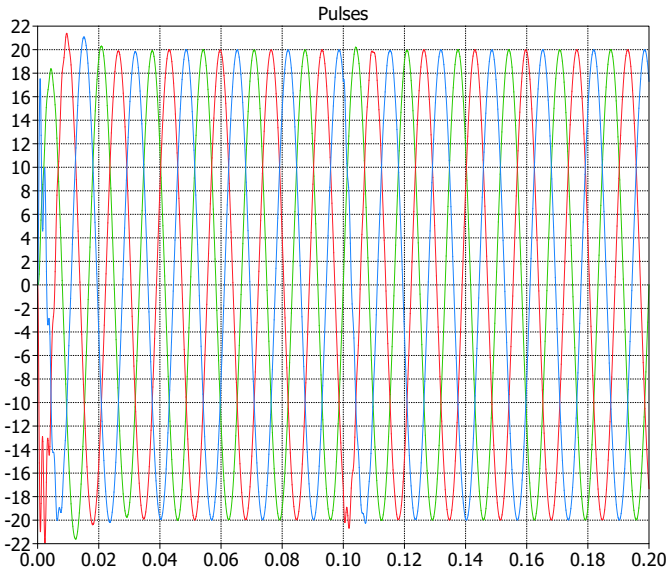


Fig. 6: Voltage time response in the *abc* stationary frame case study 2

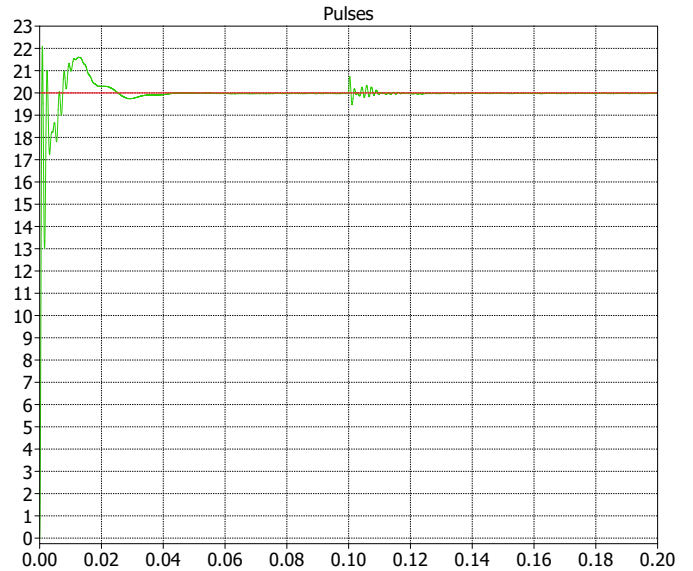


Fig. 8: Voltage time Response *dq* frame case study 3

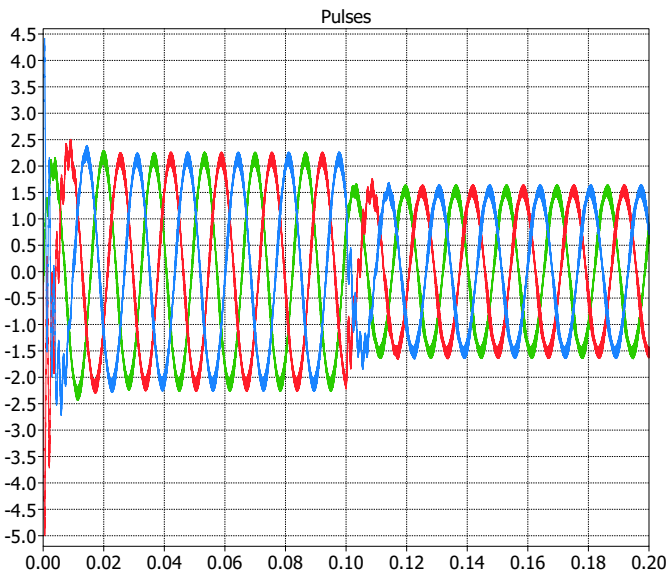


Fig. 7: Current time response in the *abc* stationary frame case study 2

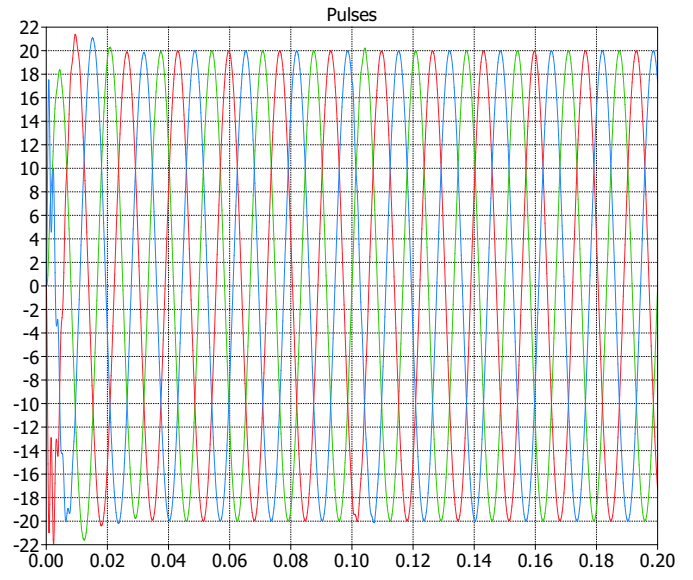


Fig. 9: Voltage time response in the *abc* stationary frame case study 3

TABLE II: Prototype Parameters

ConverterParameters	Symbol	Value
Input Voltage	$V_{DC}$	50V
Digital Controller	DSP	TMSF2808
Three phase inductor	L	1330 [ $\mu H$ ]
Three phase resistor	R	10 or 15 $\Omega$
Switching Frequency	$f_{sw}$	10 kHz

programming of the DSP was done in Altair Embed. Altair Embed is a software that generates code from block diagram models. This code is then uploaded in the DSP flash memory using Code Composer from Texas Instruments. Besides from the Francecol power equipment there were needed to build two more circuit boards, the first of which has the voltage sensors that were needed to perform the voltage control, we can see it in figure (12), this board allows us to modify the gain and the offset so that the analog input of the DSP, which reads from 0 to 3 [V] could read the voltage. Then the second one which had the loads that allows us to make the load variation with switches shown in figure (13).

The parameters that were considered when building the prototype are the ones shown in table (II).

#### A. Programming

Altair Embed is the software used for the programming. The block diagram used is the shown in the figure (14). There are three inputs user determined which are the input DC voltage, the desired output ac voltage and the frequency. Other inputs are the voltage and the current measurements, All of these

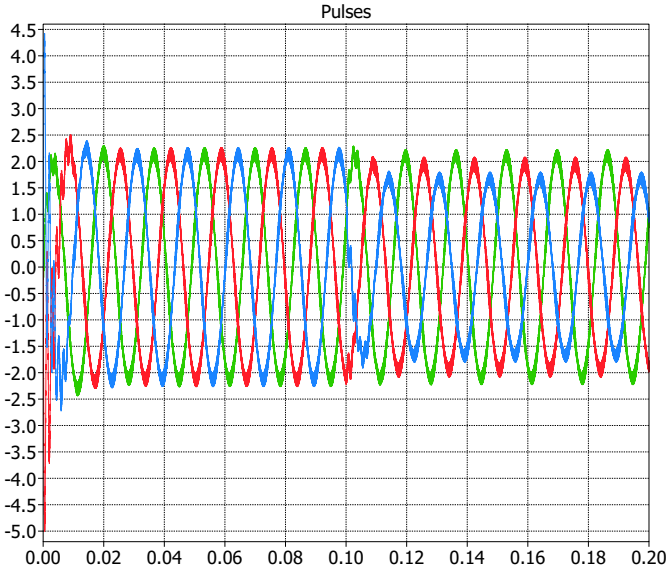


Fig. 10: Current time response in the  $abc$  stationary frame case study 3

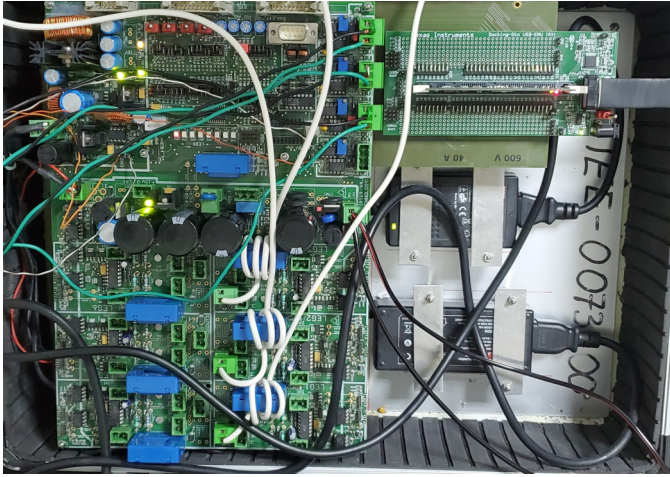


Fig. 11: Francecol Power Module

are transformed to the  $u_\alpha u_\beta$  frame. In the voltage and current control blocks the control of voltage and current is done, in the figure (15) is shown the control used. At last control values are sent to the PWM block for the switching, in figure (16) we can see the programming of PWM.

The control block presented in figure 15 is built in base of the design of the controller shown in the equation 5. The control block is the same for the voltage and the current control.

The PWM control block shown in figure 16 is the one that controls the output switching. The PWM is configured with the following properties: Switching frequency  $f_{sw} = 10kHz$ , deadband is 50, the count mode is up/down.

## V. RESULTS

In this section results of different scenarios when using the prototype implemented are presented. Measurements are done

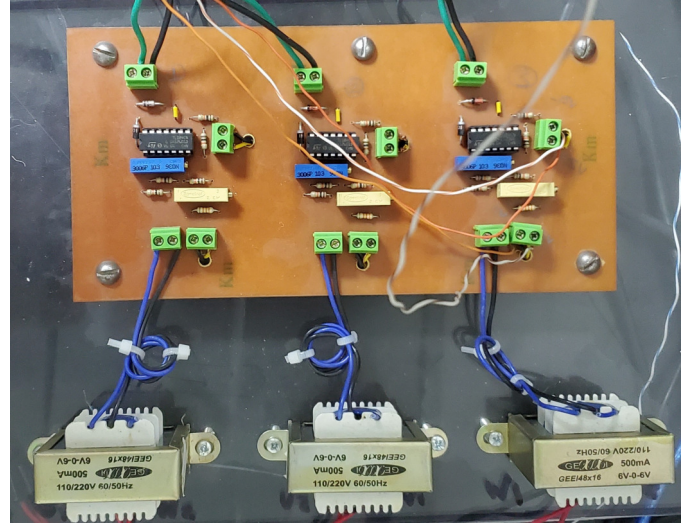


Fig. 12: Voltage sensors

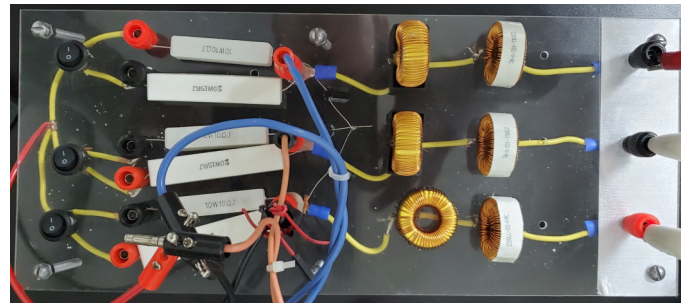


Fig. 13: Loads

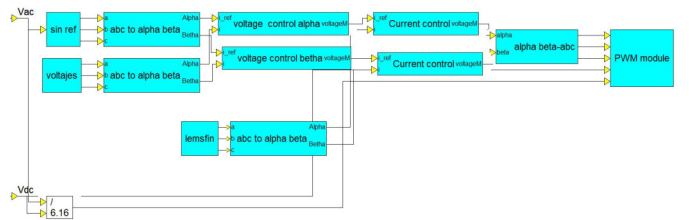


Fig. 14: Block diagram

with an Agilent 2 channel oscilloscope, in which we measure voltage on the resistor load.

### A. Case 1

The first result presented in figure (17) is the voltage control when the load remains constant. The input voltage  $V_{DC} = 50[V]$ , the desired output voltage at time  $t = 0[s]$  is  $V_{out} = 8[V]$  in a second instance at time  $t = 0.09[s]$  the voltage reference is set at  $V_{out} = 18[V]$ , frequency is  $f_{out} = 60[Hz]$ . As shown in figure (17) the voltage change can be observed when the reference changes, and then it reaches the stability in a small period of time.

### B. Case 2

The second result shown in figure (18) is to change one load, switching the system from balanced to unbalanced. The



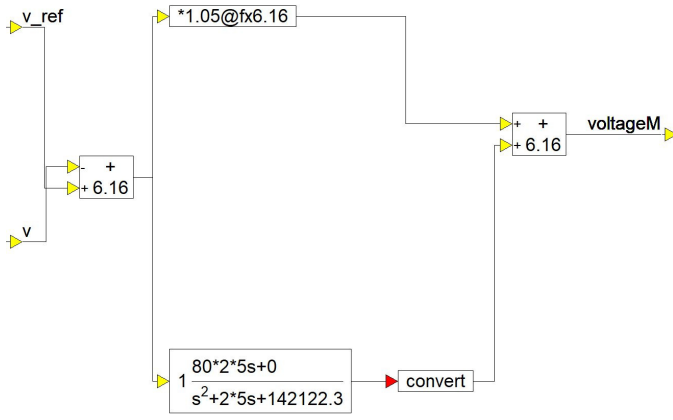


Fig. 15: Voltage and current block diagram

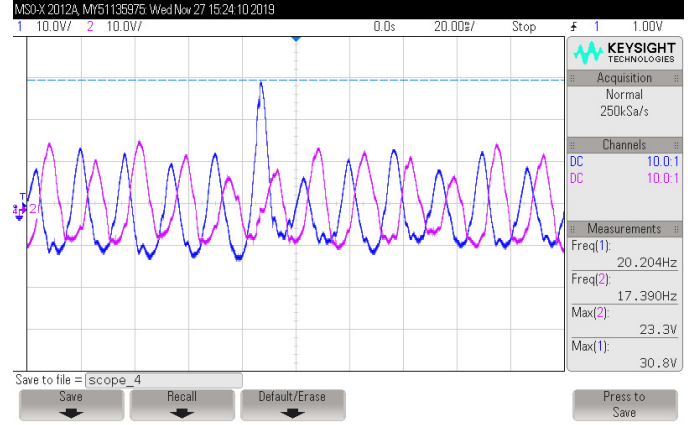


Fig. 18: Voltage measured when load changes

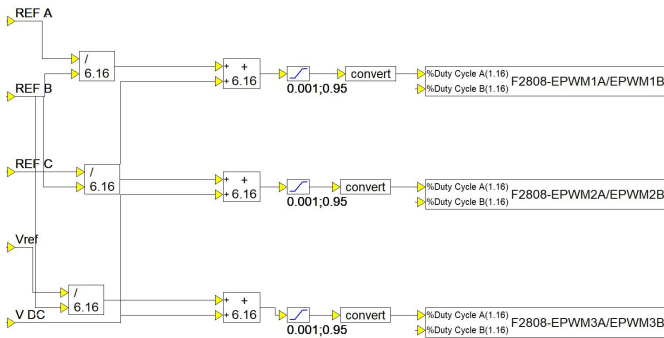


Fig. 16: Voltage and current block diagram

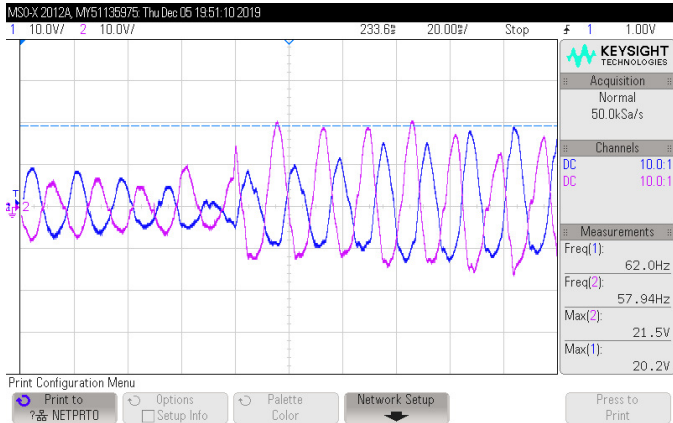


Fig. 17: Voltage measured when voltage reference varies

switching is performed with the loads board shown in figure (13). In this case the input voltage is  $V_{DC} = 50[V]$ , the output reference is (18), the load variation is the one described in table (I). frequency is set at  $f_{out} = 60[Hz]$ . In the figure we can observe the transient in the voltage response and then the voltage continuous in its values, this is an indication that the controller is working just as expected.

## VI. CONCLUSIONS

In this paper the stationary frame control design and implementation of three-leg voltage source inverter is presented. The proportional resonant compensator gives us a zero error tracking the sinusoidal reference of current and voltage. on both the simulation and the implementation.

A disadvantage of this controller is that is tuned for an specific frequency, in our case  $60[Hz]$ . In distributed generation this is not a big problem since the AC grid frequency works in practically only one value of frequency, on the other side if the frequency varies significantly the controller will not track the reference value.

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