UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio de Ciencias e Ingenierías

Dual Mode Logic – High speed and energy efficient address decoder

.

Adriana Monstserrat Arévalo Checa
Kevin Andrés Vicuña Barriga

Ingeniería Eléctrica y Electrónica

Trabajo de fin de carrera presentado como requisito
para la obtención del título de
Ingeniero Electrónico

Quito, 08 de mayo de 2020

UNIVERSIDAD SAN FRANCISCO DE QUITO USFQ

Colegio de Ciencias e Ingeniería

HOJA DE CALIFICACIÓN
DE TRABAJO DE FIN DE CARRERA

Dual Mode Logic – High speed and energy efficient address decoder

Adriana Monstserrat Arévalo Checa

Kevin Andrés Vicuña Barriga

Nombre del profesor, Título académico	**Ramiro Taco, PhD**
Nombre del profesor, Título académico	**Luis Prócel, PhD**

Quito, 08 de mayo de 2020

DERECHOS DE AUTOR

Por medio del presente documento certifico que he leído todas las Políticas y Manuales de la Universidad San Francisco de Quito USFQ, incluyendo la Política de Propiedad Intelectual USFQ, y estoy de acuerdo con su contenido, por lo que los derechos de propiedad intelectual del presente trabajo quedan sujetos a lo dispuesto en esas Políticas.

Asimismo, autorizo a la USFQ para que realice la digitalización y publicación de este trabajo en el repositorio virtual, de conformidad a lo dispuesto en el Art. 144 de la Ley Orgánica de Educación Superior.

Nombres y apellidos: Adriana Monstserrat Arévalo Checa

Código: 00133017

Cédula de identidad: 1726447889

Nombres y apellidos: Kevin Andrés Vicuña Barriga

Código: 00130813

Cédula de identidad: 1718186214

Lugar y fecha: Quito, 08 de mayo de 2020

ACLARACIÓN PARA PUBLICACIÓN

Nota: El presente trabajo, en su totalidad o cualquiera de sus partes, no debe ser considerado como una publicación, incluso a pesar de estar disponible sin restricciones a través de un repositorio institucional. Esta declaración se alinea con las prácticas y recomendaciones presentadas por el Committee on Publication Ethics COPE descritas por Barbour et al. (2017) Discussion document on best practice for issues around theses publishing, disponible en http://bit.ly/COPETheses.

UNPUBLISHED DOCUMENT

Note: The following capstone project is available through Universidad San Francisco de Quito USFQ institutional repository. Nonetheless, this project – in as a whole or in part – should not be considered a publication. This statement follows the recommendations presented by the Committee on Publication Ethics COPE described by Barbour et al. (2017) Discussion document on best practice for issues around theses publishing available on http://bit.ly/COPETheses.

RESUMEN

La lógica CMOS consiste en la utilización de los transistores de efecto de campo (MOSFET) de canal tipo p (PMOS) y de canal tipo n (NMOS), con una configuración que permite cuando el dispositivo esté apagado, el consumo de energía sea solo por la presencia de corrientes parásitas. Sin embargo, la lógica CMOS se caracteriza por ser lenta y presenta un alto consumo de energía. El objetivo de este estudio consiste en plantear una alternativa que puedan solventar los problemas mencionados anteriormente. En específico, se considera la creación de un decodificador de direcciones eficiente utilizando la Lógica de Modo Dual. De esta manera, se busca reducir el retardo de propagación y el consumo de energía en comparación con la lógica CMOS.

El decodificador de direcciones propuesto se creará mediante el uso de compuertas lógicas NAND y NOR. Las compuertas se dimensionan en el análisis del peor de los casos. Además, se realiza un análisis de consumo de energía y retardo de las compuertas y el circuito de la cadena NAND-NOR, antes de la construcción del decodificador de direcciones. Por lo tanto, se realiza el análisis de las dos topologías de Lógica de Modo Dual del decodificador de direcciones. La comparación entre el modelo de Lógica de Modo Dual y CMOS se realiza en sus dos modos de operación, estático y dinámico.

Palabras clave: decodificador de direcciones, compuertas, cadena NAND-NOR, Lógica de Modo Dual, energía, retardo, topología.

ABSTRACT

The CMOS logic consists of the use of the p-type channel (PMOS) and n-type channel (NMOS) field effect transistors (MOSFET), with a configuration that allows that when the device is turned off, the energy consumption is only due to the presence of parasitic currents. Currently, this logic is the most widely used to produce integrated circuits on a large scale. However, it has been detected that CMOS logic presents propagation delay and high energy consumption issues. The aim of this study is to offer an alternative that can solve the problems mentioned above. Specifically, it is considered the creation of an efficient address decoder using Dual Mode Logic. In this way, it seeks to reduce propagation delay and energy consumption in comparison with CMOS logic.

The proposed address decoder will be created using NAND and NOR logic gates. The gates are sized in the worst-case analysis. In addition, an analysis of energy consumption and delay of the gates and the NAND-NOR chain circuit is performed, before the construction of the address decoder. Therefore, the analysis of the two Dual Mode Logic topologies of the address decoder is performed. The comparison between the Dual Mode Logic and CMOS model is performed in its two modes of operation, static and dynamic.

Keywords: address decoder, gates, NAND-NOR chain, Dual Mode Logic, energy, delay, topology.

TABLE OF CONTENTS

TABLE INDEX

FIGURE INDEX

INTRODUCTION

Dual Mode Logic (DML) is a technique that allows the exchange between two operation modes: static and dynamic. This permutation is determined by a control signal (Shavit, Taco & Fish, 2018). DML devices can be divided into Type-A and Type-B footless or footed topologies, which provide additional characteristics in both operational modes. The footed typed DML allows a considerable decrease in pre-charge time. Nevertheless, it has negative effects on the overall performance of the device. On the other hand, the footless Dual Mode Logic has a small gate drain capacitance resulting in an improvement on gate speed and evaluation time, but the pre-charge period is longer and can produce a negative effect on the robustness (Levi, Bass, Kaizerman, Belenky & Fish, 2012).

The basic topology of DML consists in the use of a basic CMOS gate with an additional transistor, which is used for the control signal. The control signal is connected to a clock signal (Rani & Mallikarjuna, 2014). The control signal transistor is connected in parallel to the network depending on the type of logic that needs to be implemented in the design (Moyal, Levi, Teman & Fish, 2016). A PMOS transistor connected in parallel to the Pull Up Network (PUN) demonstrates a Type-A logic, and a NMOS transistor parallel to the Pull Down Network (PDN) a Type-B logic (Kaizerman, Fisher & Fish, 2013).

According to the characteristics of the transistors used in the different types of logics, the control signal CLK allows two different phases known as pre-charge and evaluation (Suresh et al., 2015). These phases determine the output of the device, with an output evaluated by the values of the inputs when the device is an evaluation phase and a charge/discharge variation in the output of a pre-charge phase due to the control signal CLK (Shavit, Stanger, Taco & Fish, 2018).

The main purpose of this work is to perform the analysis and address decoder using DML and CMOS families. An address decoder is the implementation of a binary decoder that contains two or more inputs for address bits and one or more outputs for device selection signals (Horowitz & Hill, 1989). In this work, address decoders are designed by using NAND and NOR gates in DML and CMOS logic families to accomplish a comparison between these different technologies. The main goal that has been tried to be achieved as a result of this investigation is a high speed and energy efficient address decoder.

DESIGN AND ANALYSIS OF NAND AND NOR GATES

This section explains the methodology required for a proper design of the logic gates used in the implementation of the address decoder using CMOS and DML logic families. The tool Custom Compiler from Synopsys is being used to carry out simulations in order to evaluate the topologies. The simulations are performed for energy and propagation delay measurements in each of the stages to achieve an address decoder, which provides a good performance. NAND and NOR gates are designed with MOSFET transistors using 32 nm technology considering a voltage supply (VDD) of 1.2V for CMOS and DML. For DML gates, it is considered all topologies of this family: Type-A footed and unfooted, and Type-B headed and unheaded, which can be observed in Figure 1.

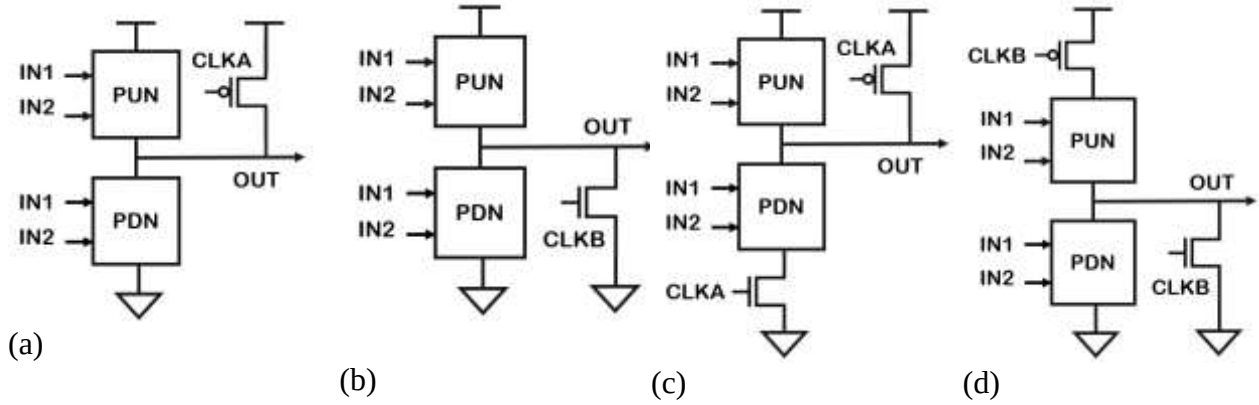

Figure 1. General DML gates. (a) Type-A unfooted. (b) Type-B unheaded. (c) Type-A footed. (d) Type-B headed.

To design a CMOS gate with multiple fan-in's, it must be contemplated the combination of inputs that induces the least favorable conditions (Rabaey, Chandrakasan & Nikole, 2003). The CMOS sizing is performed considering the worst-case delay and a balanced voltage transfer curve (VTC) to ensure that the PMOS and the NMOS transistors pulls the same amount of current (Rabaey, Chandrakasan & Nikole, 2003). When only one of the NMOS devices turns on, the worst transition happens for the CMOS NAND gate (Rabaey, Chandrakasan & Nikole, 2003). While, for the CMOS NOR gate, the worst case occurs when in the PUN just one PMOS transistor is on (Amirtharajah & Baas, 2011).

DML gates present an unconventional sizing to reduce the device capacitances and to achieve a fast pre-charge time (Levi & Fish, 2013), in which the DML transistors of the complementary network are sized to the minimum dimensions (Yuzhanino, Levi & Fish, 2015). The minimum width of the transistor gate (Wmin) for this technology is 0.23 µm. In Table 1, it has been sized the NAND with two inputs (NAND2), NAND with three inputs (NAND3), NOR with two inputs (NOR2) and NOR with three inputs (NOR3).

Table 1 Dimensions of the Gates

Gates	Network	CMOS $[\mu m]$	Dual Mode Logic			
			Type A		Type B	
			Unfooted $[\mu m]$	Footed $[\mu m]$	Unheaded $[\mu m]$	Headed $[\mu m]$
NAND2	PUN	1.10	0.23	0.23	1.10	1.55
NAND2	PDN	0.77	0.77	1.05	0.23	0.23
NOR2	PUN	1.55	0.23	0.23	1.55	1.90
NOR2	PDN	0.46	0.46	0.77	0.23	0.23
NAND3	PUN	1.10	0.23	0.23	1.10	1.55
NAND3	PDN	1.05	1.05	1.3	0.23	0.23
NOR3	PUN	1.90	0.23	0.23	1.90	2.05
NOR3	PDN	0.46	0.46	0.77	0.23	0.23

The next step is to perform measurements for both, delay and energy. These measures will allow the comparison of the DML and CMOS topologies of gates. Additionally, the results will let us realize the strong aspects of each logical family. For DML gates in the dynamic operation,

the delay is measured during evaluation (Yuzhaninov, Levi & Fish, 2015). The results of delay measurements are presented in Table 2.

Table 2. Delay of Gates

Delay [ps]					
Gates				NAND2	NOR2
CMOS				30,4	27,4
DUAL MODE LOGIC	Type-A	Unfooted	Static	25,6	62,7
			Dynamic	19,2	4,96
		Footed	Static	18,8	88,1
			Dynamic	7,8	5,21
	Type-B	Unheaded	Static	30,2	24,4
			Dynamic	6,61	21,1
		Headed	Static	29,9	35,5
			Dynamic	7,37	10,5

In static mode, DML Type-A footed NAND is faster than CMOS, since the delay of these DML gates represents approximately 60% the delay of a CMOS gate, on the other hand, DML Type-A unfooted has a delay that is only 20% lower than CMOS. The delay of CMOS NAND is almost five times greater than the delay of DML Type-B NAND headed and unheaded gates in dynamic mode. Among all DML topologies, the fastest is Type-B unheaded NAND in the dynamic mode with a delay of 22% of the delay of a CMOS gate. The Type-B unheaded NAND is the slowest in static mode, however, its delay is less than CMOS NAND delay by 2%. The DML Type-A NAND footed gate in the static operating state has the lowest delay, about half

the delay of the CMOS gate. Unlike the other gates, the DML Type-A NAND unheaded gate has similar propagation delays in both operation modes.

The DML Type-A footed and unfooted NOR in dynamic mode has the highest operating speed, since the delay of these topologies are less than 20% of the CMOS NOR delay. The delay of DML Type-A footed and unfooted NOR gates in static mode is greater than twice the delay of the CMOS gate. DML in all its topologies in dynamic mode has a lower delay than CMOS, for NOR gate. The DML type-A footed NAND gate in static mode has the highest delay.

In terms of delay, for the NAND gate the DML Type-B headed in dynamic mode is the best, while for the NOR gate the DML Type-A unfooted in dynamic mode is the fastest.

The next step is to perform the energy measurements using the equation 1.

$$Energy = \frac{V_{DD}}{N}\int_{0}^{NT} i(t)\,dt \qquad (1)$$

The energy was measured for CMOS and DML in static and dynamic mode, as can be observed in Table 3. DML Type-B headed NAND energy consumption in static mode is approximately 40% of gate power consumption implemented in CMOS and in static mode it is just 4% higher than CMOS consumption. DML Type-A NAND gate energy consumption is slightly less than 70% of CMOS consumption. As shown in the table, the energy consumption of the DML gates in static mode is less than the energy consumption of CMOS. DML Type-B unheaded NAND has the highest energy consumption in the dynamic state, since the consumption of this gate is 47% higher than the consumption of the CMOS gate.

The energy consumption of DML Type-A footed NOR in both operation modes is slightly less than 56% of the consumption of the CMOS gate. The energy consumption of DML Type-A NOR in all topologies and modes of operation is less than the energy consumption of CMOS

gates. DML Type-B headed NOR in dynamic mode and DML type-B unheaded NOR in static mode have a higher delay with a percentage more than 20% of CMOS consumption.

The DML Type-B headed in static mode has the lowest energy consumption for NAND gate, while for NOR gate the best topology is DML Type-A footed in static mode.

As it can be observed in Table 1 and Table 2, there is a trade-off between energy consumption and operation speed of the logic gates. The energy consumption of DML in static mode, with the types A or B according to the transistor configuration of the gates, is lower than the consumption of CMOS. DML in dynamic mode in the evaluation state has higher speed than CMOS.

Table 3. Energy consumption of gates

Energy [fJ]					
Gates				NAND2	NOR2
CMOS				1,63	1,70
DUAL MODE LOGIC	Type-A	Unfooted	Static	0,88	1,38
			Dynamic	1,04	1,14
		Footed	Static	1,08	0,95
			Dynamic	1,08	0,93
	Type-B	Unheaded	Static	1,38	1,45
			Dynamic	2,41	1,95
		Headed	Static	0,66	1,75
			Dynamic	1,71	1,04

ANALYSIS OF THE NAND-NOR CHAIN

The NAND-NOR chain circuit consists of twenty gates alternating NAND and NOR gates. This circuit is studied using CMOS and DML logic families. The DML NAND-NOR chain is built using the best topologies regarding performance and delay according to the previous section as shown in Figure 2. The DML NAND-NOR chain is built using NAND Type-B and NOR Type-A, and a headed or footed gate every five gates. In this implementation, a Type-A gate followed by a Type-B gate or vice versa is considered, because as Amirtharajah and Baas (2011) mention: "all dynamic logic must apply a proper cascading policy of evaluation networks to ensure correct data propagation". In the case of CMOS logic, an analysis with the NAND-NOR chain is performed to determine the worst case delay, and average energy per operation of the circuit in comparison to DML.

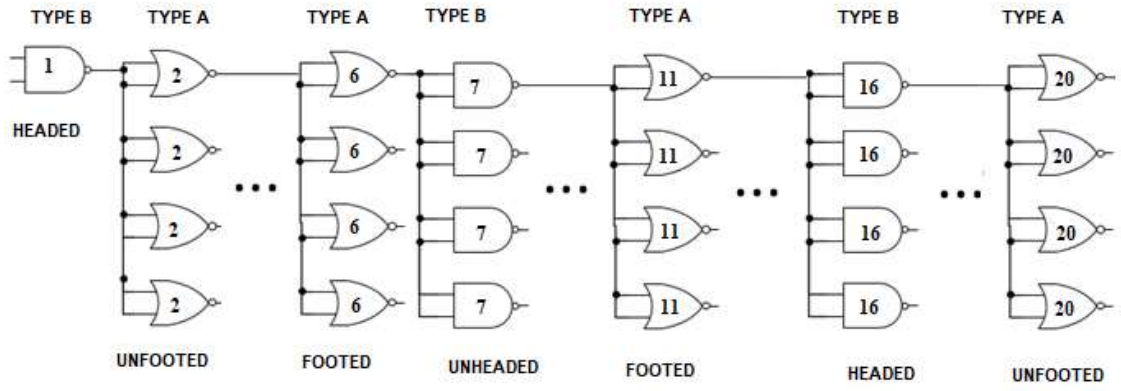

Figure 2. NAND NOR Chain implemented using Dual Mode Logic.

The delay of the NAND-NOR chain circuit using CMOS and DML is analyzed for a range of VDD from 0.4V to 1.2V as shown in Figure 3.

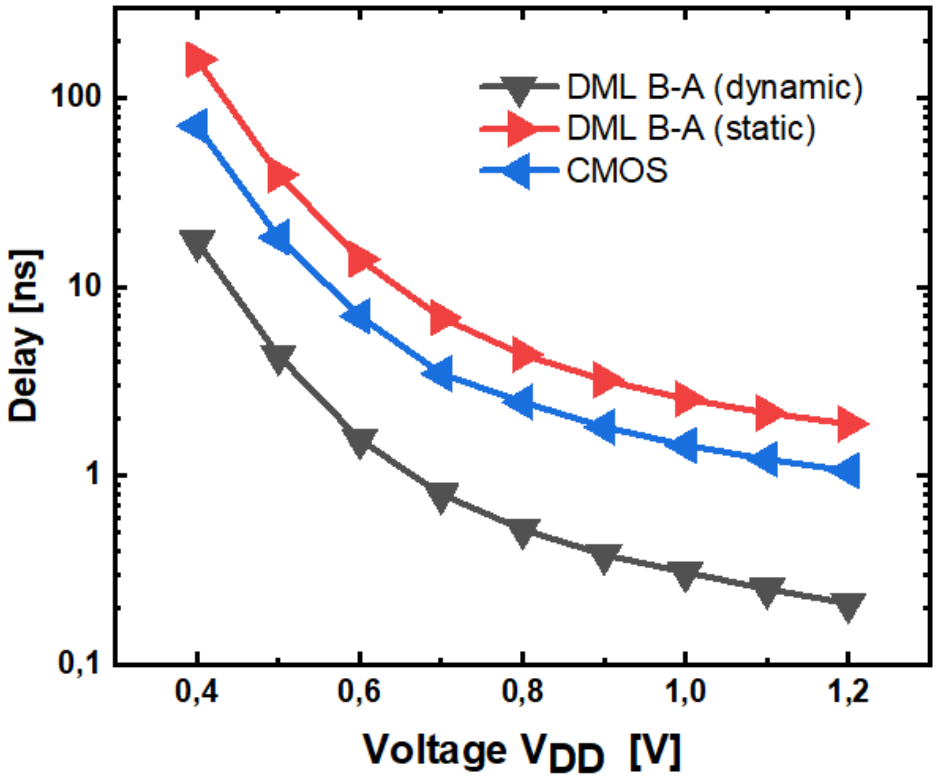

Figure 3. Delay in function of Voltage VDD for NAND-NOR chain.

In Figure 3, DML B-A implies that a Type-B NAND gate and a Type-A NOR gate are used in the circuit. Figure 3 shows that the speed of the device increases as the voltage VDD increases. DML NAND-NOR chain circuit operation in dynamic mode presents the lowest delay, while this circuit in static mode has the highest delay. The NAND-NOR chain implemented using CMOS logic is faster than DML in static mode, since the average delay of DML logic is almost twice the delay of CMOS, but it is slower than DML in dynamic mode by 80 %.

The average energy consumption per operation of the NAND-NOR chain circuit using CMOS and DML in both modes is analyzed for a range of voltage VDD from 0.4V to 1.2V as shown in Figure 4.

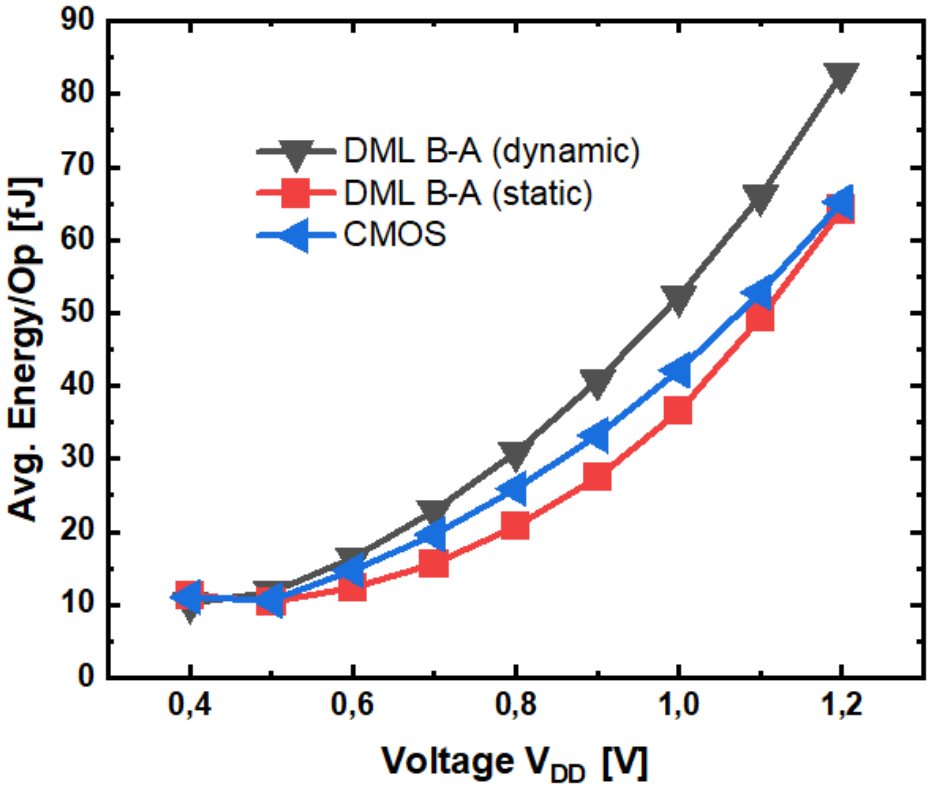

Figure 4. Average Energy per Operation versus Voltage VDD for NAND-NOR chain.

Figure 4 shows that the average energy consumption per operation increases as voltage VDD increases. The DML NAND-NOR chain in dynamic mode consumes the most amount of energy with a consumption that represents approximately an additional 20% of the CMOS energy consumption, while the same circuit in static mode has the lowest energy consumption being approximately 15% less than the consumption of CMOS. CMOS NAND-NOR chain has an energy consumption higher than DML in static mode, but its consumption is lower than DML in dynamic mode. Furthermore, the average energy consumption of DML NAND-NOR chain in dynamic mode increases faster with respect to voltage than CMOS.

DESIGN AND ANALYSIS OF ADDRESS DECODER

In this part, the previous results will be used to design and evaluate an address decoder of 1024 bits implemented with NAND and NOR gates using 32nm MOSFET technology in DML and CMOS logic families. The general topology of an address decoder of $2^n - 1$ bits is presented in Figure 6.

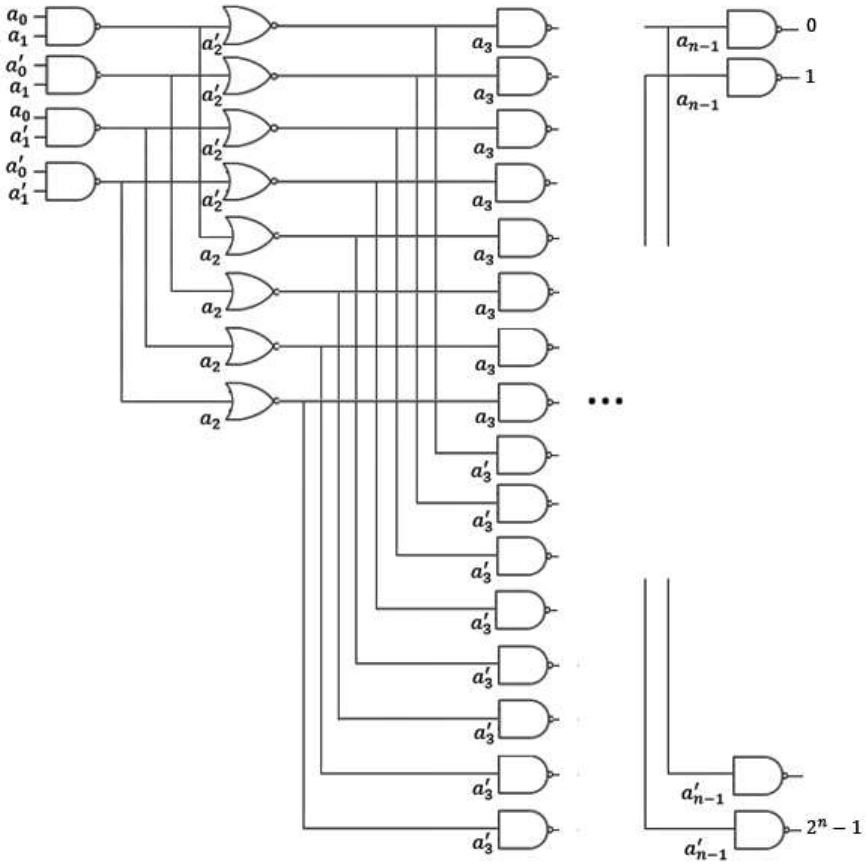

Figure 5. Topology of an Address Decoder.

This address decoder is composed by four branches arising from the first four NAND gates of the circuit. For DML address decoder, two topologies have been developed. In design, we alternate a Type-A gate and a Type-B gate to avoid short circuits and erroneous value outputs as was mentioned in the previous section of the NAND-NOR chain. The first topology (B-A) implements NAND Type-B and NOR Type-A. The second topology (A-B) is formed by NAND type A and NOR type B. Both topologies are considered in order to find the circuit with

the best performance and low energy consumption. The first four gates are footed or headed accordingly to the topologies in order to avoid short circuits in dynamic mode as clock and input transitions occur. The rest of the gates are unheaded or unfooted to have less energy consumption and the device uses the less physical area.

To determine the best topology to design an address decoder, performance and energy consumption are analyzed for the address decoder implemented with CMOS and the two topologies of DML (B-A and A-B) in static and dynamic modes.

A delay analysis is performed in function of supply voltage VDD ranging from 0.4V to 1.2V and the results are shown in Figure 7.

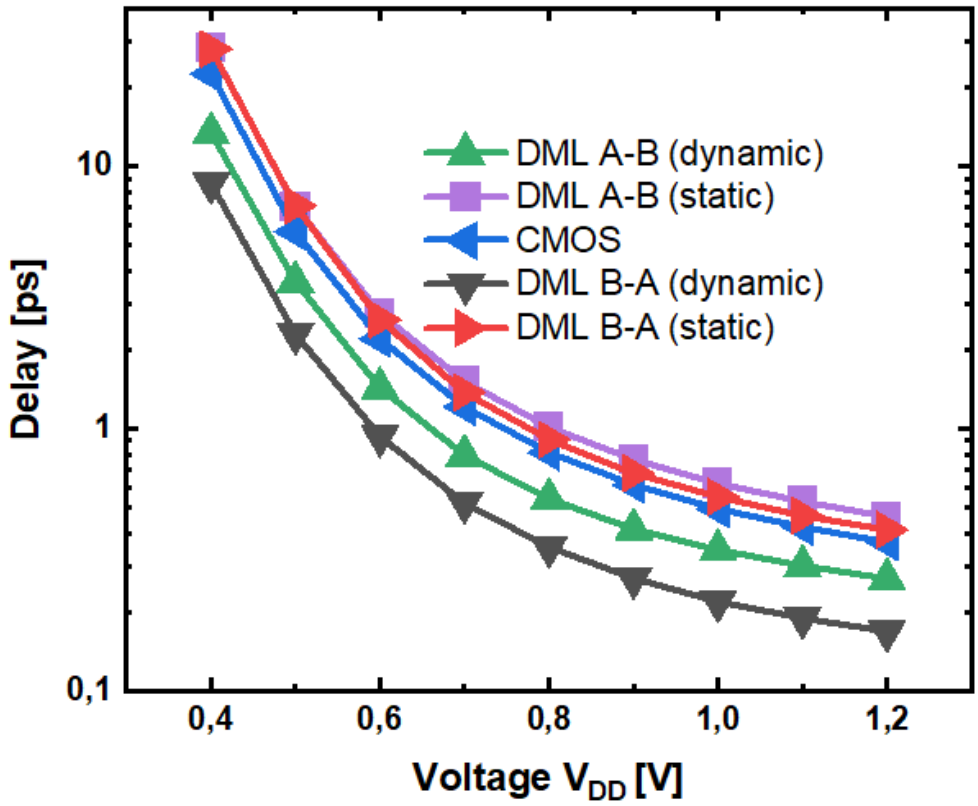

Figure 6. Delay versus Voltage VDD for Address Decoder.

The DML B-A topology in dynamic mode of operation has a propagation delay that is less than CMOS by approximately 58%, while the delay of the DML A-B in dynamic mode is less than CMOS by 33%. The address decoder implemented using CMOS is faster than DML B-A and DML A-B in static mode, since the delay of DML topologies is about 25% greater than circuit delay with CMOS logic. In the case of DML, the B-A topology has a delay that is approximately 56% less than the delay of the A-B topology in dynamic mode. While in static mode, the B-A topology is barely 12% faster than the A-B topology. The DML delay in dynamic mode constitutes approximately a third of the DML delay operating in static mode for the two topologies. As can be noted, the CMOS delay is less than the DML delay in static mode but is greater than the DML delay in dynamic mode.

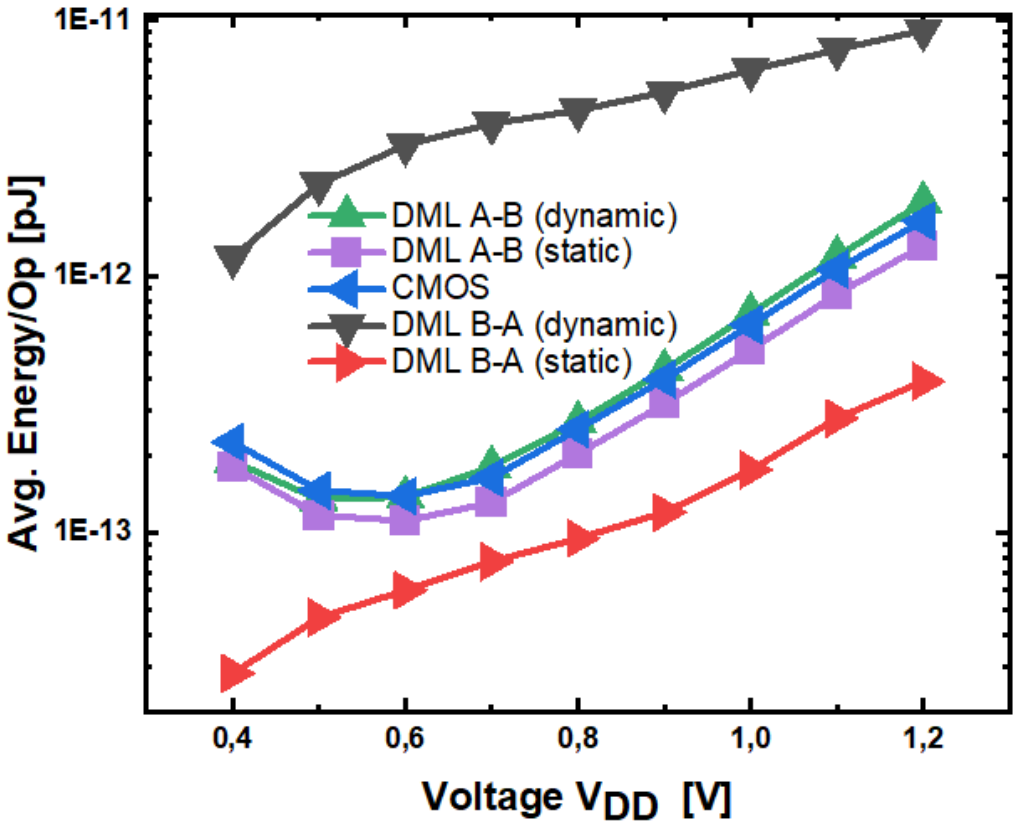

Figure 7. Energy Consumption per operation versus VDD for Address Decoder.

The average energy consumption per operation in function of supply voltage for each of the Address Decoder topologies defined by the DML and CMOS logic families are shown in Figure 8. DML B-A energy consumption in static mode represents only about 30% of the energy consumption of the address decoder implemented with CMOS logic. DML A-B in static mode only represents 20% savings in energy consumption compared to CMOS. The energy consumption of DML A-B in dynamic mode is strongly high compared to CMOS since on average it is fourteen times higher than the consumption of CMOS. DML A-B energy consumption in dynamic mode is slightly higher than CMOS energy consumption by approximately 5%.

CONCLUSIONS

This project discusses the benefits of logical families CMOS and DML. DML tries to achieve an improvement in operating time and energy consumption, but there is always a trade-off between energy and time. It is noted that as operation time improves there is a higher power consumption. The DML A-B address decoder presents an optimal behavior concerning performance and energy consumption in both modes of operation, since the delay in dynamic mode can be less than CMOS by 33% with a 5% increase in energy, and in static mode the energy saving compared to CMOS can be 20% with a delay 25% greater than the delay CMOS. The DML B-A address decoder is the fastest in dynamic mode with a propagation delay that is approximately 42% of the CMOS delay, but it implies an energy cost that is approximately average fourteen times more than the consumption of CMOS. The DML B-A address decoder presents the lowest energy consumption in static mode with 70% energy savings compared to CMOS, at the cost of performance degradation with a delay that is approximately 15% higher than CMOS delay. The CMOS family accomplishes an intermediate behavior with respect to DML in both operation modes in terms of speed and energy consumption and allows the device to use a smaller area. The CMOS family is slower than DML in dynamic mode, and faster than DML in static mode. The CMOS family consumes more energy than DML in static mode, and less energy than DML in dynamic mode. The logical family and the mode of operation that were chosen for the implementation will depend on the type of application required.

BIBLIOGRAPHIC REFERENCES

Amirtharajah, R. & Baas. (2011). *CMOS Logic*. University of California, Intel Corporation.

Kaizerman, A., Fisher, S. & Fish, A. (2013). Subthreshold Dual Mode Logic. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *21* (5), 979-983.

Levi, I., Bass, O., Kaizerman, A., Belenky, A. & Fish, A. (2012). High speed Dual Mode Logic Carry Look Ahead Adder. *2012 IEEE International Symposium on Circuits and Systems (ISCAS),* 3037-3040.

Levi, I., and Fish, A. (2013). Dual Mode Logic—Design for Energy Efficiency and High Performance. *IEEE Access*, *1*, 258-265.

Moyal, L., Levi, I., Teman, A. & Fish, A. (2016). Synthesis of Dual Mode Logic. *INTEGRATION, the VLSI journal*, *55*, 246-253.

Horowitz, P. & Hill, W. (1989). *The Art of Electronics* (2nd Ed.). Cambridge University Press.

Rabaey, J., Chandrakasan, A. & Nikole, B. (2003). *Digital Integrated Circuits. A design perspective.* Prentice Hall Electronics and VLSI Series.

Rani, D. & Mallikarjuna, R. (2014). LOGIC EFFORT OF CMOS BASED DUAL MODE LOGIC GATES. *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), 3* (11).

Shavit, N., Stanger, I., Taco, R. & Fish, A. (2018). Process Variation-Aware Datapath Employing Dual Mode Logic. *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Burlingame, CA, USA*, 1-3.

Shavit, N., Taco, R. & Fish, A. (2018). Efficiency of Dual Mode Logic in Nanoscale Technology Nodes. *2018 IEEE International Conference on the Science of Electrical Engineering in Israel (ICSEE),* 1-4.

Suresh, U., Bhargav, C., Prasad Babu, K., Sudhkar, K. & Chakrapani, T. (2015). Dual Mode Logic – Design for Energy Efficiency and High Performance Carry Skip Adder. *International Journal of Innovative Science, Engineering & Technology, 3* (9).

Yuzhaninov, V., Levi, I. & Fish, A. (2015). Design Flow and Characterization Methodology for Dual Mode Logic. *IEEE Access*, *3*, 3089-3101.